Daffodil International University

Daffodil Smart City (DSC), Savar, Dhaka

Department of Computing and Information System

Semester Project on

Computer Architecture and Organization [CIS - 131]

Semester Fall-2024

Prepared By	Submitted To
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Acknowledgement

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I am grateful to Daffodil International University for providing me with an environment that has helped me develop my knowledge and skills.

Lastly, I would like to dedicate this project to those who are differently abled and have a thirst for knowledge. Their determination and resilience are a true inspiration to us all.

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Theory Part:

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Task 1:

Q1: Do you believe Mr. Israfil's mention of the topics he will cover during the Fall 2024 semester is sufficient to teach students about computer architecture and organization? Justify your answer with proper explanation.

Ans:

Yes, it appears that the topics Mr. Israfil designed for the Computer Architecture and Organization (CAO) course will give students a solid foundation in the field. Here's why:

Q1-1

1. Basic Components and Architecture:
   Foundation of computers systems.

2. Eight Ideas of computers Architecture:
   key design principles.

3. CPU Performance Analysis and numbers Represents
   : Crucial for system optimization.

4. Digital Logic Circuits : Includes essential
   components like multiplexers and flip-flops.

5. Pipelining Techniques: Performance optimization.

Justification:

Mr. Israfil's plan provides a solid foundation but lacks depth some areas. Adding more topic will better equip students to analyze, design and optimize computers system for future challenges.

Q2. How do you differentiate between Circuit-1 and Circuit-2? Give your answers with proper explanation based on the scenario.

Ans:

Circuit-1: It is combinational circuit.

Components: Multiplexers, De-Multiplexers, Encoders, Decoders, Half-Adders, Full-Addars.

Purpose: Used for data routing, arithmetic operation and encoding/decoding of signal.

Functionality: Focuses on manipulating input signals based on control signals to produce desired output.

Circuit-2: It is sequential circuit.

Components: Flip-Flops, Registers, counters

purpose: Used for storing, transferring and counting binary information

Q2.1

Functionality: Focuses on state retention, memory and sequential operations.

differences between Circuit-1 and Circuit-2:

Feature	Circuit-1	Circuit-2
Type of Circuit	Combinational Logic	Sequential Logic
Dependency	Output depends only on current input	Output depends on input and stored state.
use of memory	No memory elements	Includes memory elements.
Example Circuits	Basic arithmetic logic units (ALUs), multiplexers	Shift registers, binary counters, state machines

Q3. Why Computers use 2's complement in representing signed integers ? Briefly explain with example.

Ans:

Computers use 2's complement for signed integer representation due to its simplicity in hardware implentation, efficient arithmetic operation and ele elimination of ambiguity in representing zero.

Use 2's complement for signed integers because:

1. It uniquely represent zero.
2. Negative numbers are easy to generate. (invert bits, add 1)
3. The sign bit (MSB) is simple: 0=positive, 1= negative.

Example of 2's Complement:

let's take a 4-bit representation.

Positive number Representation:

$(+5)_{10} = (0101)_2$

Negative number Representation:

$(-5)_{10} = \{\emptyset 1010+1\}$

$= 1011$

-5 in 2's complement is 1011

Additional Example:

Adding +5 and -5 should give 0:

$0101 + 1011 = 0000$

This 2's complement effectively handles positive and negative arithmetic with same binary addition operation

Task 2:

Q4: How do the students convert 32-bits IEEE 754 Floating Point Representation? Calculation is needed based on the scenario.

Ans:

Last 2 digits of my students ID is - 08

So, number would be (0825.50)

Now let's finds out the binary of the number 0825.50

1st step:

$(0825)_{10} = (1100\ 1110\ 01)_2$

2|825 — 1
2|412 — 0
2|206 — 0
2|103 — 1
2|51 — 1
2|25 — 1
2|12 — 0
2|6 — 0
2|3 — 1
1

2nd step:

$0.50 \times 2 = 1.0$

$0.0 \times 2 = 0$

Therefore,

$(0825.50)_{10} = (1100\ 1110\ 01.1)_2$

$= (1.1001\ 1100\ 11 \times 2^9)_2$

3rd step:

Exponent

we know,

$E - 127 = n$

$\Rightarrow E - 127 = 9$

$\Rightarrow E = 9 + 127$

$= (136)_{10}$

$= (1000\ 1000)_2$

Q4-2

Step 4:

Fraction value:

0100 0100 0110 0111 0011 0000

Q5. Visualize the designed circuit (simplification is done k-map) that is made by Mr. Salman using different logic gates.

Ans:

Lionel Messi jersey number 10 and Mushfiqur Rahim jersey number is 15.

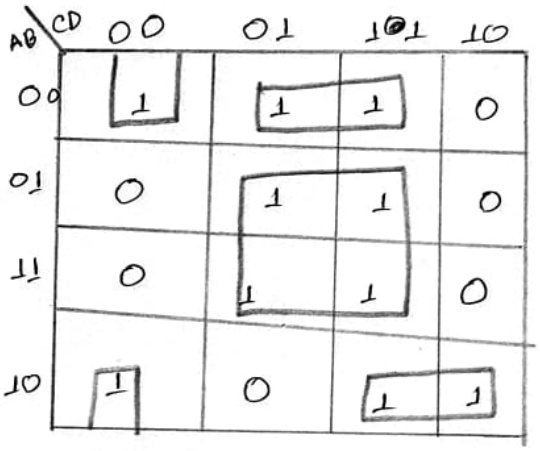
Therefore,

$F(A,B,C,D) = \Sigma(0,1,3,5,7,8,10,11,13,15)$

Number of variables = 4

$\therefore 2^n = 2^4 = 16$ cells.

Q5-1



We found 1 group and 3 pairs from here.

group 1:

A	B	C	D
0	1	0	1
0	1	1	1
1	1	0	1
1	1	1	1
	B		D

[Always unchanged items will be taken

Pair-1

A	B	C	D
0	0	0	0
1	0	0	0
	B'	C'	D'

Pair-2

A	B	C	D
0	0	0	1
0	0	1	1
A'	B'		D

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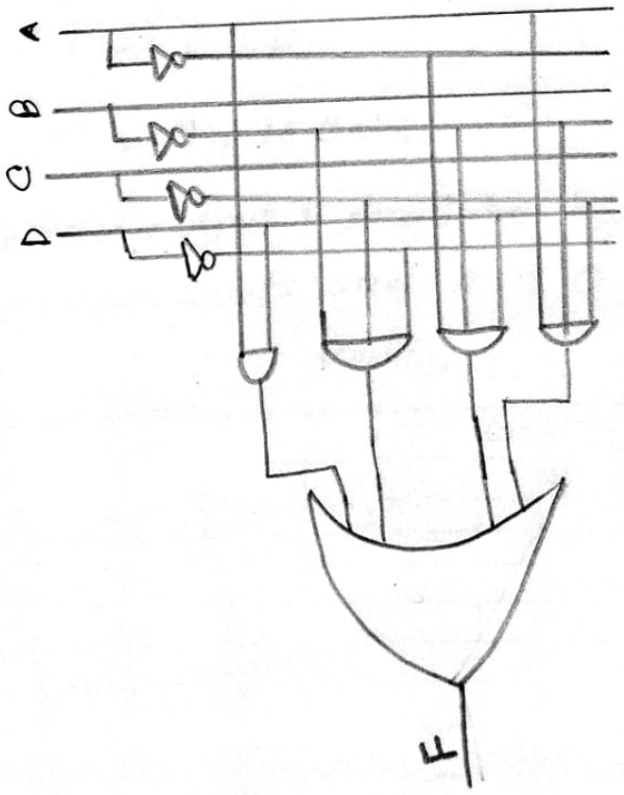
Part-3

A	B	C	D
1	0	1	1
1	0	1	0
A	B'	C'	

The simplified expression would be $F = BD + B'C'D' + A'B'D + ABC'$

Our Circuit Diagram would be,



Question-6:

Visualize the designed circuit (simplification is done by k-map) that is made by Mr. Abdullah using different logic gates.

Ans:

Given variables 4.

A (MSB), B, C, D

$\therefore 2^n = 2^4 = 16$ Cells.

Now The output F should be high(1) when A = 0 and 2 others inputs are also 0.
let's check our conditions.

A	B	C	D	condition(Y/N)	F
0	0	0	0	N(3 low's)	0
0	0	0	1	Y(2 low's)	1
0	0	1	0	Y(2 low's)	1
0	0	1	1	N(1 low)	0
0	1	0	0	Y(2 low's)	1
0	1	0	1	N(1 low's)	0
0	1	1	0	N(1 low's)	0
0	1	1	1	N(0 low's)	0
1	x	x	x	A=1 so F=0	0

Q6 - 1

Our K-map would be:

AB \ CD	00	01	11	10
00	0	1	0	1
01	1	0	0	0
11	0	0	0	0
10	0	0	0	0

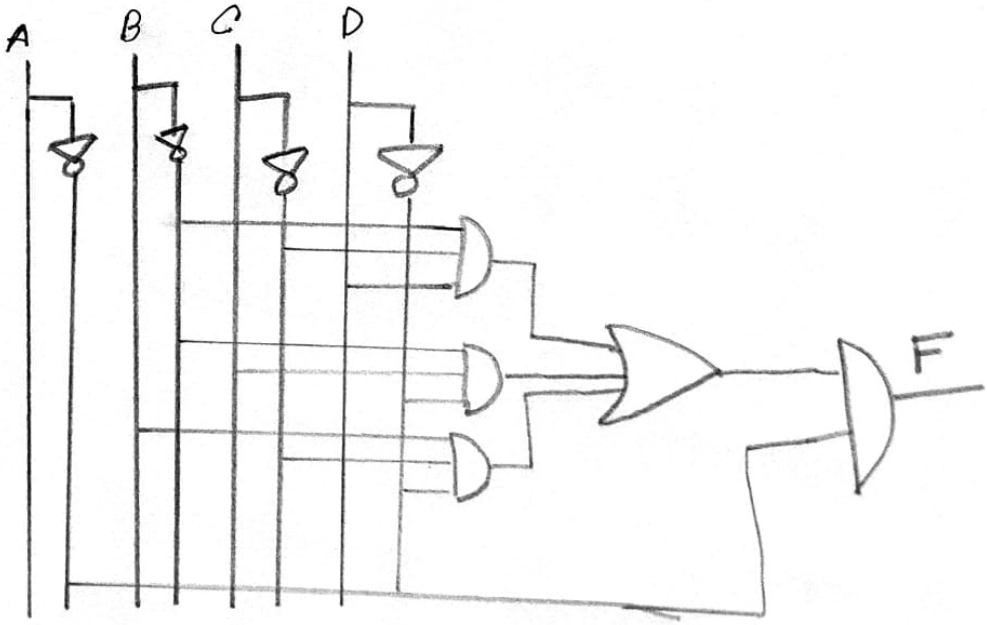
[only F=1 will be taken]

The resulting simplified expressions from the K-map would be:

$$F = (A'B'C'D + A'B'CD' + A'BC'D'$$

$$= A'(B'C'D + B'CD' + BC'D')$$

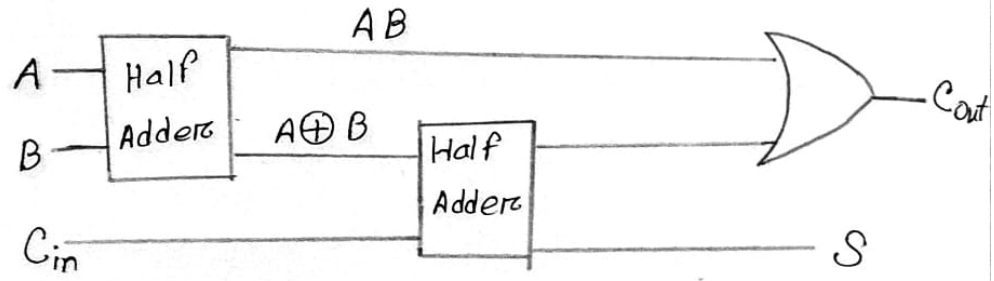
Our Circuit Diagram would be:



Q7: How Full Adder can be implement using Two Half Adders and OR Gate.

Ans:

Implementation of Full adder using 2 half adder:



1. First Half adder:

Input: A, B

Output: $S_1 = A \oplus B$, $C_1 = A \cdot B$

2. Second Half Adder:

Input: S_1, Cin

Output: $S = S_1 \oplus Cin$, $C_2 = S_1 \cdot Cin$

$Q_7 - 1$

3. OR Gate:

Input: C_1, C_2

Output: $C_1 + C_2$

Outputs:

Sum: $A \oplus B \oplus C_{in}$

Cout: $(A \cdot B) + (C_{in} \cdot (A \oplus B))$

Q8. What is the purpose of the last topic that Mr. Israfil will continue after Mid-term exam in computer architecture? Briefly describe with example.

Ans:

The last topic that Mr. Israfil will cover after the mid-term exam in the computer Architecture and Organization is "pipelining techniques."

Purpose of Pipeling Techniques:

Pipelining techniques used in the design of ~~mord~~ modern processors to improve their performance. It allows multiple instruction to be processed simultaneously by breaking down the execution pathway into distinct stages. Each stage completes a part of the

instruction, and different instructions can be in different stages of execution at the same time.

Example:

Consider a simple instruction pipeline with three stages:

1. Fetch 2. Decode 3. Execute.

consider two instruction:

1. Add (a, b) 2. Sub (C, D)

without pipelining:

Cycle	Instruction 1	Instruction 2
1	F	
2	D	
3	E	
4		F
5		D
6		E

with pipelining:

Cycle	stage1	stage2	stage 3
1	F_1		
2	F_2	D_1	
3		D_2	E_1
4			E_2

Significantly improving performance