
# Serial To Parallel

## Lecture (12)

# Serial to Parallel

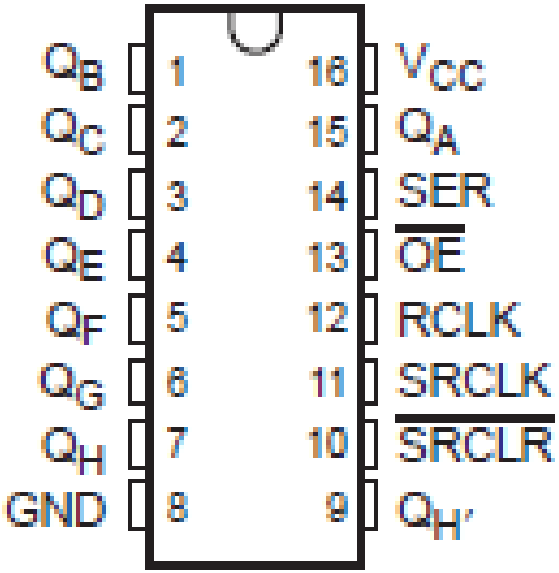
A serial to parallel converter is a digital circuit where we feed the input data serially, and read the outputs in parallel fashion.

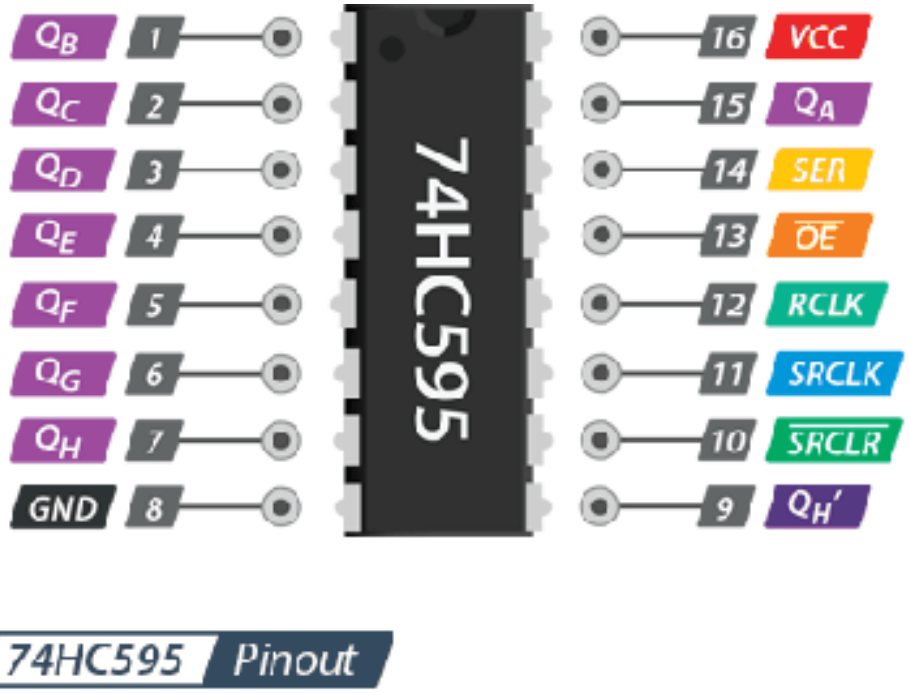
It is important to understand that the D-type flip-flop is a rising edge triggered device, and the data at its input transfers to the output only on the rising edge of the clock pulse.

The SN74HC595 devices contain an eight-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register.

# Serial to Parallel

## Shift Register SN74HC595-IC:

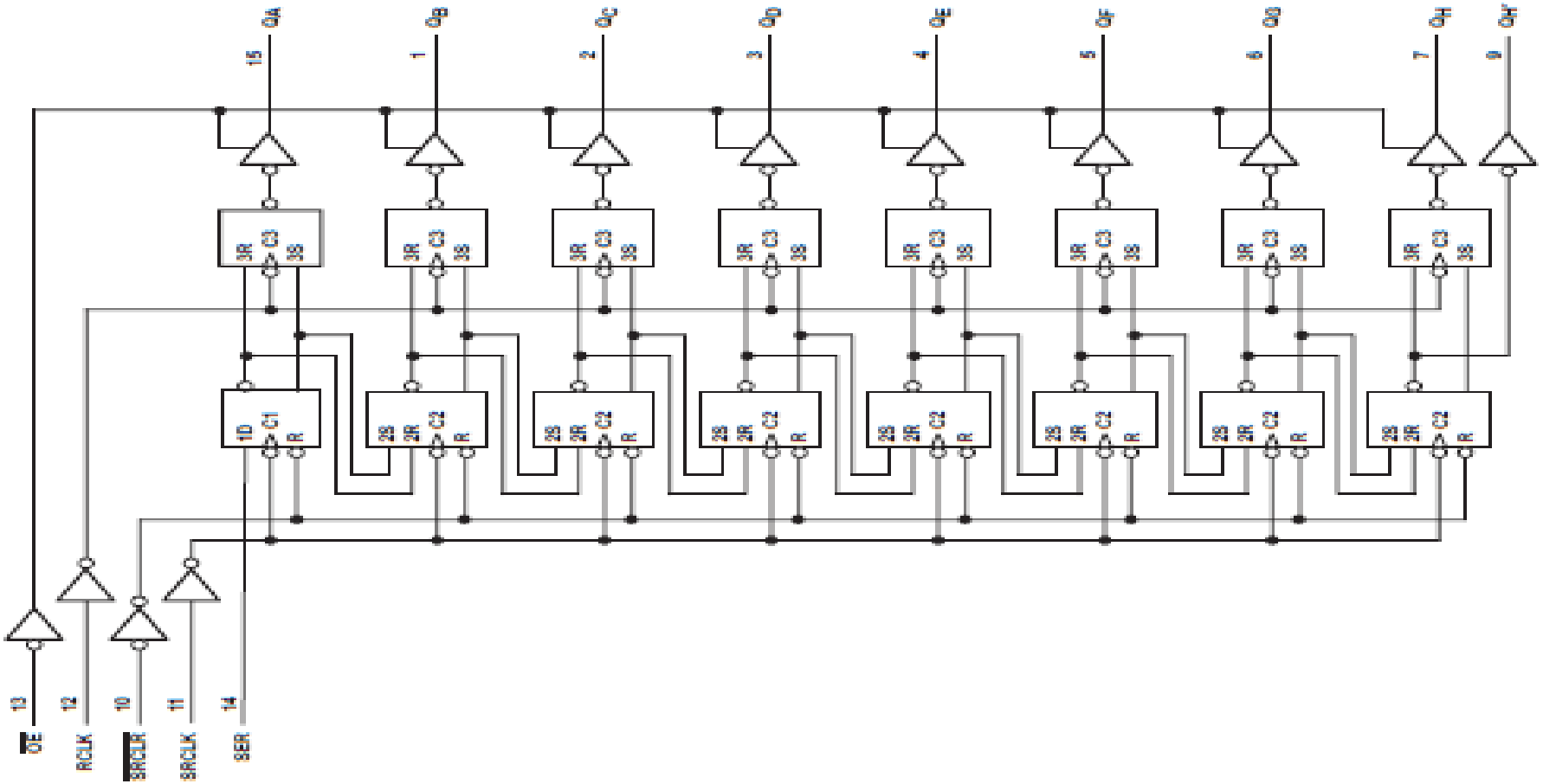



74HC595 Pinout

# Serial to Parallel

## Hardware Circuit of SN74HC595-IC:



# How SN74HC595 work?

**Pins of SN74HC595 is :**

| | |
|---|---|
| Input Pins | It mainly has three pins are responsible to serial input ( Data “SER_14”, Bit Latch “SRCLK_11” and Byte Latch “RCLK_14”). |
| Output Pins | It mainly has eight pins responsible to parallel output (Bit_0 “Qa_15”, Bit_1 “Qb_1”, Bit_2 “Qc_2”, Bit_3 “Qd_3”, Bit_4 “Qe_4”, Bit_5 “Qf_5”, Bit_6 “Qg_6” and Bit_7 “Qh_7”). |
| Serial Output | one pin responsible to serial output (Qh’_9). |
| Reset Pin | SRCLK_10 pin is called a reset clock and is an active low pin, its function is to reset the internal circuit and clear all of stored data if this pin is connected to low signal. |
| Enable Pin | OE_13 pin is called as an output enable pin, this pin is active low, so if you want the stored bits to appear on output pin, this pin must be connected to ground. |

# How SN74HC595 work?

**MSB First**

- Related to this method, the output will be sequentially from Qa_15 pin (which is the least significant bit) to Qh_7 (which is the most significant bit), so the arrangement of bits' Order will not affect

**LSB First**

- Related to the this method, the output will be reversely from Qa_15 pin (which is the least significant bit) to Qh_7 (which is the most significant bit), so the arrangement of bits' Order will be reversed

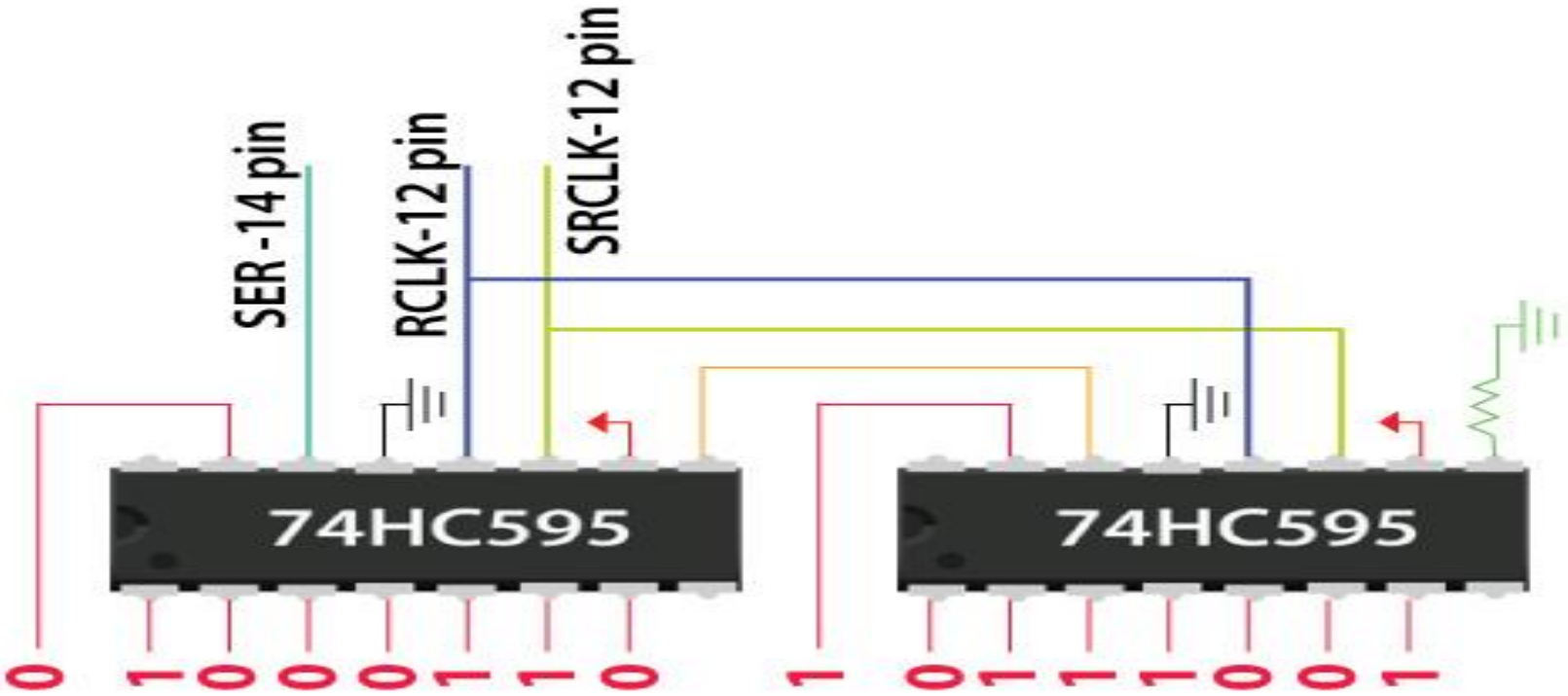
# How to make unlimited output pins?

Qh'_9 pin is used to leak the additional bits, so if you want to out more than one byte, as example, two bytes, you must gian two ICs to do it and the SRCLK_11 and RCLK_12 pins must be connected in parallel and the Qh'_9 pin of the first IC must be connected to the SER_14 pin of the second IC to stored the leaked data from the first IC to the Second.

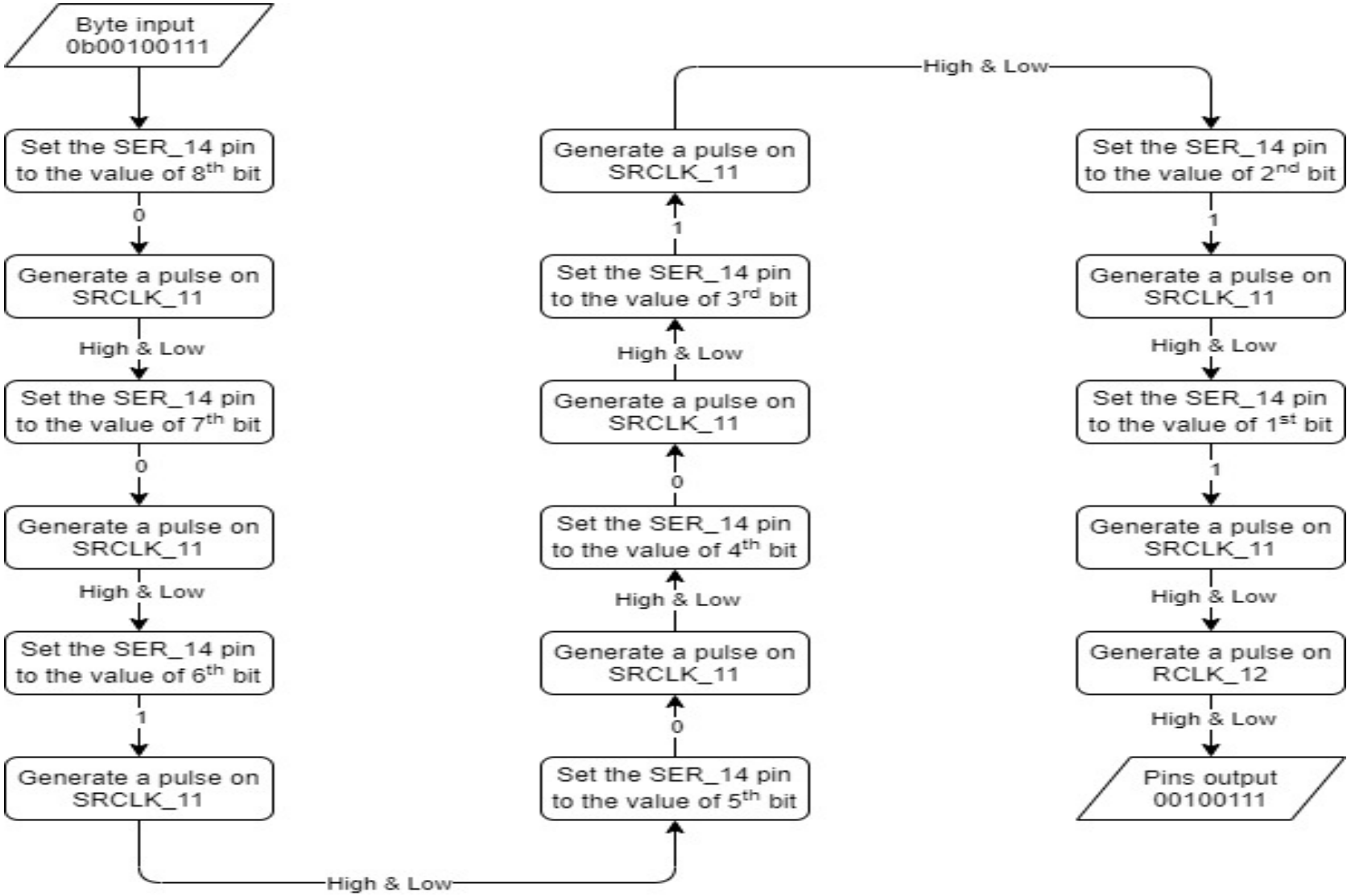
MSB order method is preferred in this case because this method doesn't affect the order arrangement of bits to be more logical and the least byte appears on the first and the highest byte on the second.

# How to make unlimited output pins?

- **Assume that the sent data is “0b1001110101100010”**
  **The output will be:**



# Shift Register Coding Diagram



# Time To Code

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