Embedded Systems Interfacing

Lecture one

Digital Input Output Part 1

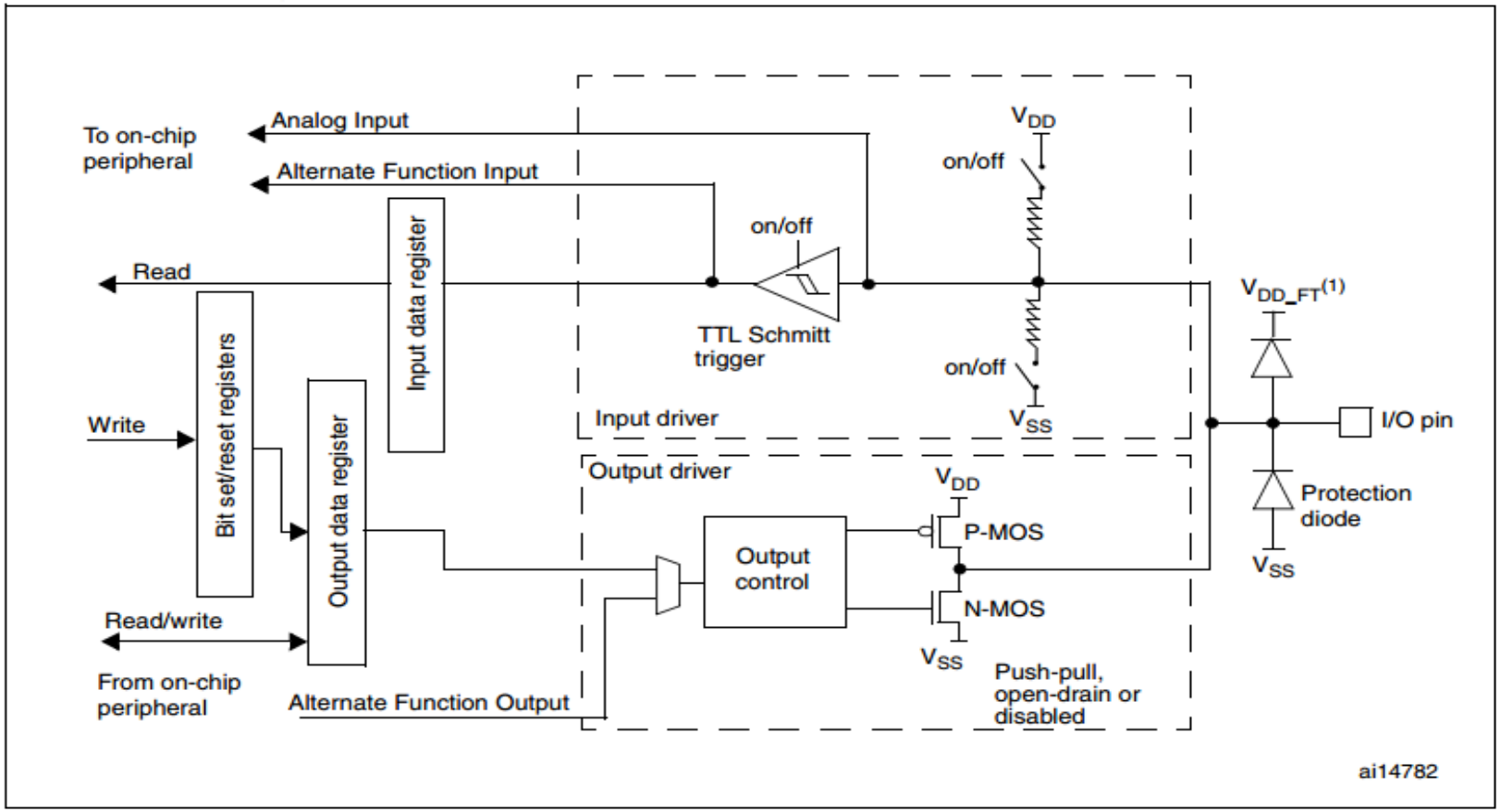
GPIO

the general-purpose I/O ports(GPIO), is a pin on an IC (Integrated Circuit). It can be used for driving loads, reading digital and analog signals, controlling external components, generating triggers for external devices etc. Each of the general-purpose I/O ports has two 32-bit configuration registers, two 32-bit data registers, a 32-bit set/reset register , a 16-bit reset register and a 32-bit locking register.

Each port bit of GPIOs can be individually configured by software in several modes:

- **Input floating.**
- **Input pull-up.**
- **Input-pull-down.**
- **Analog.**
- **Output open-drain.**
- **Output push-pull.**
- **Alternate function push-pull.**
- **Alternate function open-drain.**

GPIO Block Diagram



GPIO Registers

Port configuration register low (GPIOx_CRL) (x=A..G)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF7[1:0]		MODE7[1:0]		CNF6[1:0]		MODE6[1:0]		CNF5[1:0]		MODE5[1:0]		CNF4[1:0]		MODE4[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNF3[1:0]		MODE3[1:0]		CNF2[1:0]		MODE2[1:0]		CNF1[1:0]		MODE1[1:0]		CNF0[1:0]		MODE0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Port configuration register high (GPIOx_CRH) (x=A..G)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF15[1:0]		MODE15[1:0]		CNF14[1:0]		MODE14[1:0]		CNF13[1:0]		MODE13[1:0]		CNF12[1:0]		MODE12[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNF11[1:0]		MODE11[1:0]		CNF10[1:0]		MODE10[1:0]		CNF9[1:0]		MODE9[1:0]		CNF8[1:0]		MODE8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO Registers

Each port has 16 pin and each pin has 4 bits to select it's direction. we have (4*16) bits to each port, these 64 bits are divided into two halfs:

- Configuration register low (CRL) that control the direction of the first 8 bits(form bit 0 to bit 7).
- Configuration register high (CRH) that control the direction of the high bits (form bit 8 to bit 15).

3	2	1	0
CNF0[1:0]		MODE0[1:0]	
rw	rw	rw	rw

MODEy[1:0]:

These bits are written by software to select the mode

- **00: Input mode (reset state)**
- **01: Output mode, max speed 10 MHz.**
- **10: Output mode, max speed 2 MHz.**
- **11: Output mode, max speed 50 MHz.**

GPIO Registers

3	2	1	0
CNF0[1:0]		MODE0[1:0]	
rw	rw	rw	rw

CNFy[1:0]:

1- In input mode (MODE[1:0]=00):

- **00: Analog mode**
- **01: Floating input (reset state)**
- **10: Input with pull-up / pull-down**
- **11: Reserved**

2- In output mode (MODE[1:0] > 00):

- **00: General purpose output push-pull**
- **01: General purpose output Open-drain**
- **10: Alternate function output Push-pull**
- **11: Alternate function output Open-drain**

GPIO Registers

Port input data register (GPIOx_IDR) (x=A..G)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

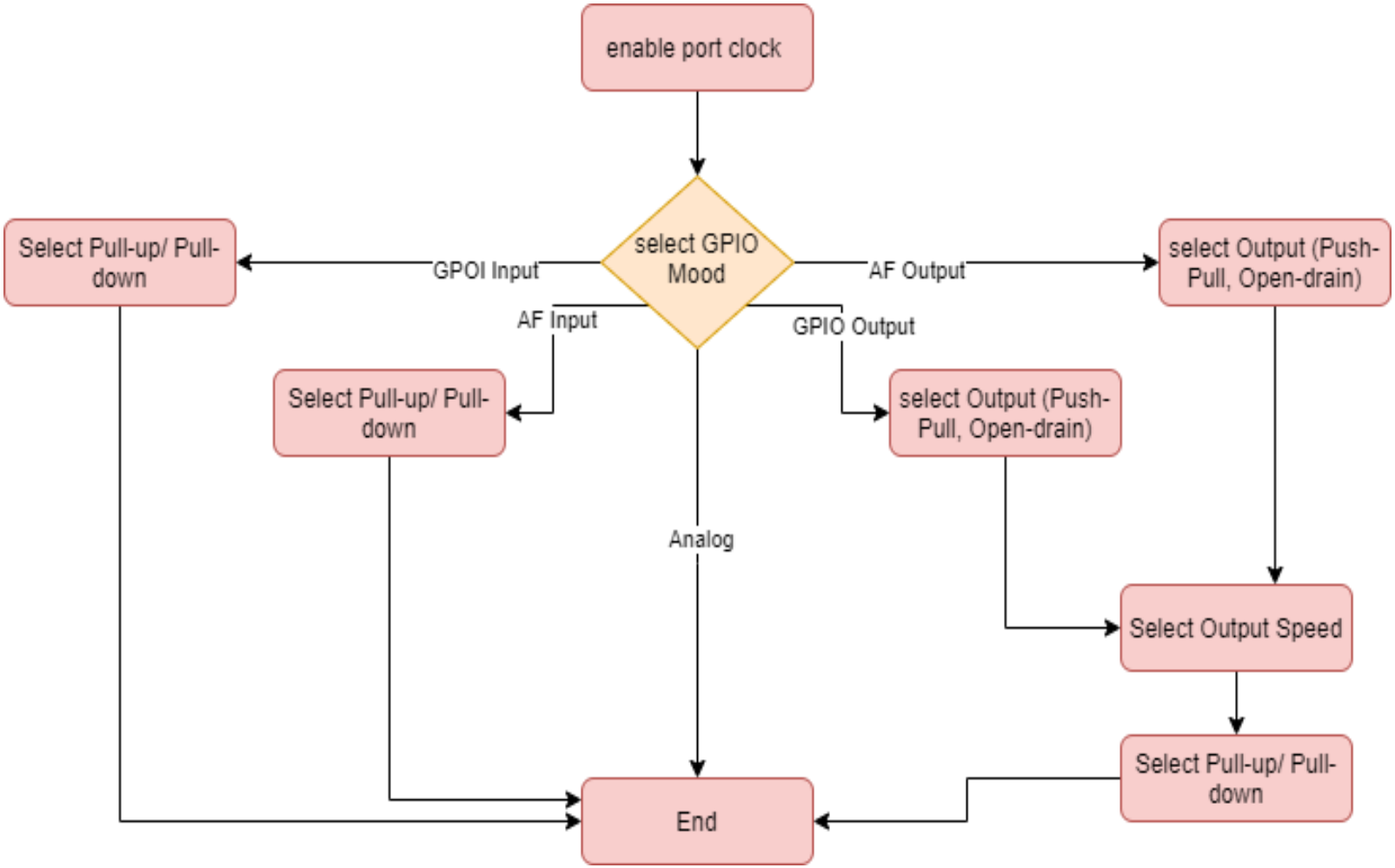
These bits are read only and can be accessed in Word mode only. They contain the input value of the corresponding I/O port.

Port output data register (GPIOx_ODR) (x=A..G)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

These bits can be read and written by software and can be accessed in Word mode only.

GPIO Flowchart



The End …

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