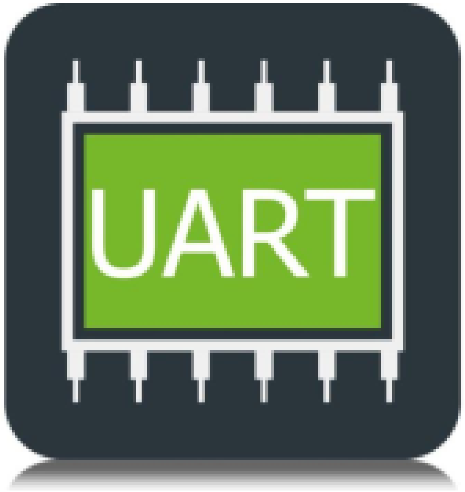
Embedded Systems Interfacing

Lecture one

Digital Input Output Part 1

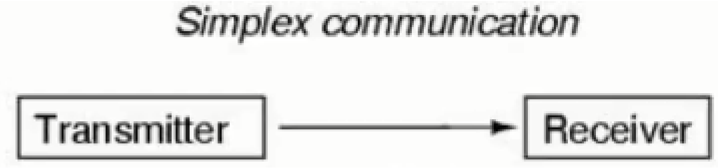
USART Communication

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The USART offers a very wide range of baud rates using a fractional baud rate generator. It supports synchronous one-way communication and half-duplex single wire communication. It allows multiprocessor communication. High speed data communication is possible by using the DMA for multibuffer configuration.

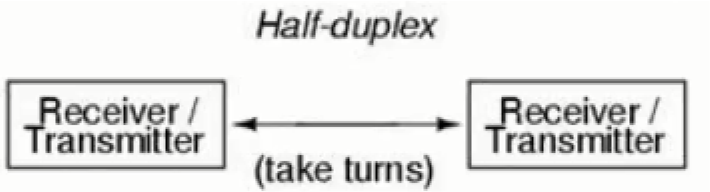


Duplex Communication

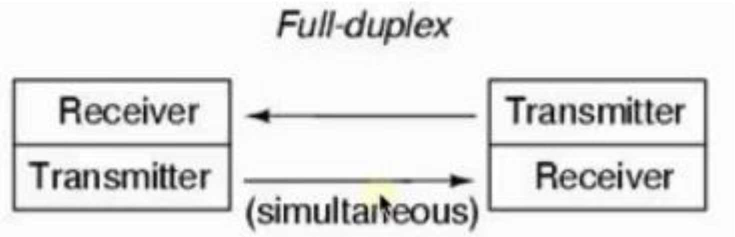
Simplex : - In which one device transmits and the others can only “listen”, ex. ***Radio***



Half Duplex: - In which both parties can communicate with each other, but not simultaneously, the communication is one direction at a time. Ex **walkie-talkie**

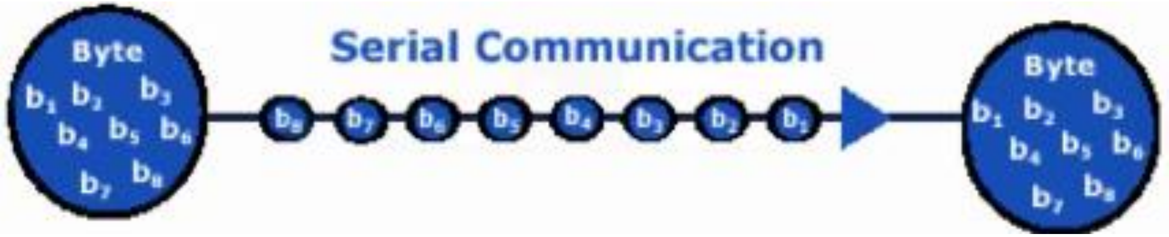


Full Duplex: - In which both parties can communicate with each other simultaneously. Ex **telephone**

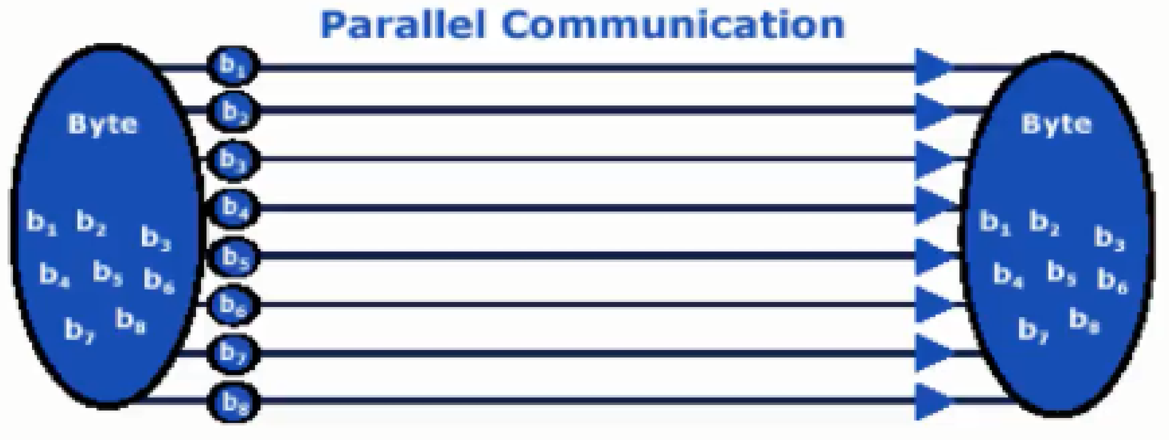


Serial VS Parallel Communication

Serial Communication :- Process of sending data one bit at a time, sequentially, over a communication channel or computer bus.

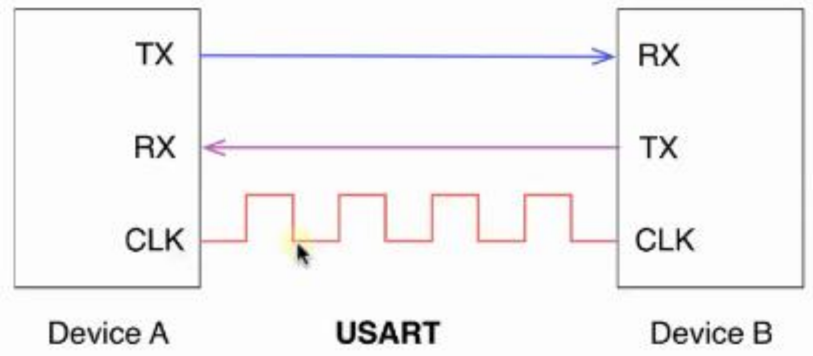

Serial Communication
Byte
b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8
b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1
Byte
b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8

Parallel Communication :- Process of sending several bits at as a whole, on a link with several parallel channels.

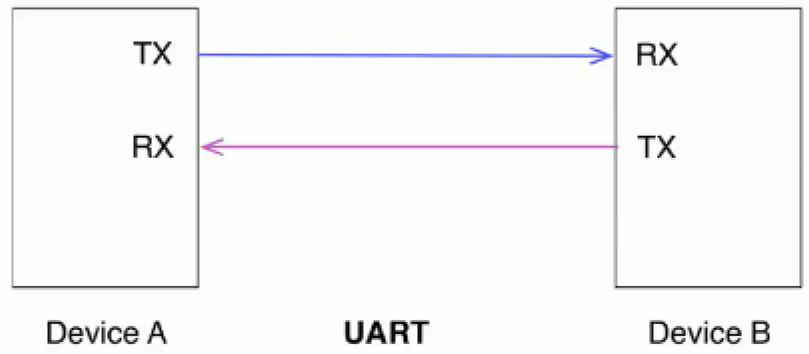

Parallel Communication
Byte
b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8
b_1
b_2
b_3
b_4
b_5
b_6
b_7
b_8
Byte
b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8

Synchronous VS Asynchronous Communication

Synchronous :- Synchronous transmission in which data is sent in a continuous stream at a constant rate.



Asynchronous :- Asynchronous transmission of data, generally without the use of an external clock signal, where data can be transmitted intermittently rather than in a steady stream.



USART Transmitter

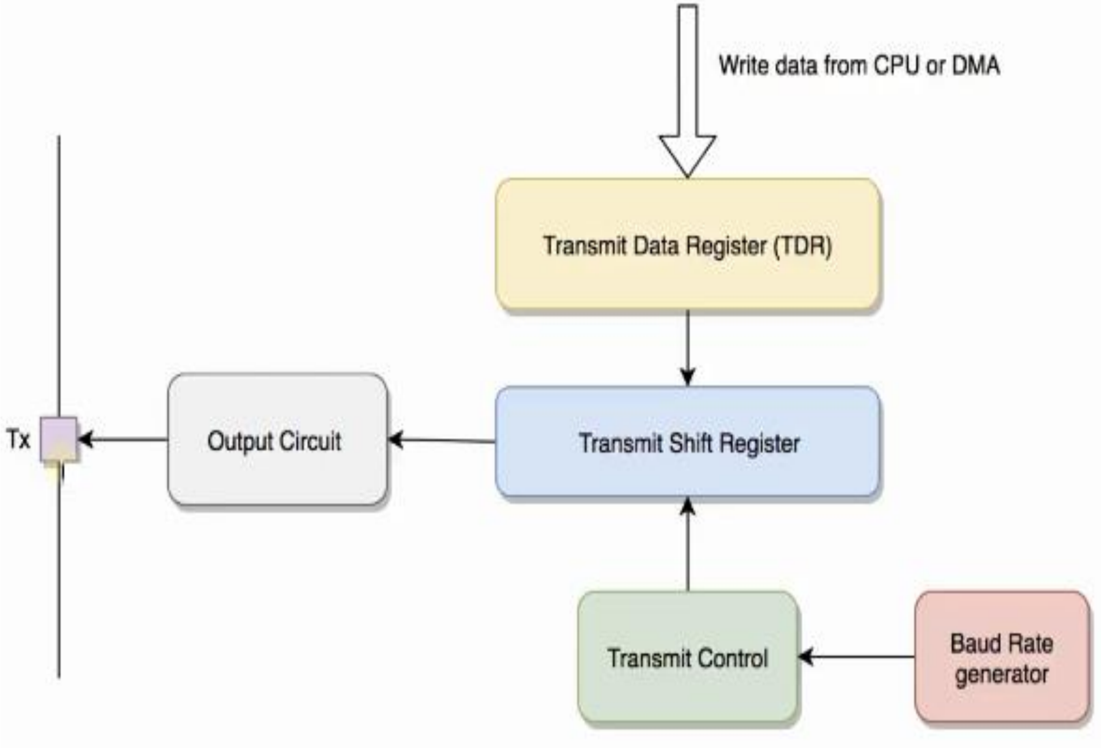
-During a USART transmission, data shifts out least significant bit first on the TX pin. In this mode, the USART_DR register consists of a buffer (TDR) between the internal bus and the transmit shift register .

-Every character is preceded by a start bit, which is a logic level low for one bit period.
The character is terminated by a configurable number of stop bits.

-The following stop bits are supported by USART: 0.5, 1, 1.5 and 2 stop bits.

-The TE bit should not be reset during transmission of data. Resetting the TE bit during the transmission will corrupt the data on the TX pin as the baud rate counters will get frozen.

-The current data being transmitted will be lost. An idle frame will be sent after the TE bit is enabled.



Transmission Configuration Workflow

1. Enable the USART by writing the UE bit in USART_CR1 register to 1.

2. Program the M bit in USART_CR1 to define the word length.

3. Program the number of stop bits in USART_CR2.

4. Select DMA enable (DMAT) in USART_CR3 if Multi buffer Communication is to take place. Configure the DMA register as explained in multibuffer communication.

5. Select the desired baud rate using the USART_BRR register.

6. Set the TE bit in USART_CR1 to send an idle frame as first transmission.

7. Write the data to send in the USART_DR register (this clears the TXE bit). Repeat this for each data to be transmitted in case of single buffer.

8. After writing the last data into the USART_DR register, wait until TC=1. This indicates that the transmission of the last frame is complete. This is required for instance when the USART is disabled or enters the Halt mode to avoid corrupting the last transmission

Single byte Communication

The TXE bit is always cleared by a write to the data register.
The TXE bit is set by hardware and it indicates:

The data has been moved from TDR to the shift register and the data transmission has started. The TDR register is empty.

The next data can be written in the USART_DR register without overwriting the previous data. This flag generates an interrupt if the TXEIE bit is set.

When a transmission is taking place, a write instruction to the USART_DR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the USART_DR register places the data directly in the shift register, the data transmission starts, and the TXE bit is immediately set.

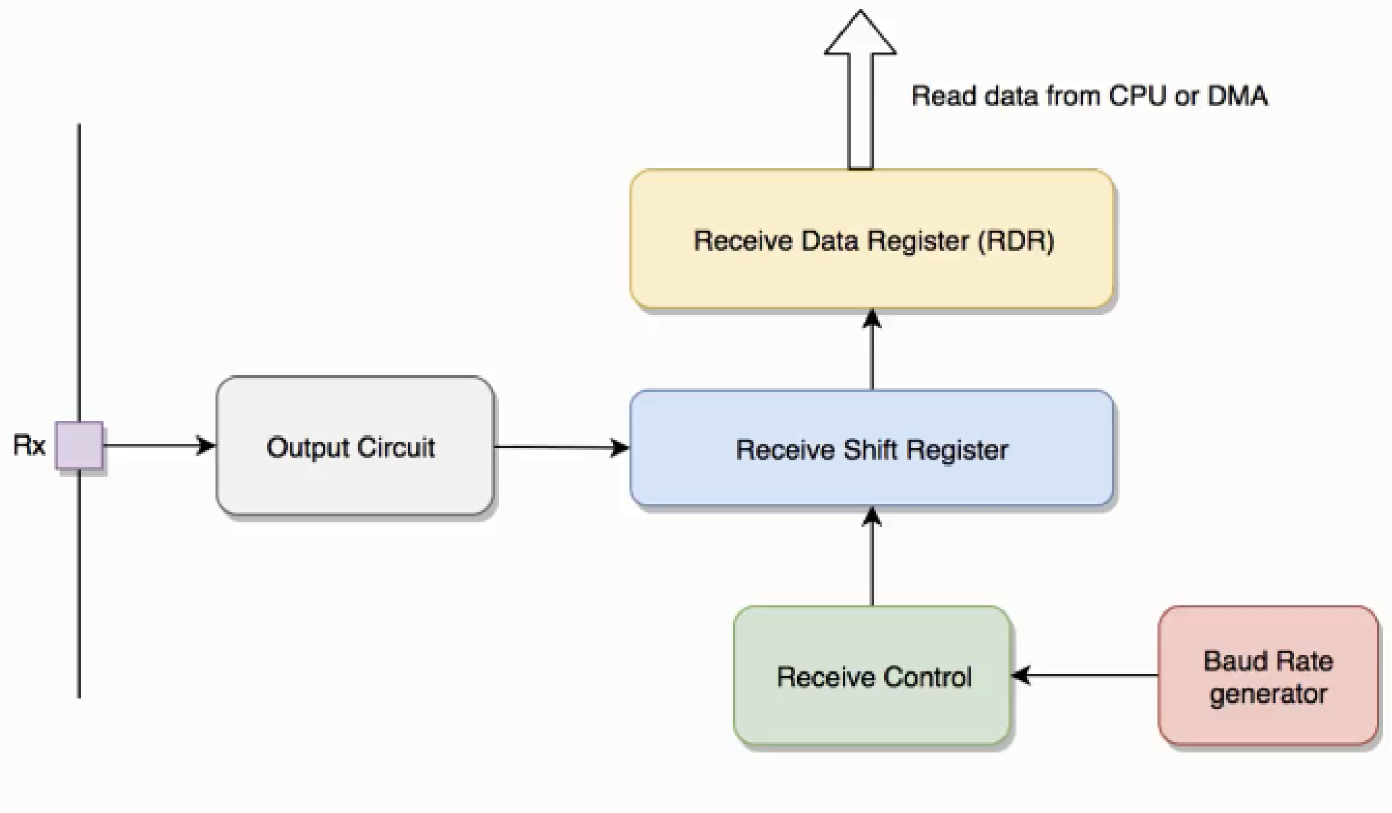
If a frame is transmitted (after the stop bit) and the TXE bit is set, the TC bit goes high. An interrupt is generated if the TCIE bit is set in the USART_CR1 register.

After writing the last data into the USART_DR register, it is mandatory to wait for TC=1 before disabling the USART or causing the microcontroller to enter the low-power mode.

The TC bit is cleared by the following software sequence:
1. A read from the USART_SR register
2. A write to the USART_DR register

USART Receiver

During a USART reception, data shifts in least significant bit first through the RX pin.
In this mode, the USART_DR register consists of a buffer (RDR) between the internal bus and the received shift register



When Character is Received

The RXNE bit is set. It indicates that the content of the shift register is transferred to the RDR. In other words, data has been received and can be read .

An interrupt is generated if the RXNEIE bit is set.

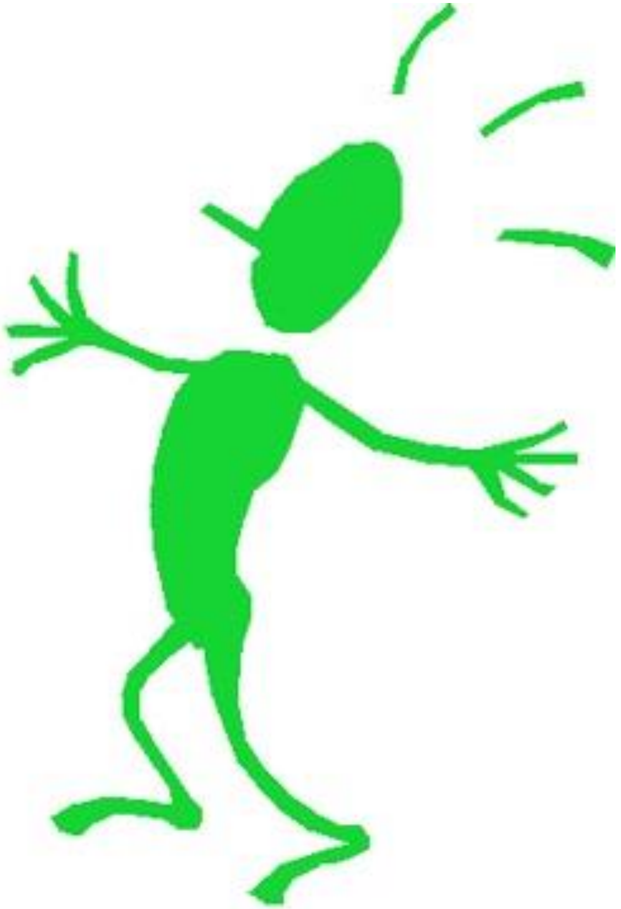
The error flags can be set if a frame error, noise or an overrun error has been detected during reception.

In multibuffer, RXNE is set after every byte received and is cleared by the DMA read to the Data Register.

In single buffer mode, clearing the RXNE bit is performed by a software read to the USART_DR register. The RXNE flag can also be cleared by writing a zero to it. The RXNE bit must be cleared before the end of the reception of the next character to avoid an overrun error.

The End ...

Any questions ...?



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