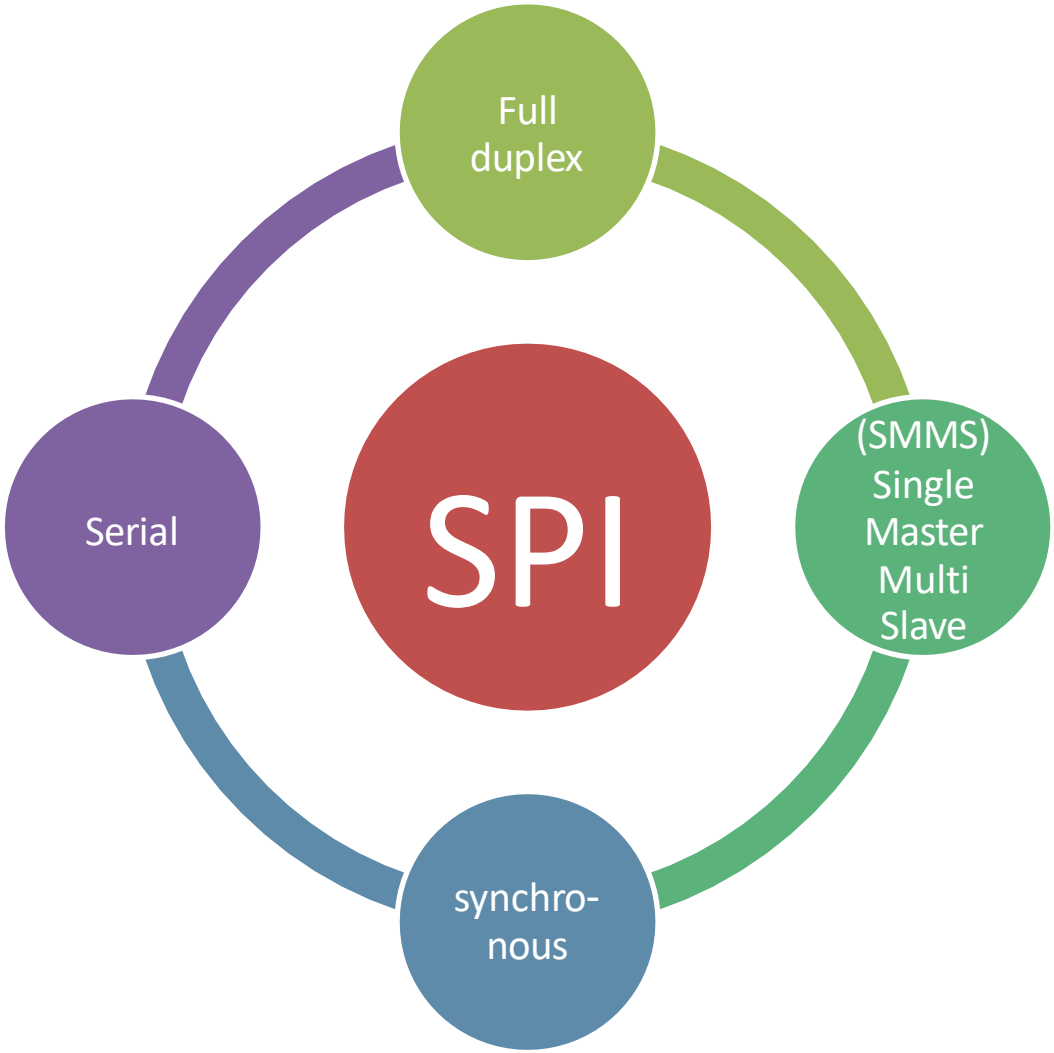
Embedded Systems Interfacing

Lecture Fourteen

SPI Serial Communication

SPI features



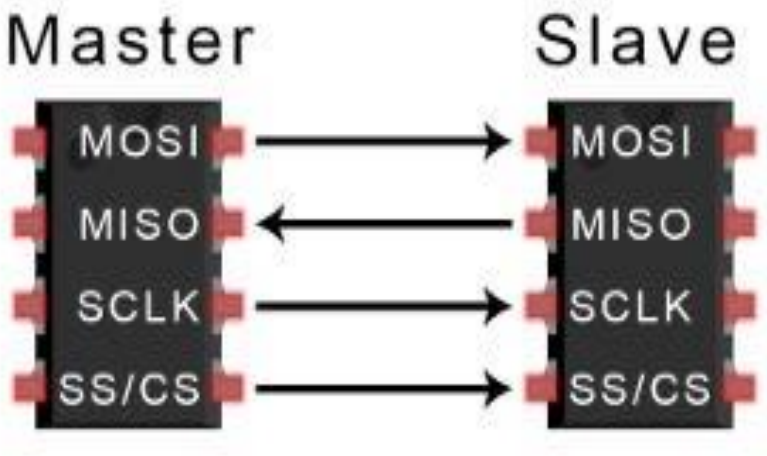
SPI concept

What is SPI?

•Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication.
• The SPI bus can operate with a single master device and with one or more slave devices.

SPI connections :

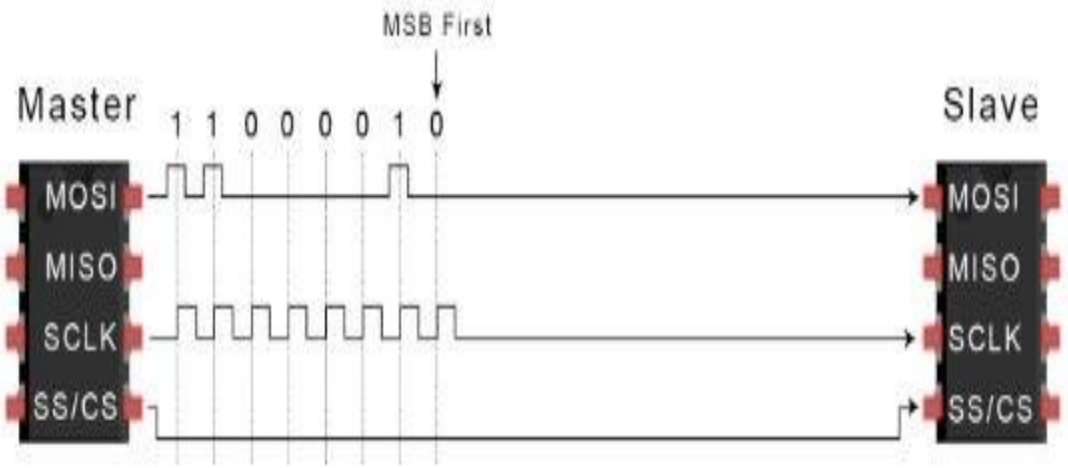
•SCLK : Serial Clock (output from master).
•MOSI : Master Output, Slave Input (output from master).
• MISO : Master Input, Slave Output (output from slave).
•SS : Slave Select (active low, output from master).



SPI concept

STEPS OF SPI DATA TRANSMISSION

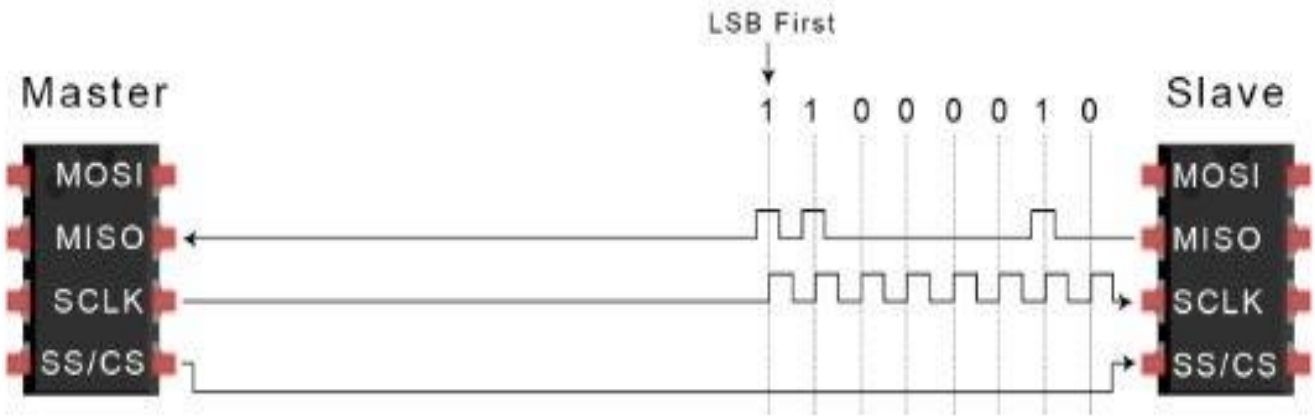
3. The master sends the data one bit at a time to the slave along the MOSI line. The slave reads the bits as they are received::



SPI concept

STEPS OF SPI DATA TRANSMISSION

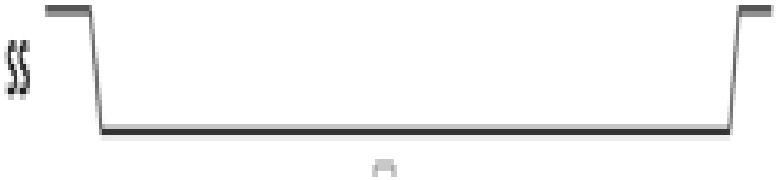
4. If a response is needed, the slave returns data one bit at a time to the master along the MISO line. The master reads the bits as they are received:



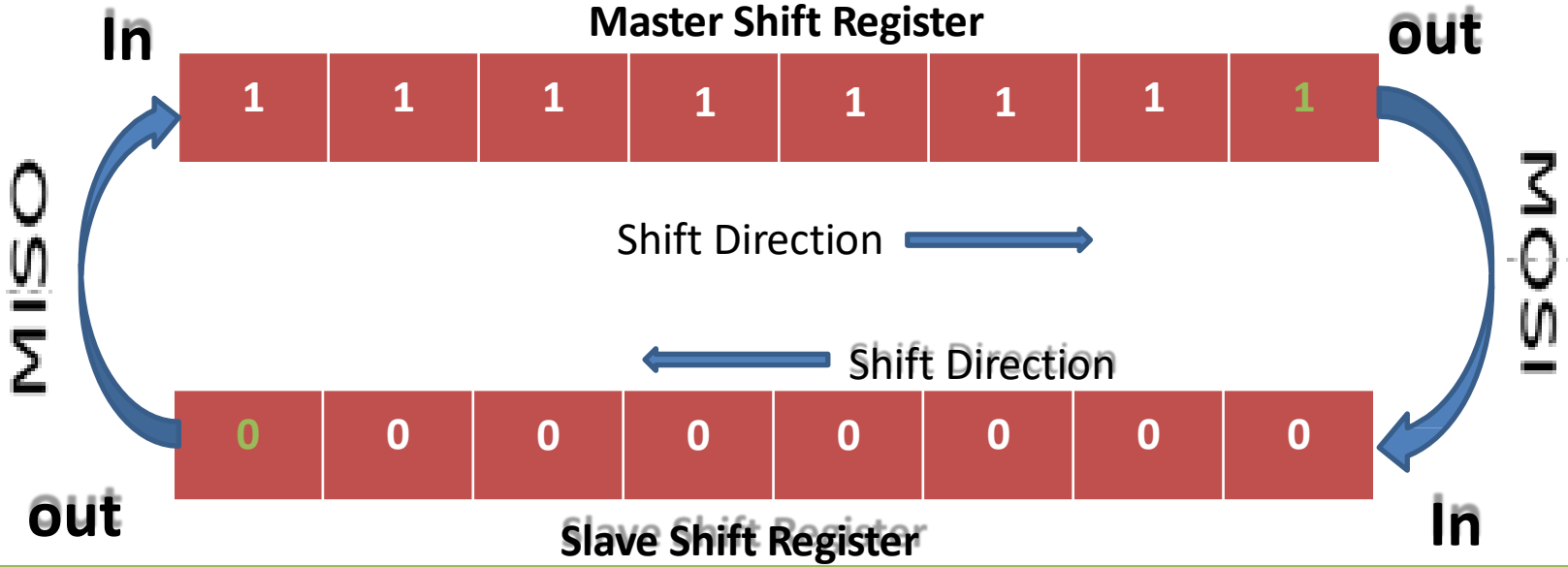
SPI concept

THE INTERCONNECTION BETWEEN MASTER AND SLAVE

The SPI Master initiates the communication cycle when pulling low the Slave Select SS pin of the desired Slave.



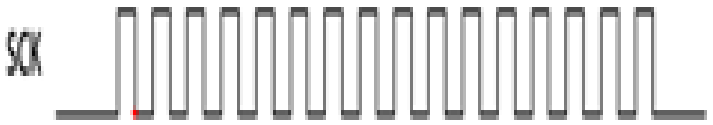
Master and Slave prepare the data to be sent in their respective Shift Registers.



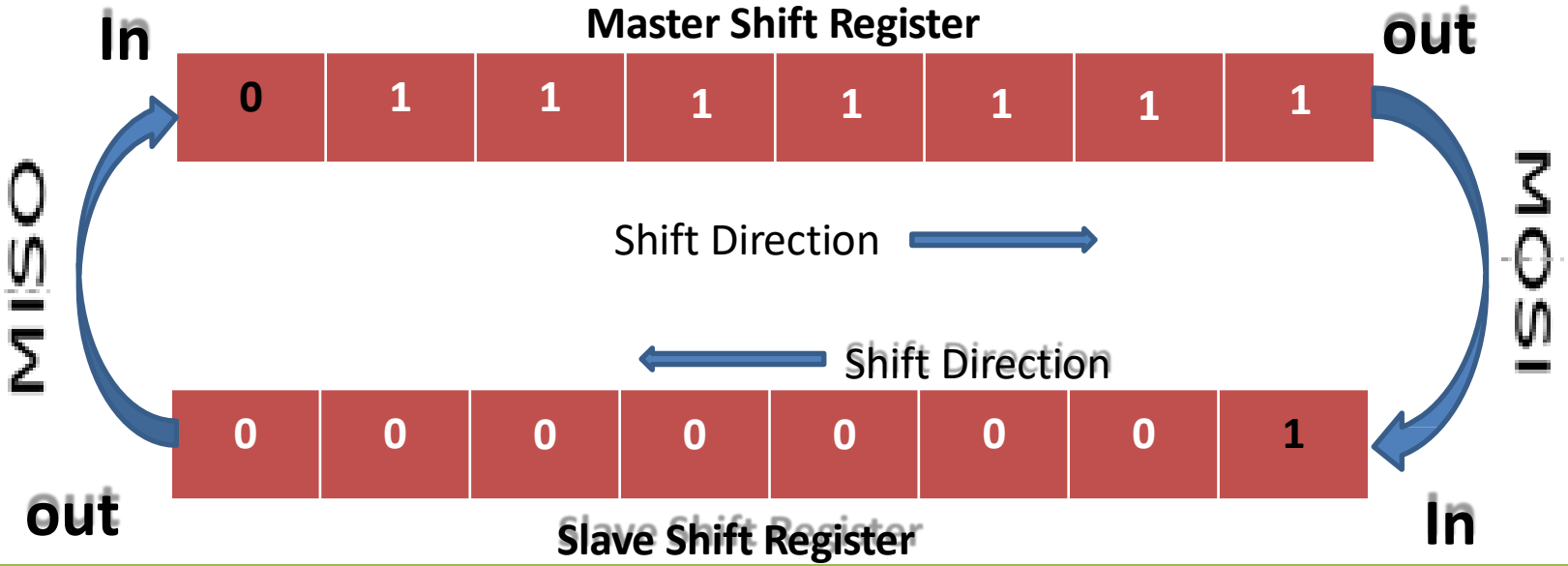
SPI concept

SPI DATA TRANSMISSION AND RECEIVE

the Master generates the required clock pulses on the SCK line to interchange data.



Data is always shifted from Master to Slave on MOSI, line, and from Slave to Master on MISO, line.



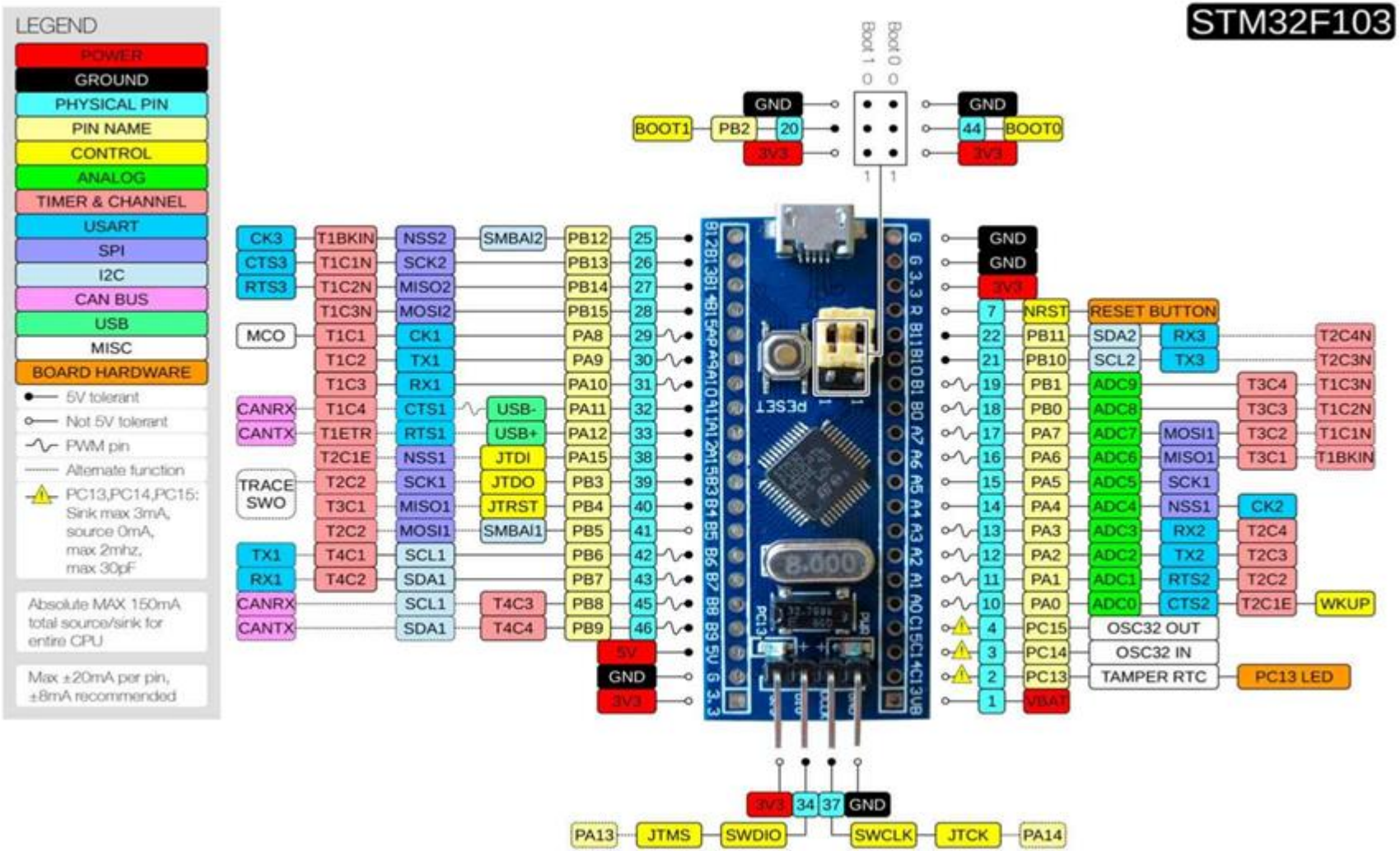
SPI on STM32F103

STM32F103 supports two SPI peripherals (SPI_1, SPI_2).
SPI in stm32f104 supports some new features, some of these features are standard and the others are not standard.

Features:

- It supports multi masters multi slaves (Not standard).
- It supports automatic control for NSS in master mode.
- It supports an optional CRC check (Not Standard).
- It supports DMA.

SPI on STM32F103



SPI on STM32F103

SPI Register Description:

The base address of SPI-one is (0x40013000).

The base address of SPI-two is (0x40003800).

A-**SPI_CR1** (SPI Control Register 1):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDI MODE	BIDI OE	CRC EN	CRC NEXT	DFF	RX ONLY	SSM	SSI	*LSB FIRST*	SPE	BR [2:0]			MSTR	CPOL	CPHA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- CPHA «Clock Phase» = 1 → «Write then Read»
- CPOL «Clock Polarity»= 0 → «idle clock will be “High”»
- MSTR «Master Mode» → « 0 for Slave – 1 for Master»
- BR «Baud Rate» = 001 → «for being Fperi/4»
- SPE «SPI Enable» = 1 → «Enabling SPI»
- LSB First → « 1 for LSB first – 0 for MSB first»

SPI Register Description:

The base address of SPI-one is (0x40013000).

The base address of SPI-two is (0x40003800).

A-**SPI_CR1** (SPI Control Register 1):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDI MODE	BIDI OE	CRC EN	CRC NEXT	DFF	RX ONLY	SSM	SSI	*LSB FIRST*	SPE	BR [2:0]			MSTR	CPOL	CPHA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- SSI «Internal Slave Select»= 1 → «NSS Pin is cut for Master Mode»
- SSM «Slave Selection Management»= 1 → «Enabled»
- RX «Receive only»= 0 → « Transmiting and receiving»
- DFF «Data Frame Format» → «1 for two bytes – 0 for one byte»
- CRC Next «CRC Transfer next» = 0 → «Sending Data»
- CRC EN «CRC Enable» = 0 → «Disabling CRC Mode»

SPI Register Description:

The base address of SPI-one is (0x40013000).

The base address of SPI-two is (0x40003800).

A-**SPI_CR1** (SPI Control Register 1):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDI MODE	BIDI OE	CRC EN	CRC NEXT	DFF	RX ONLY	SSM	SSI	*LSB FIRST*	SPE	BR [2:0]			MSTR	CPOL	CPHA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- BIDIOE, BIDIMODE «Bidirectional Mode»:

  These bits control if SPI is unidirectional or bidirectional mode

  These bits will be «00» to work as a unidirectional

SPI Register Description:

The base address of SPI-one is (0x40013000).

The base address of SPI-two is (0x40003800).

B-**SPI_CR2** (SPI Control Register 2):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TXEIE	RXNEIE	ERRIE	Res.	Res.	*SSOE*	TXDMAEN	RXDMAEN
								rw	rw	rw			rw	rw	rw

This register is used to enable any Interrupt Mode.

SPI Register Description:

The base address of SPI-one is (0x40013000).

The base address of SPI-two is (0x40003800).

C-**SPI_SR** (SPI Status Register):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BSY	OVR	MODF	CRC ERR	UDR	CHSID E	TXE	RXNE
								r	r	r	rc_w0	r	r	r	r

This register is used to write the data will be sent

or

read the data which is received.

SPI Register Description:

The base address of SPI-one is (0x40013000).

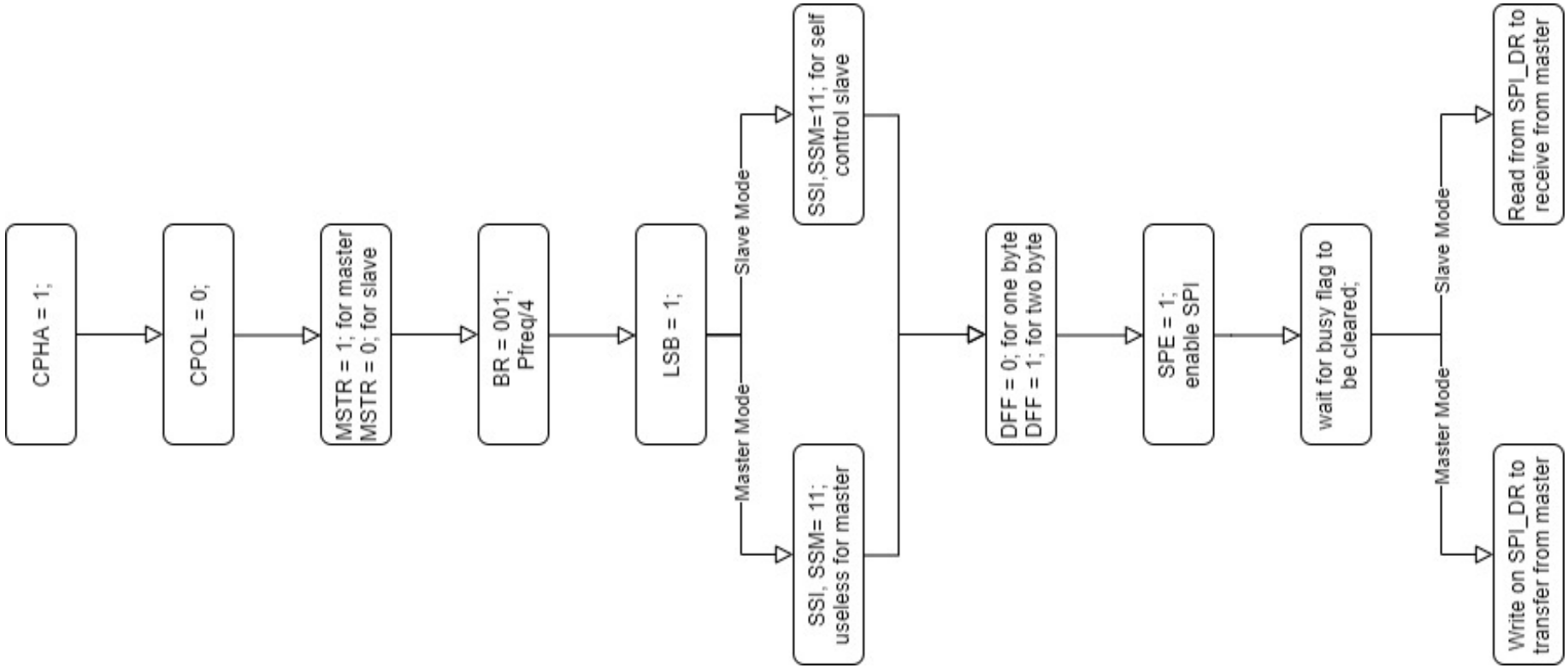
The base address of SPI-two is (0x40003800).

D-**SPI_DR** (SPI Data Register):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

This register is used to check any flag, specially BSY flag which is used at polling mode.

SPI Coding Diagram:



Time To Code

The End …

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