Embedded Systems Concepts

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Computing System Definition

A device capable for performing mathematical and logical operations in accordance with a predetermined set of instructions.

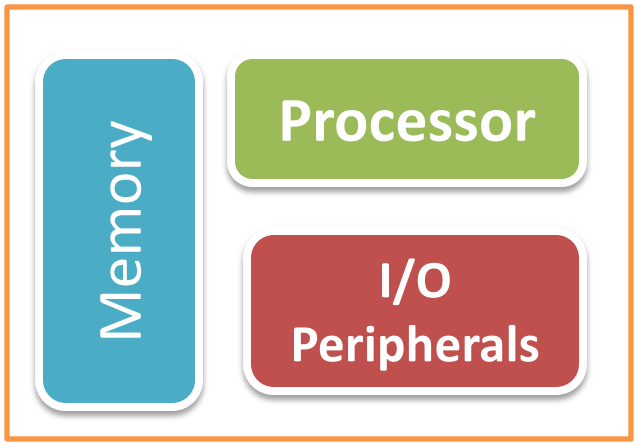
Computing System Components

Any computing system consists of 3 main components:

1- **Processor** which is responsible for performing the instructions.

2- **Memory** which is responsible for storing the program

3- **Input / Output peripherals** for interacting with the user.



Embedded System Definition

Embedded system is a computing system with limited resources (Processor, Memory and I/O) used for performing a specific task.

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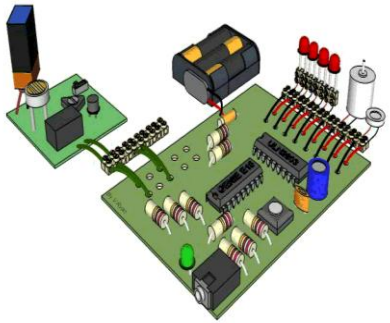
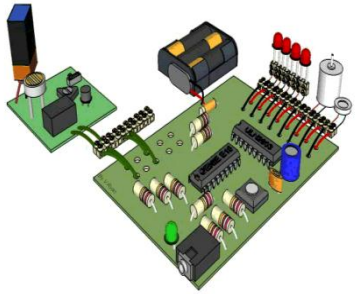


Personal Computer Vs. **Embedded System**



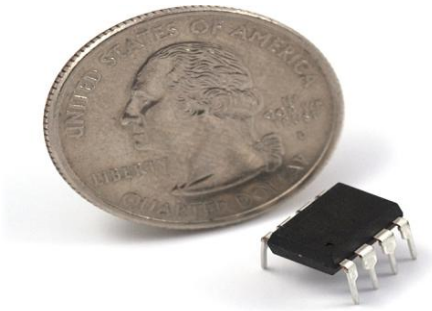
Computer is for general purpose use and with huge resources

Embedded system is for specific purpose and with limited resources

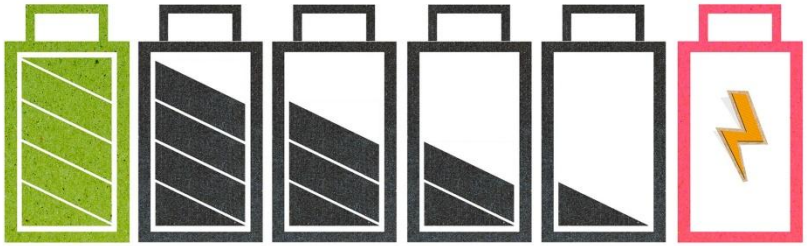
Embedded Systems Challenges

1- Performance

2- Size

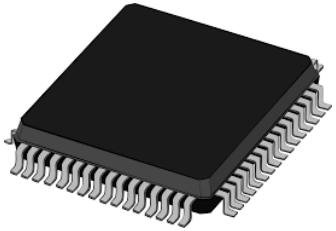


3- Power Consumption



4- Cost

ES Implementation Techniques

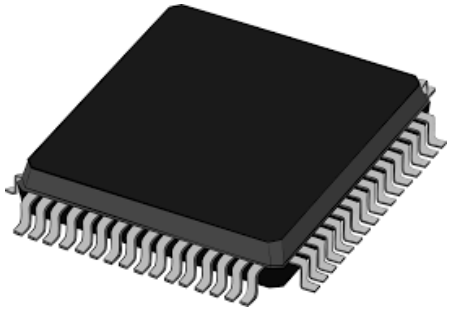
	System on Board SB	System on Chip SOC
		
performance	——	——
size	High	Low
cost	High	Low
Power consumption	High	Low
configurability	Easy	NA

When To use … ?

System Board

For Development and Design phase

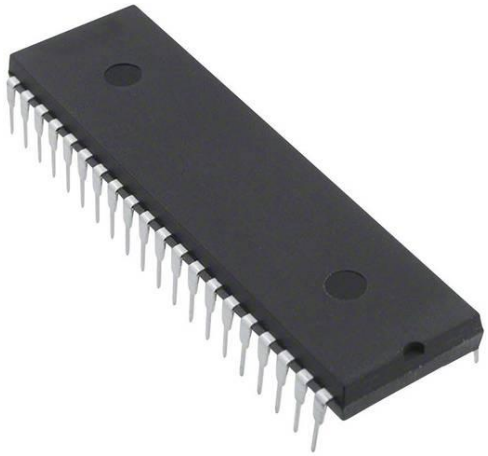
System On Chip



For Production after Design

Microcontroller Definition

The microcontroller is a system on chip consists of processor, memory and I/O peripherals. So, it looks like an IC but inside it has all the needed elements to make an ES and ready for programming.



Microcontroller Vs. Microprocessor

Microcontroller -> is a system on chip, contains processor, memory and I/O.

Microprocessor -> is one element from the needed 3 elements to make ES. So it needs memory and I/O.

Question …

What is the difference between the following:

1- Processor
2- Microprocessor
3- Central Processing Unit (CPU)

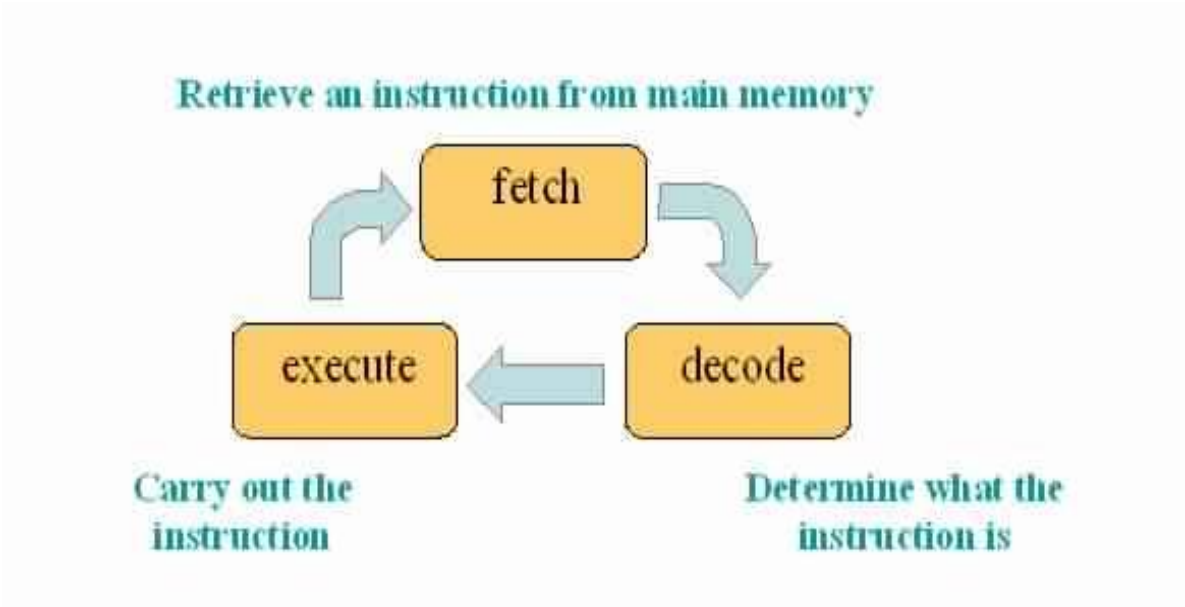
The Processor

The 3 main steps by processor:

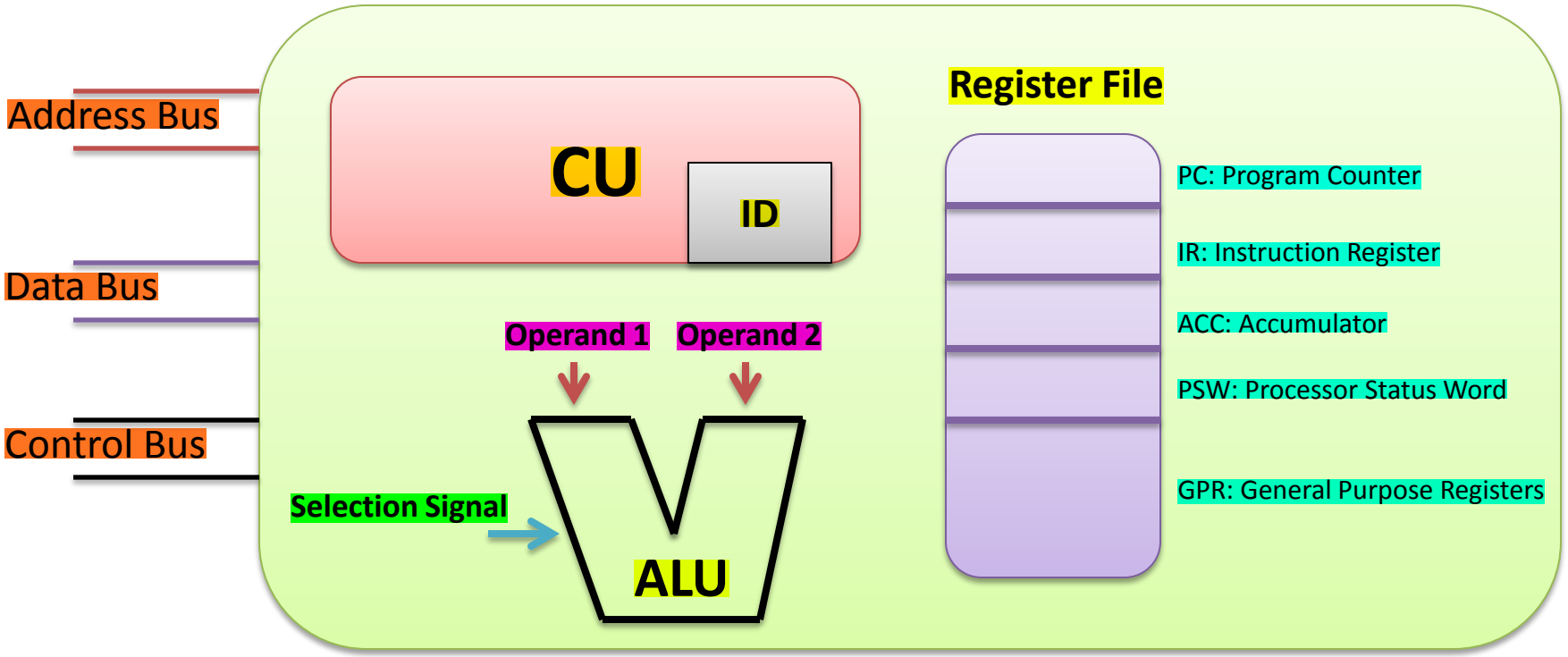
1- Fetch

2- Decode

3- Execute



Inside the processor



CU : Control Unit

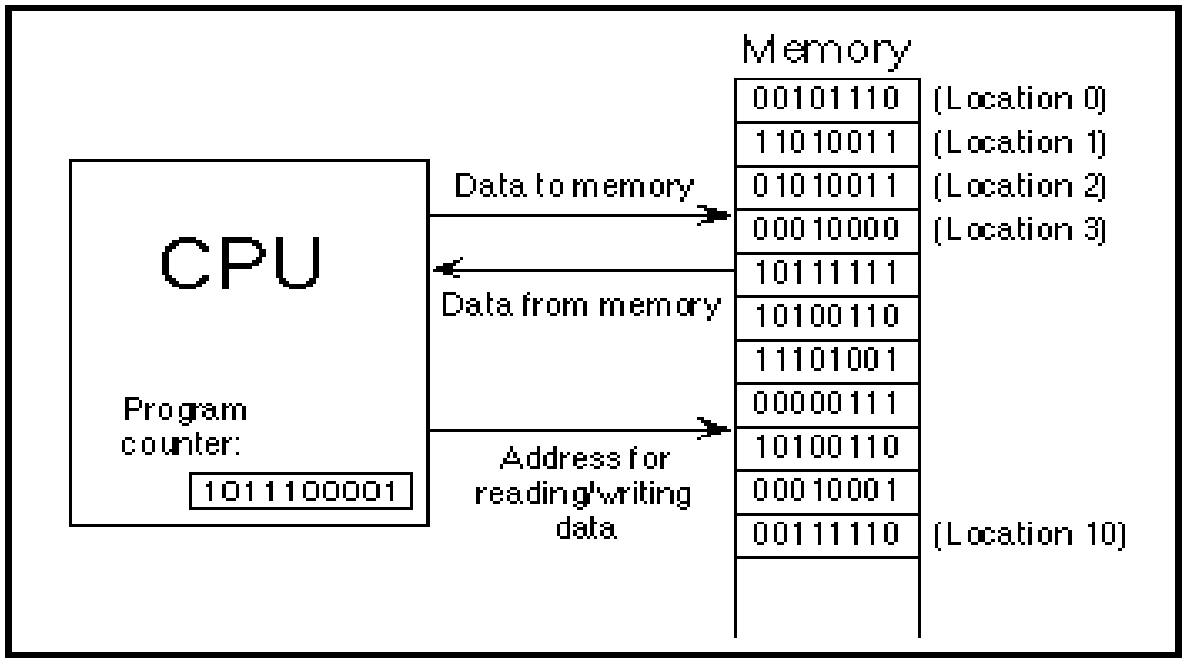
ID : Instruction Decoder

ALU: Arithmetic Logic Unit

Processor Operation

1- Fetch :

By CU “Control Unit” from the main memory.



2- Decode :

Inside CU "Control Unit" by ID "Instruction Decoder".

Every processor has its **instruction set** which is the group of instructions that could be executed by the processor.

Every instruction has a unique binary representation called **"Opcode".**

The decoding step is responsible for defining the operation required by the instruction fetched from the memory, and defining the operands of this instruction then pass these information to the ALU.

Instruction Set

Instruction	Op Code
ADD	011
SUB	101
AND	110
OR	001
XOR	111
SHIFT	100

Note, The instruction set differs from a processor to other in number of instructions, type of instruction and even for op code of the similar instructions

Processor Operation

Decoding Example

Given the shown instruction format of a certain processor and the same instruction set mentioned in the previous slide, the CU fetched the following instruction:

Instruction Format

Op Code	Operand 1	Operand 2
3 bit	3 bit	2 bit

10111011

101	110	11

Back to the instruction set, we will find that 101 is the op code for SUB operation. This means that this instruction is:

SUB 6 3

6 - 3

Question …

1- Is the compiler is target specific … ? I mean if a compiler for a processor X, can it compile for a processor Y … ? Why ?

2- A code is compiled for processor X, could it be executed on a processor Y … ? Why ?

Instruction Set Architecture
ISA

	RISC "Reduced Instruction Set Architecture"	CISC "Complex Instruction Set Architecture"
Performance	—	—
Cost	—	—
Size	—	—
Power Consumption	—	—

Instruction Set Architecture

So, it is now clear that CISC is not better that RISC or vice versa. It is all about the company mentality. Intel is one of the biggest companies in the market and it uses CISC machines, while ARM which is also one of the biggest companies in processor designing uses RISC.

Note that not all the ISA are only CISC and RISC, other types are existing but it has some drawbacks or used for specific reasons, like:

العيوب

- **OISC** "One Instruction Set Computing"
- **NISC** "No Instruction Set Computing"
- **ZISC** "Zero Instruction Set Computing"

Instruction Decoder

There are two types of “ID”

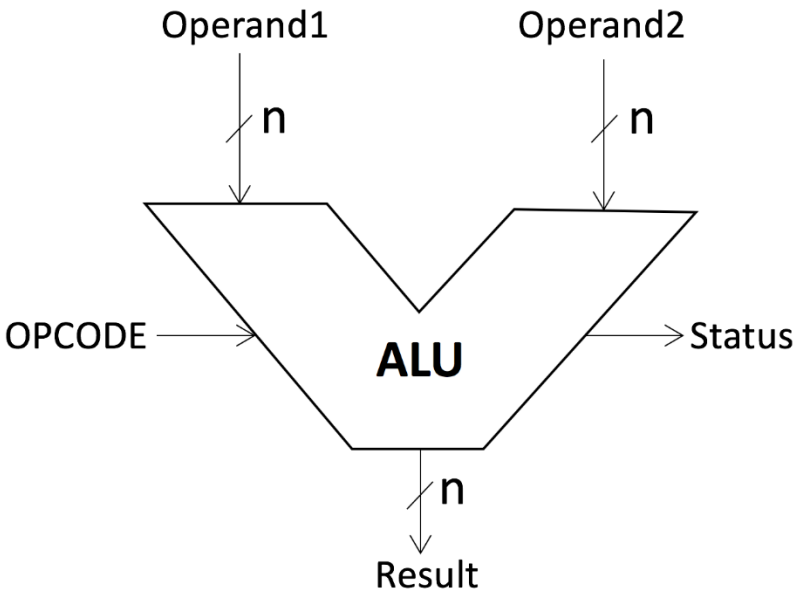
- **Hardwired**:
  uses hardware logic gates to decode Instructions. “Very fast” “High cost“

- **Micro-Programmed**:
  Uses a software to compare instruction decoded with saved instructions in a memory.
  “Slow” “Less cost”

3- Execute:

By ALU "Athematic Logic Unit".

It contains many logic gates for all the supported instructions.



Register File

It is certain type of memory existing in the processor. Each word is called register and has a specific usage. The register file differs from processor to other, but the following are the common registers:

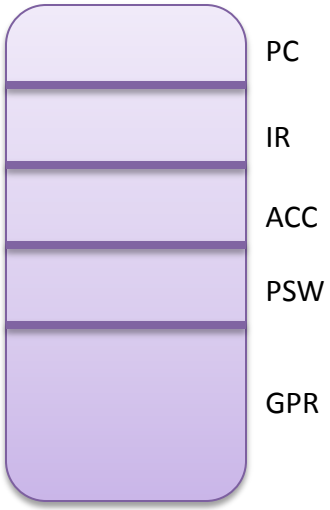
PC “Program Counter” : Address of the next instruction to fetch, decode and execute.

IR “Instruction Register”: Fetched instruction to be decoded and executed.

ACC “Accumulator” : The Real Result From ALU.

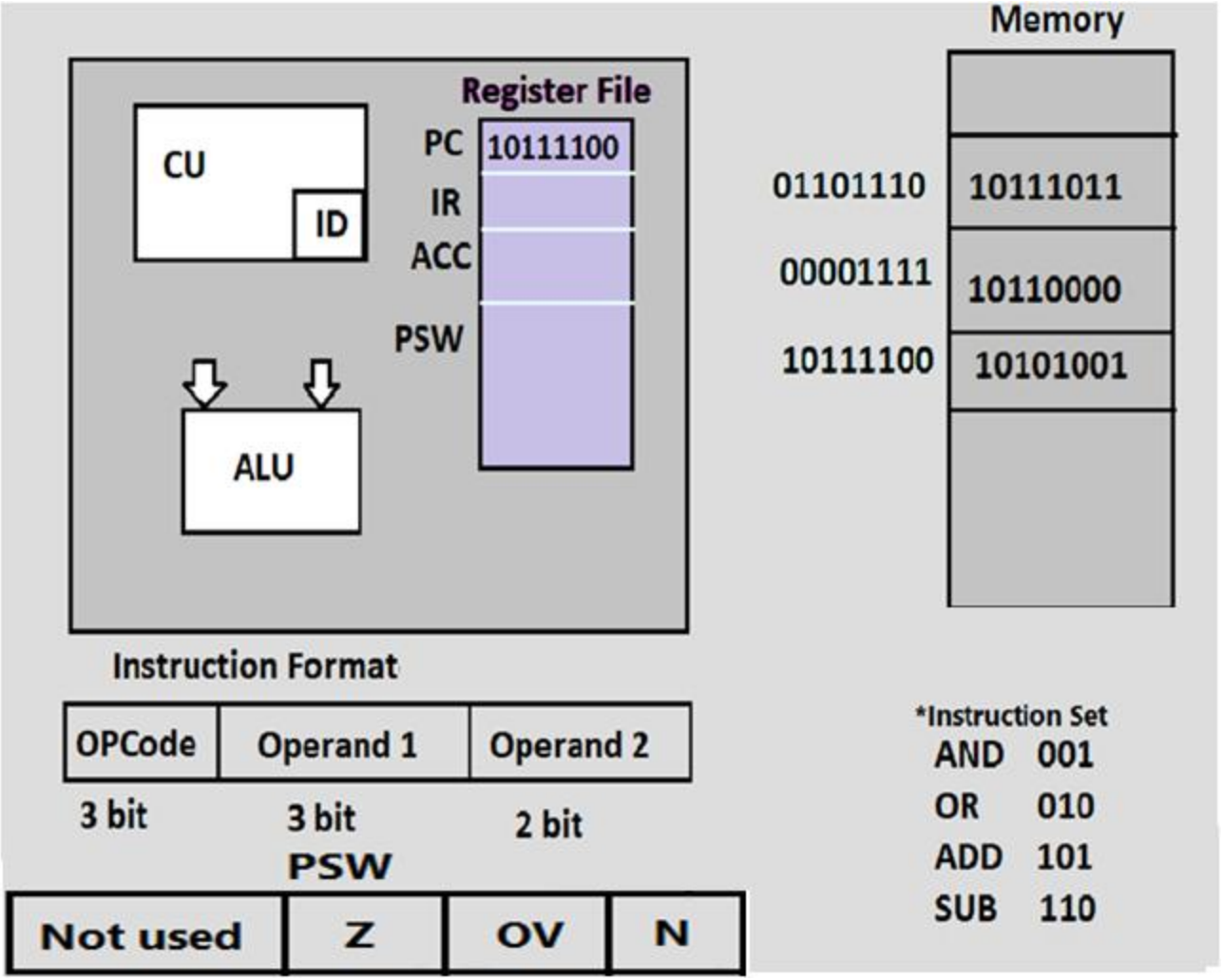
PSW “Processor Status Word”: Word Byte Holds flags about the result “Status”.

GPR “General Purpose Registers”: General registers used by the user to define high speed accessed data using the C keyword ‘register’.

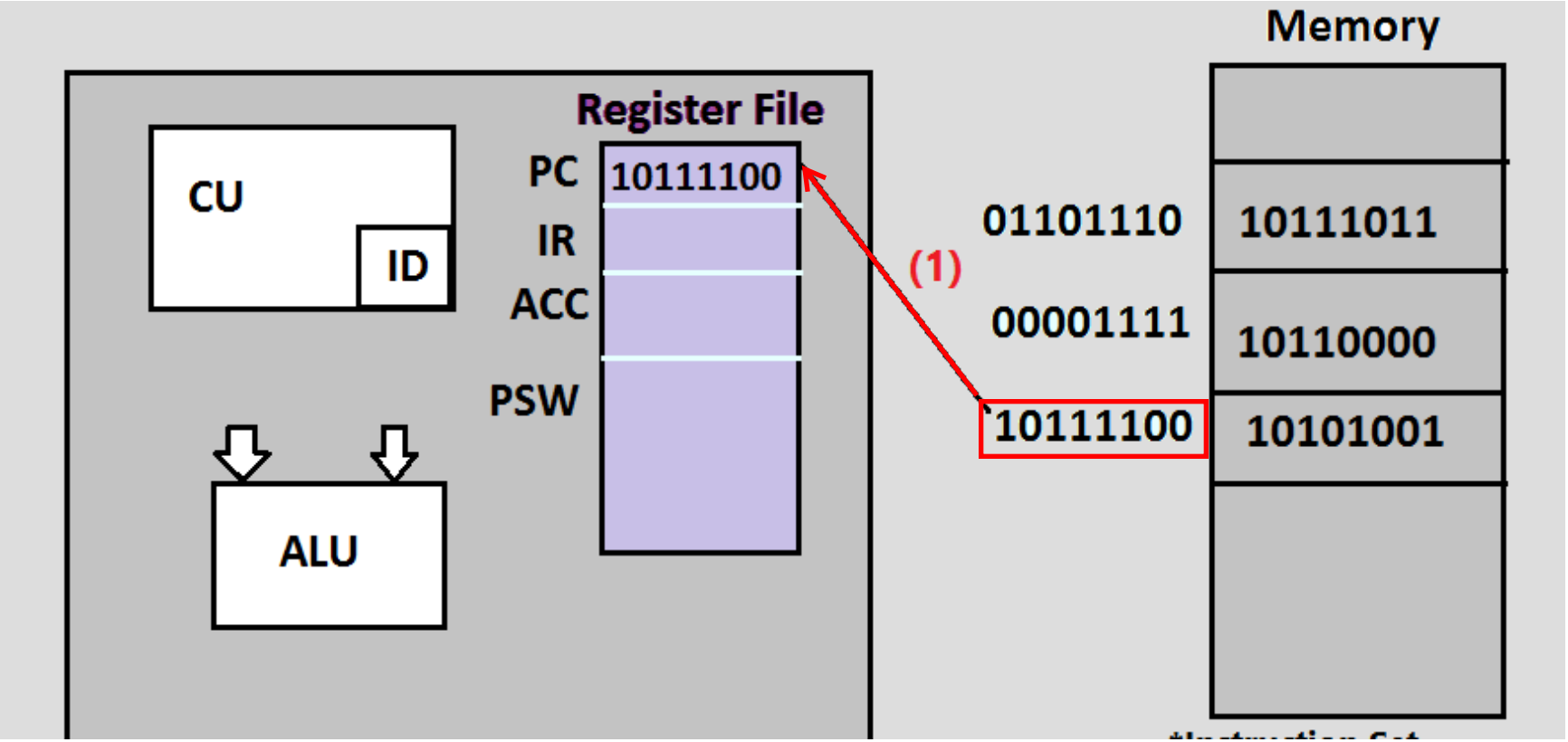


Exercise

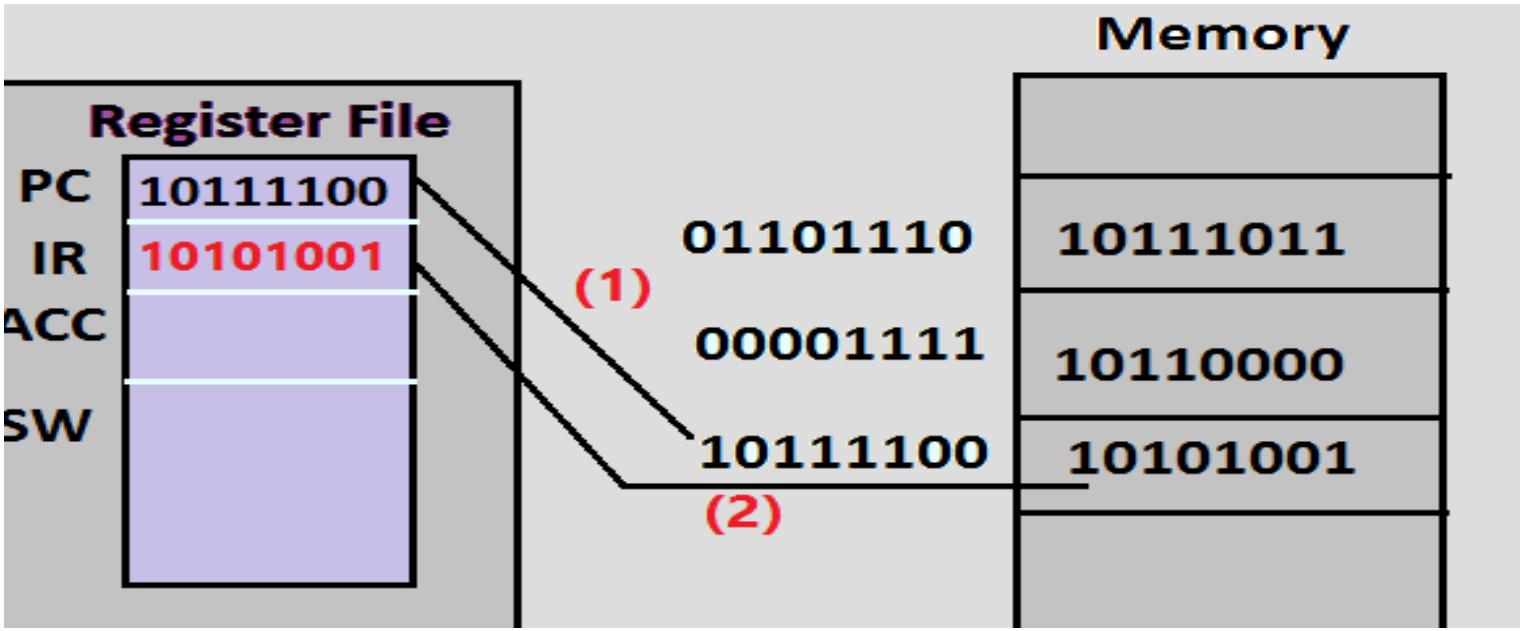
Consider the following processor, perform one complete processor cycle



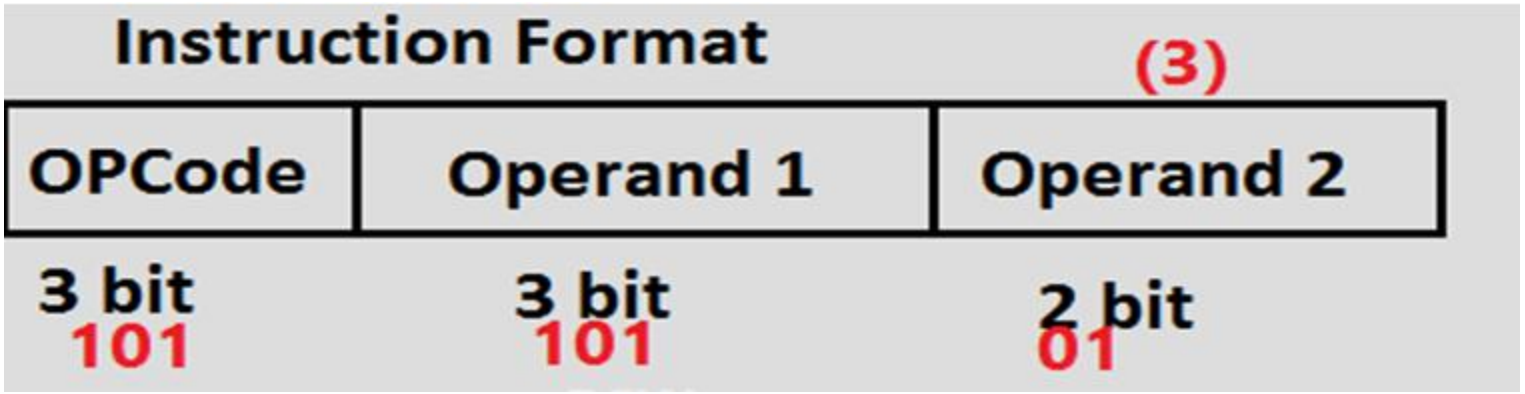
Step1: Fetch

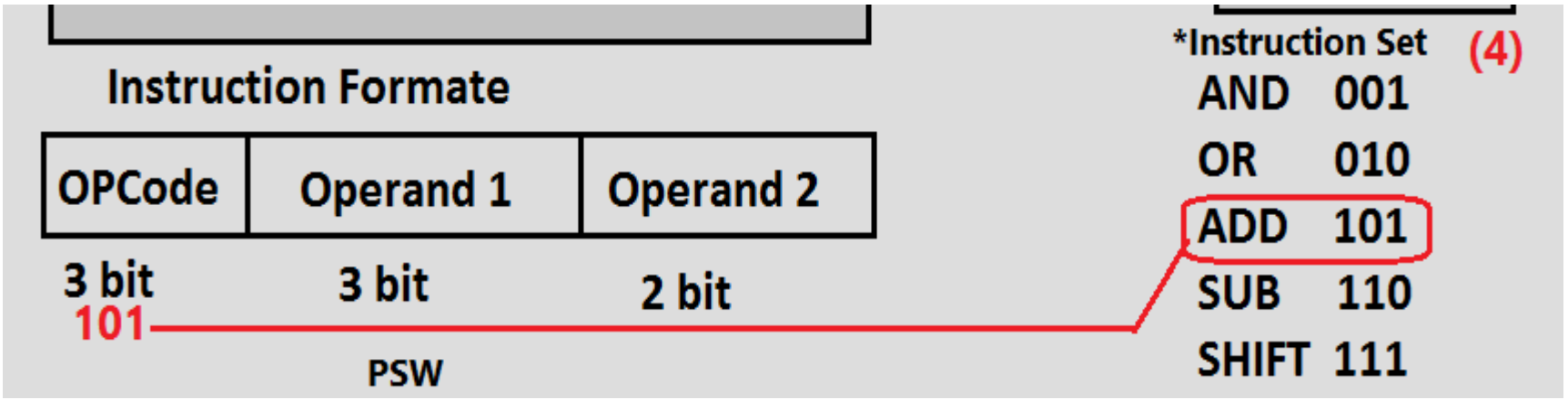

Memory
Register File
CU
ID
PC
IR
ACC
PSW
10111100
ALU
(1)
01101110
00001111
10111100
10111011
10110000
10101001

Step1: Fetch

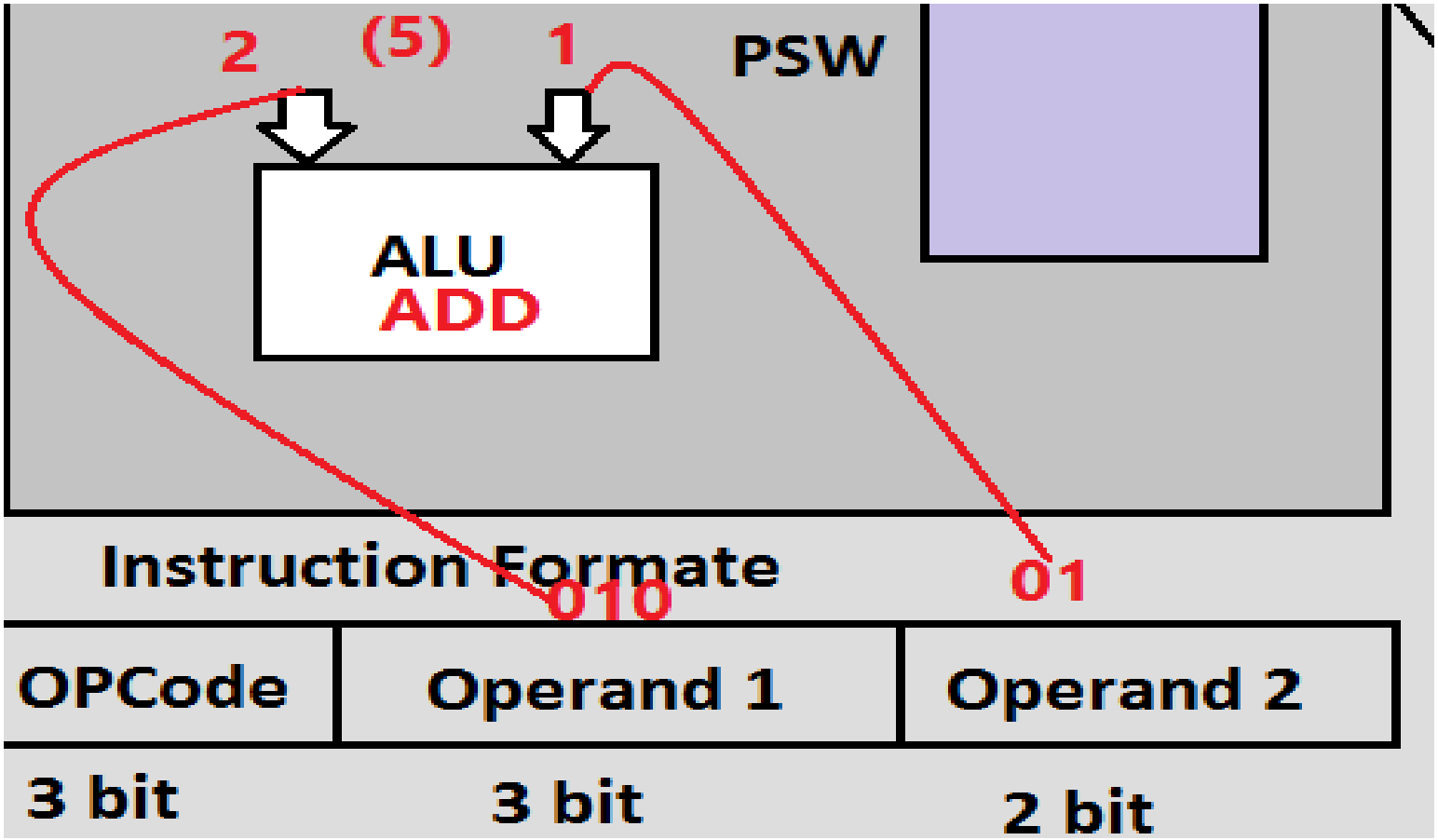

Memory
Register File
PC
10111100
IR
10101001
ACC
SW
(1)
01101110
00001111
10111100
(2)
10111011
10110000
10101001

Step2: Decode

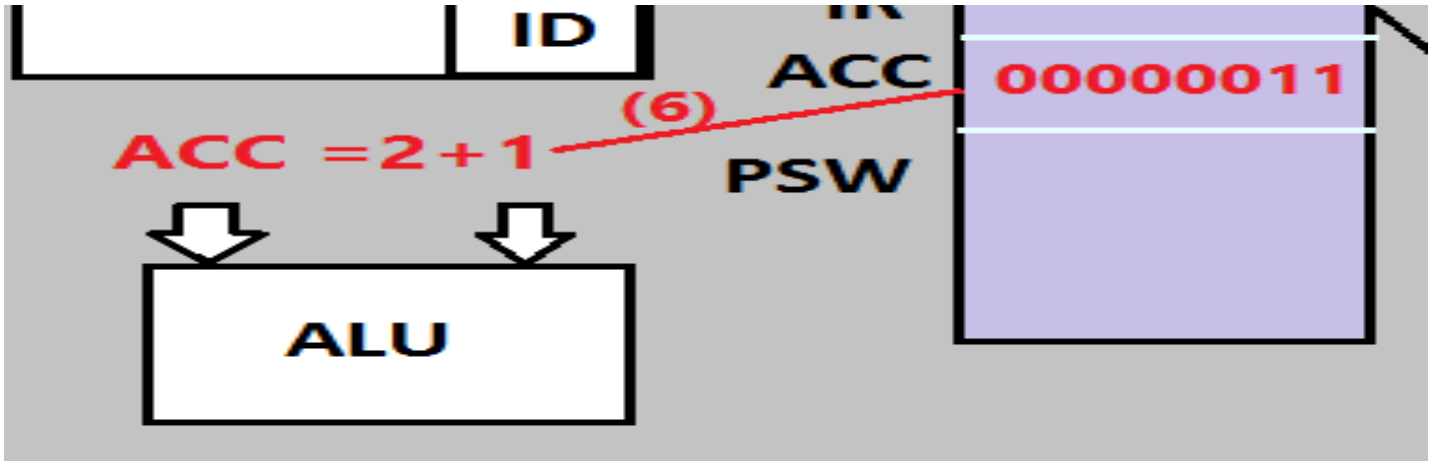




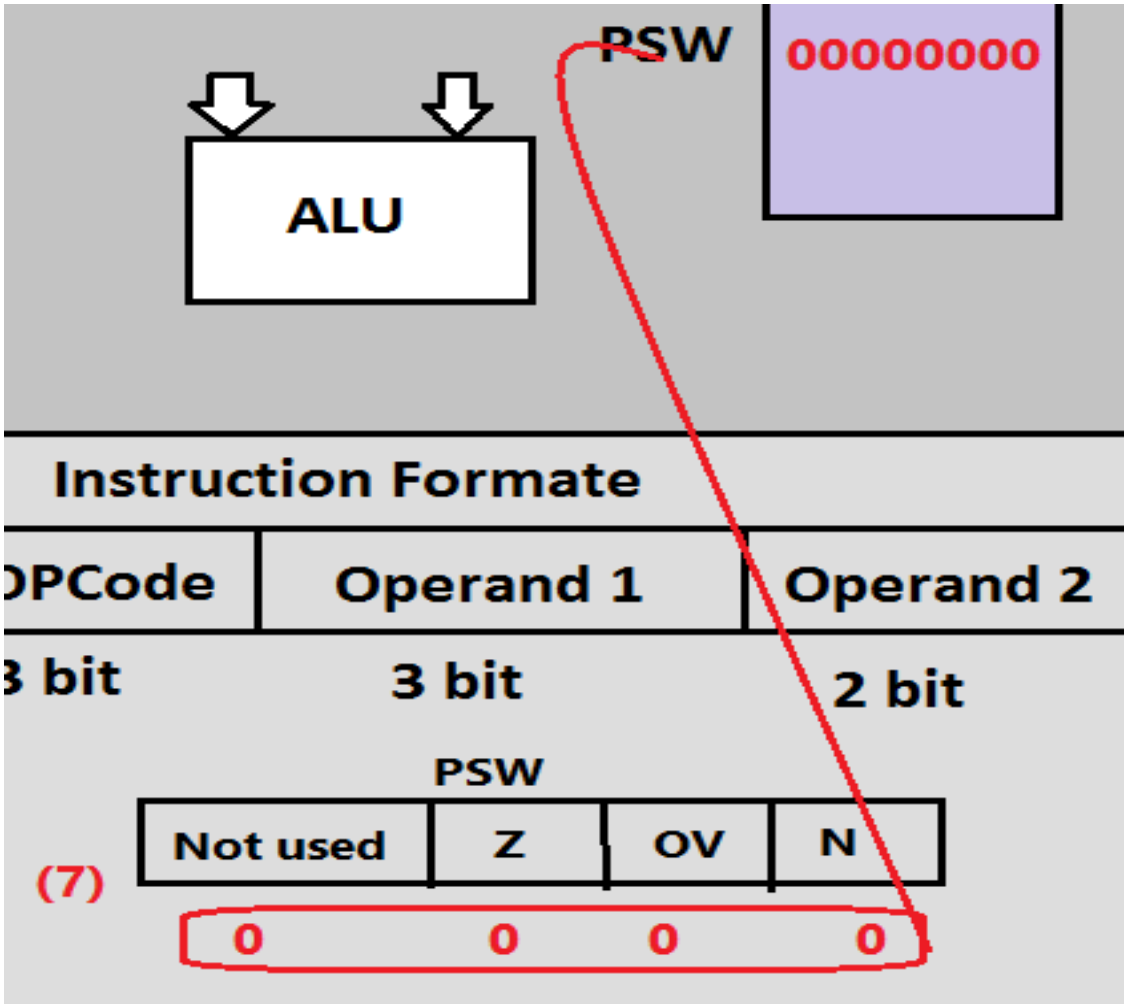
Step2: Decode



Step3: Execute

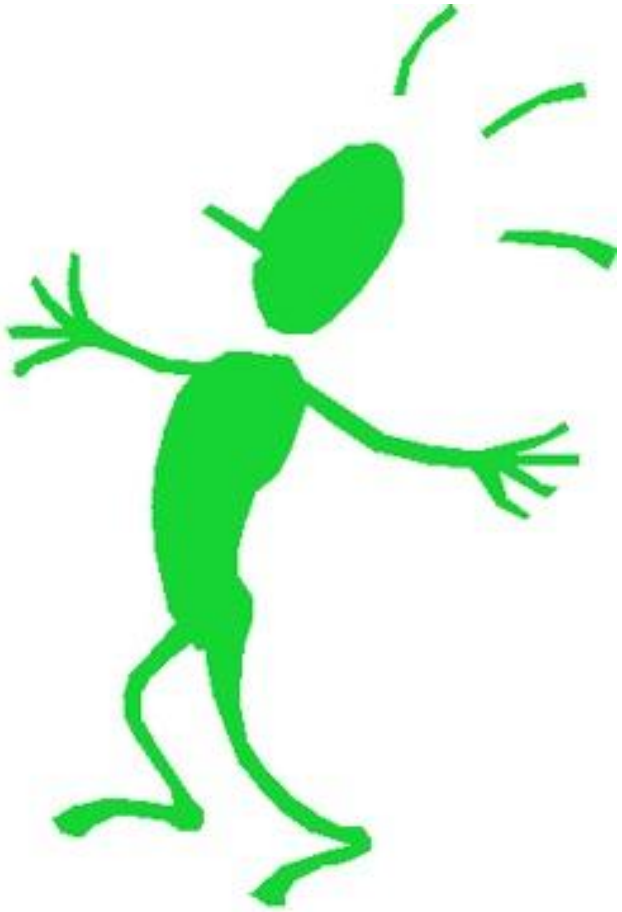


Step3: Execute



The End ...

Any questions ... ?



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