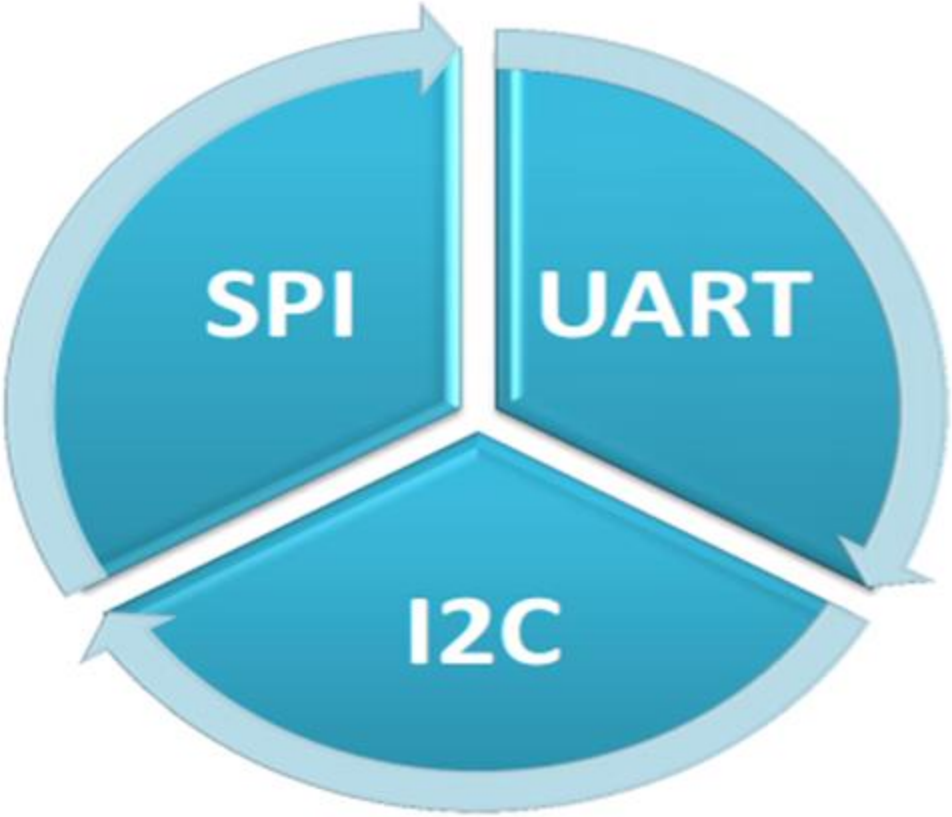

# Embedded Systems Interfacing

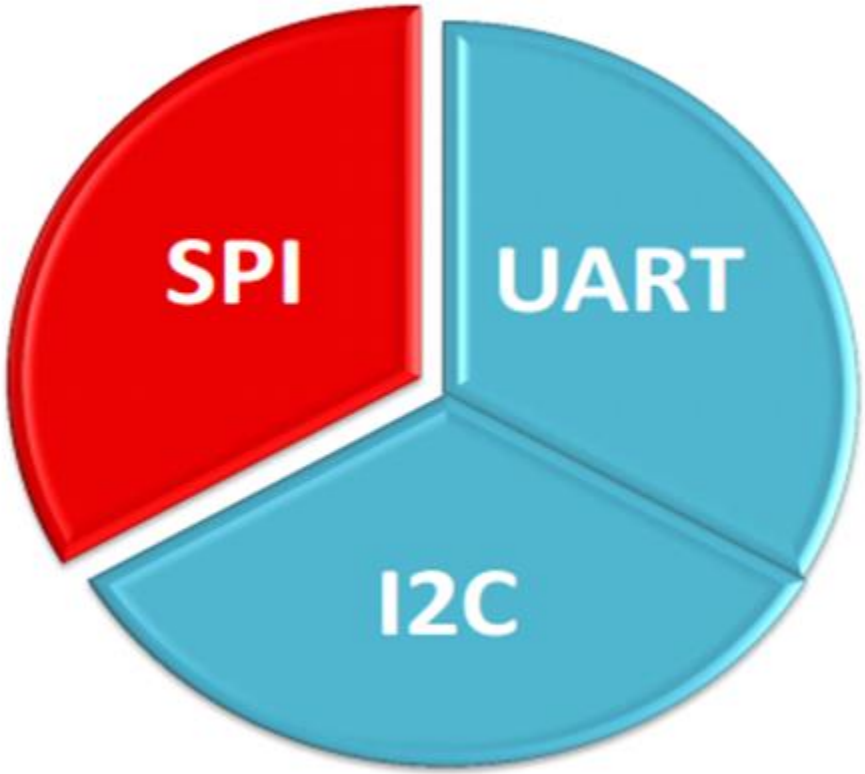
## Lecture Fourteen

## SPI Serial Communication

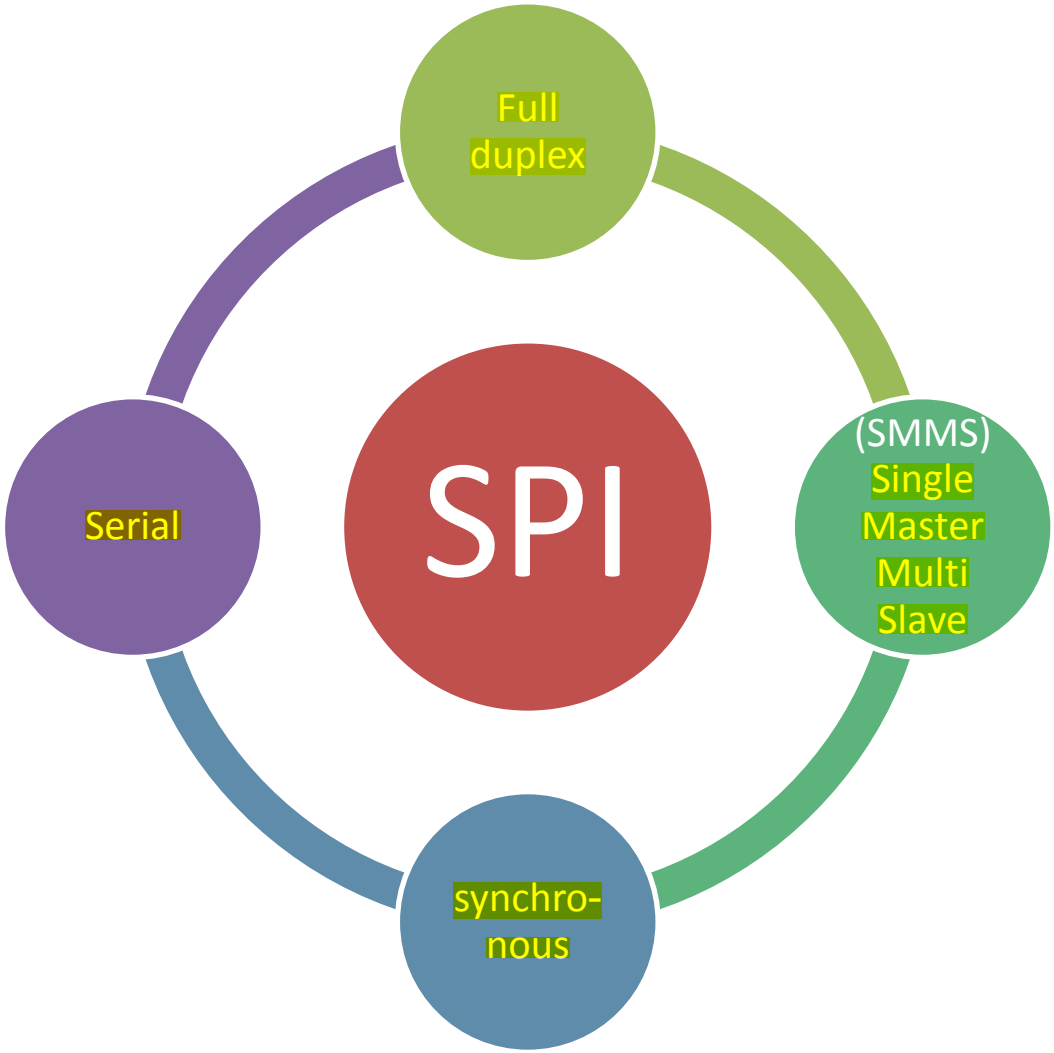
# Communication protocols



# Communication protocols



# SPI features



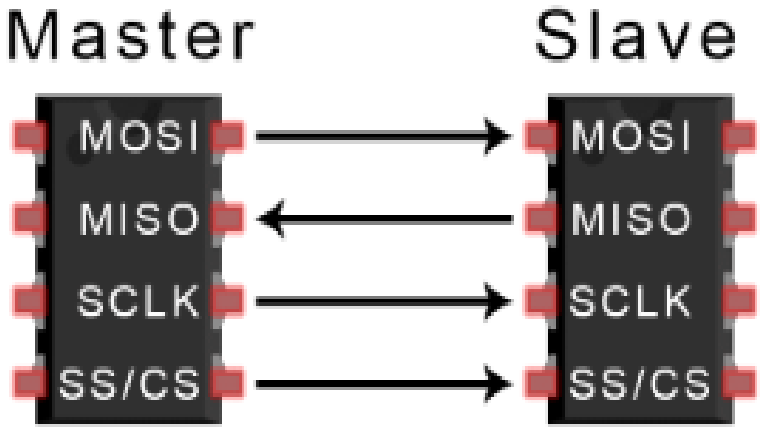
# SPI concept

## What is SPI?

- Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication.
- The SPI bus can operate with a single master device and with one or more slave devices.

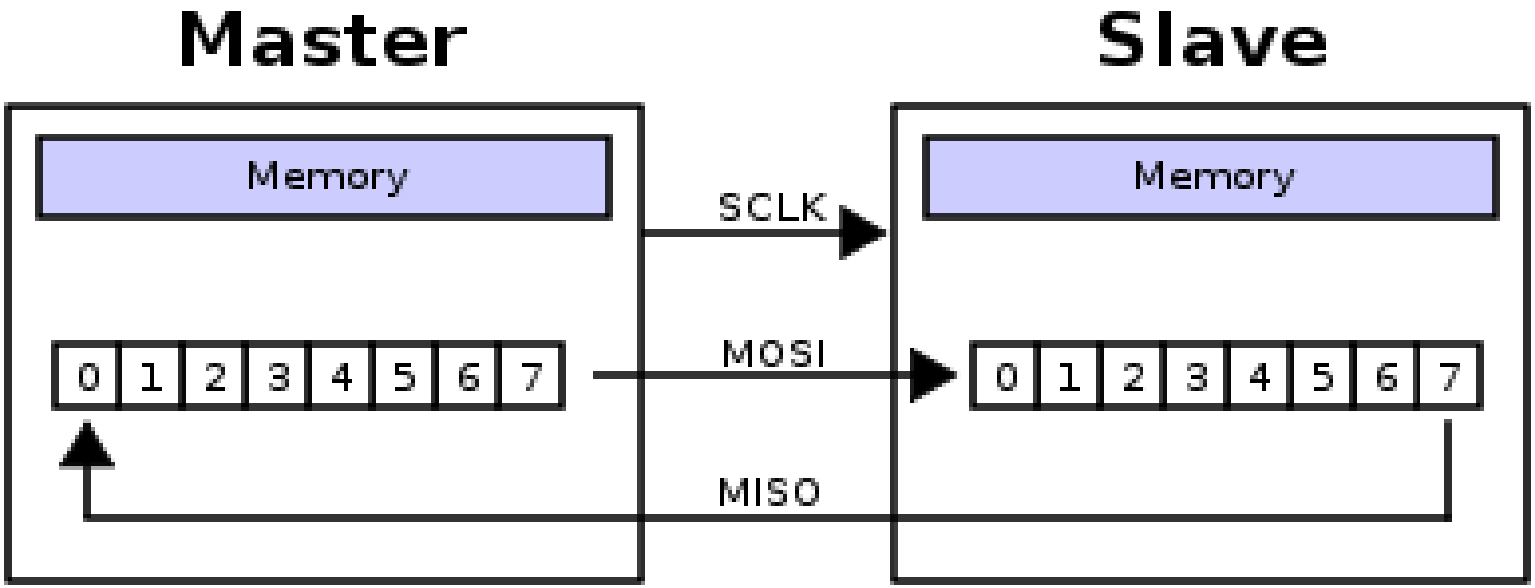
## SPI connections :

- SCLK : Serial Clock (output from master).
- MOSI : Master Output, Slave Input (output from master).
- MISO : Master Input, Slave Output (output from slave).
- SS : Slave Select (active low, output from master).



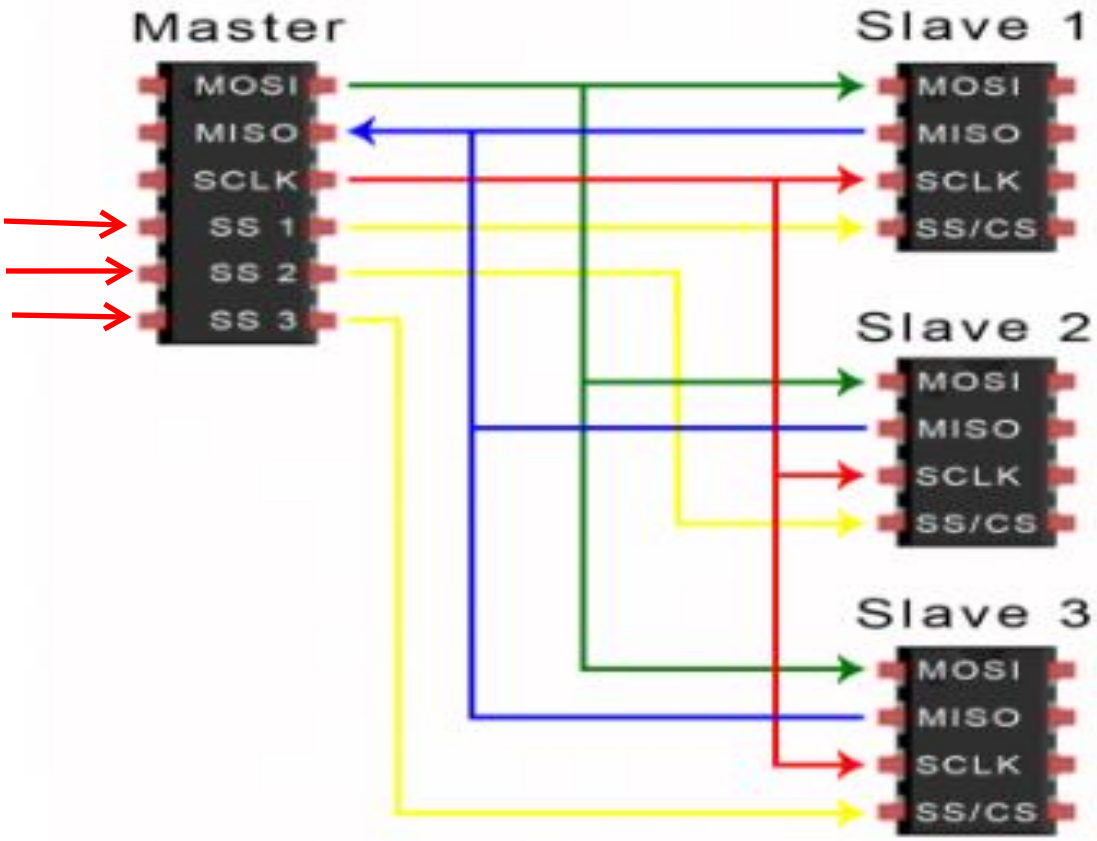
# SPI Operation

The SPI operation is a shift register operation. The master swaps a bit with the slave every clock cycle.



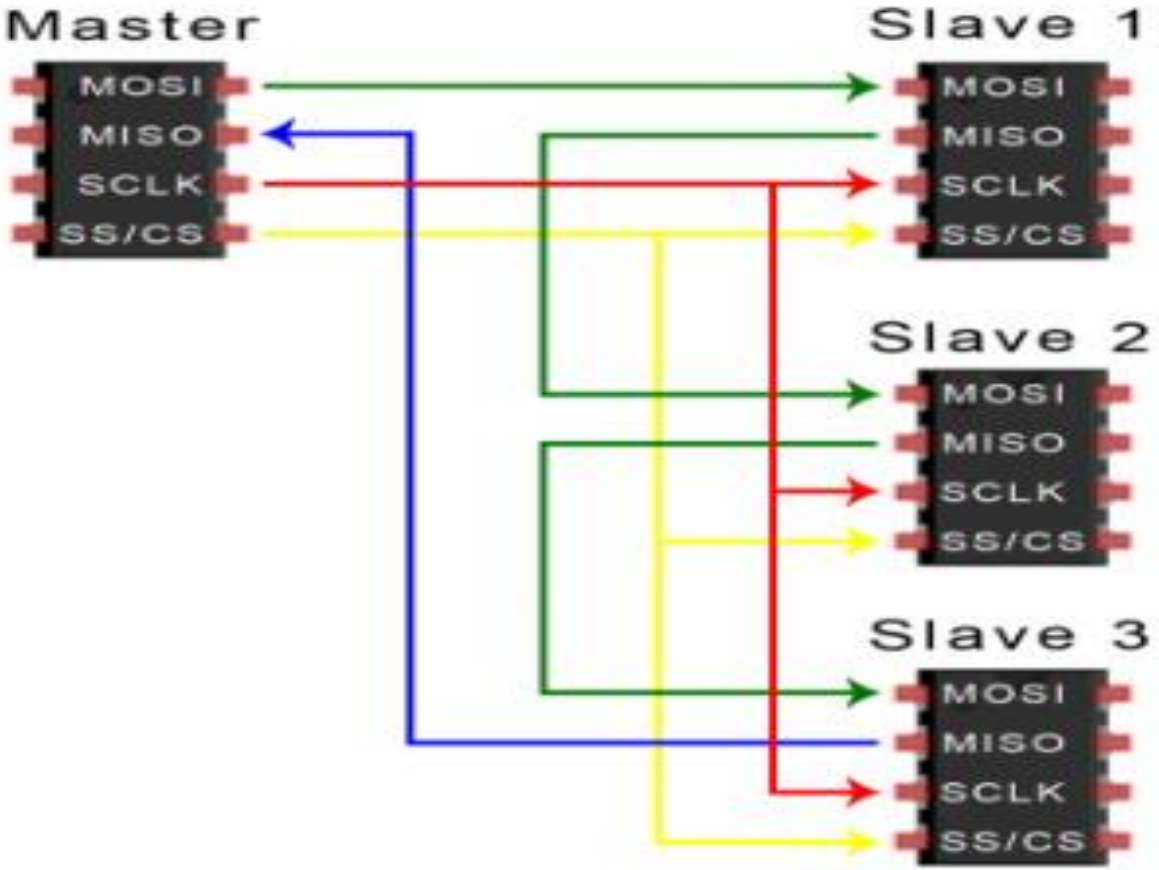
# SPI Network

## Type 1: Independent Slaves



# SPI Network

**Type 1: Daisy Chain**



# SPI Clock

The clock signal synchronizes the output of data bits from the master to the sampling of bits by the slave. One bit of data is transferred in each clock cycle, so the speed of data transfer is determined by the frequency of the clock signal. SPI communication is always initiated by the master since the master configures and generates the clock signal.

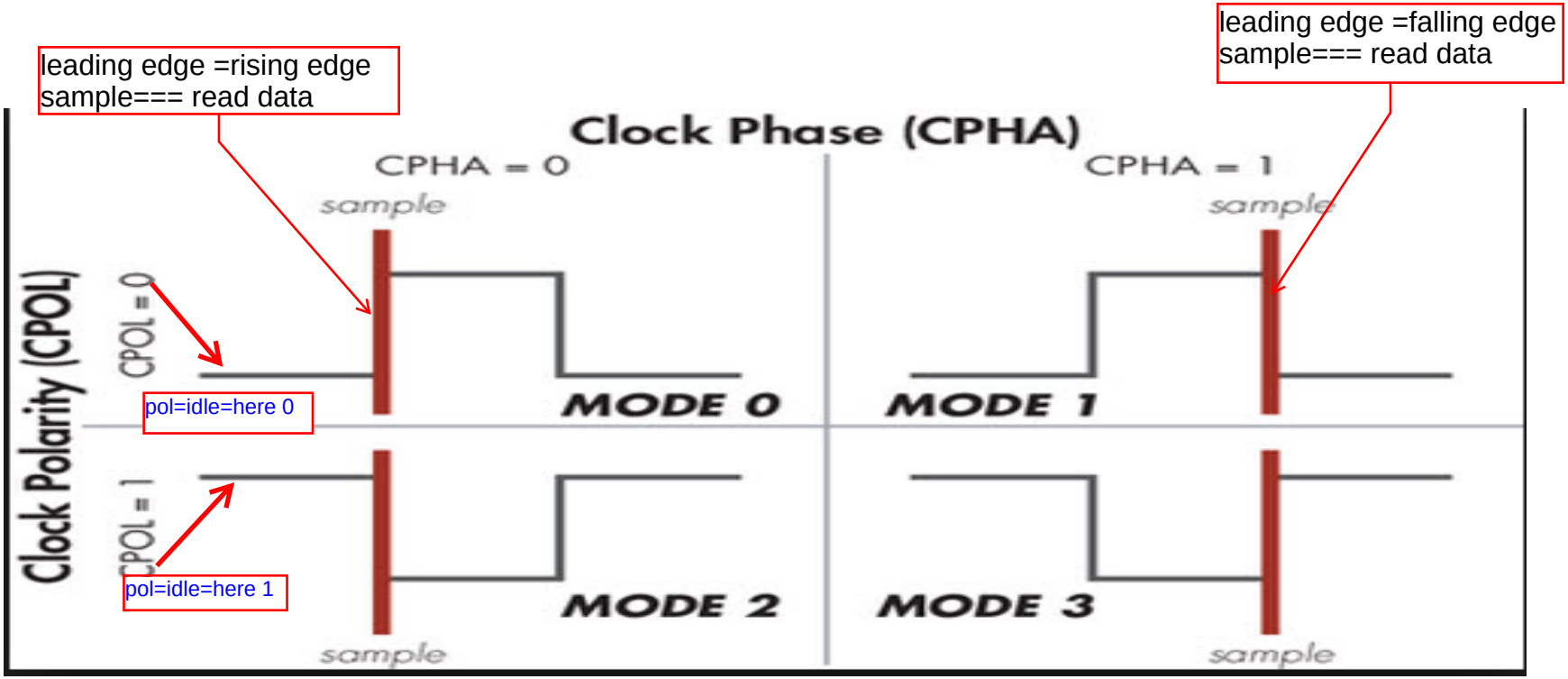
**SPI Clock Parameters:**

**Clock Polarity:** Defines the idle state of the clock

تحديد الإجراءات الرائدة التي يتعين اتخاذها

**Clock Phase** : Define the leading action to be taken. Because the clock has 2 edges; rising and falling edge, it is configurable to choose what to be done with the first edge (Called also Leading Edge). The master can choose to send data (Called also Toggle or Setup) with the leading edge. Or to choose to read data with leading edge (called also Sample).

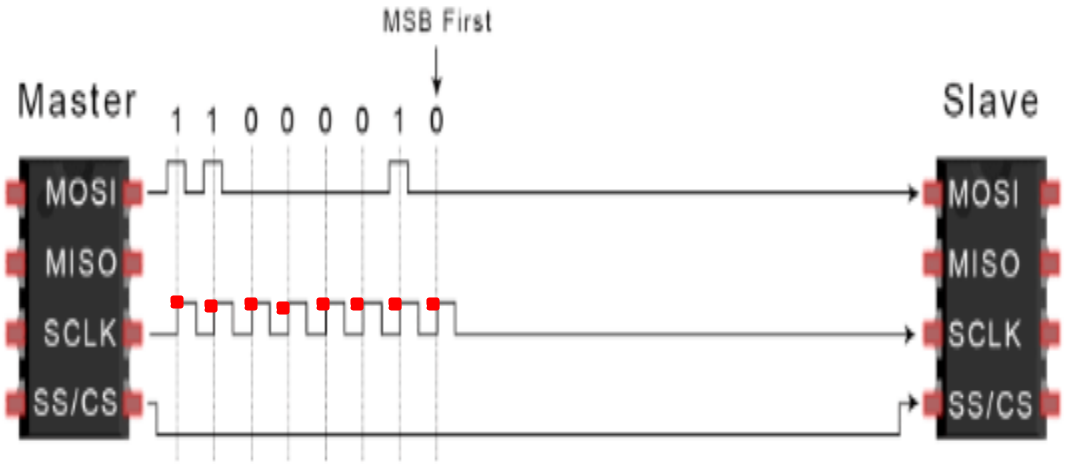
# SPI Clock


leading edge =rising edge
sample=== read data
leading edge =falling edge
sample=== read data
Clock Phase (CPHA)
CPHA = 0
CPHA = 1
sample
sample
Clock Polarity (CPOL)
CPOL = 0
CPOL = 1
pol=idle=here 0
pol=idle=here 1
MODE 0
MODE 1
MODE 2
MODE 3
sample
sample

# SPI concept

## STEPS OF SPI DATA TRANSMISSION

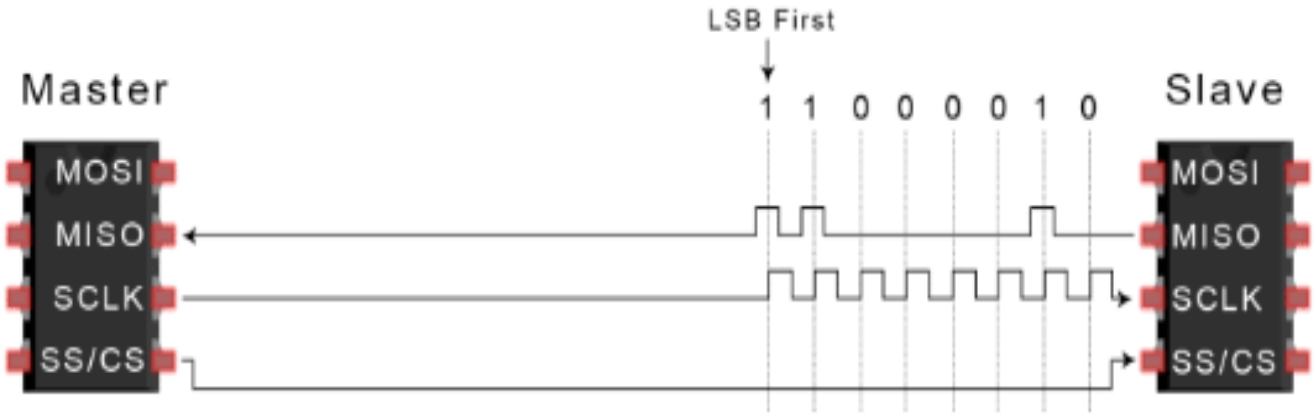
3. The master sends the data one bit at a time to the slave along the MOSI line. The slave reads the bits as they are received::



# SPI concept

**STEPS OF SPI DATA TRANSMISSION**

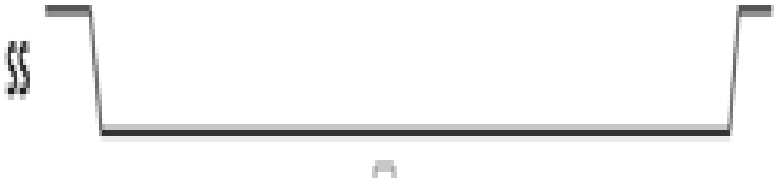
4. If a response is needed, the slave returns data one bit at a time to the master along the MISO line. The master reads the bits as they are received:



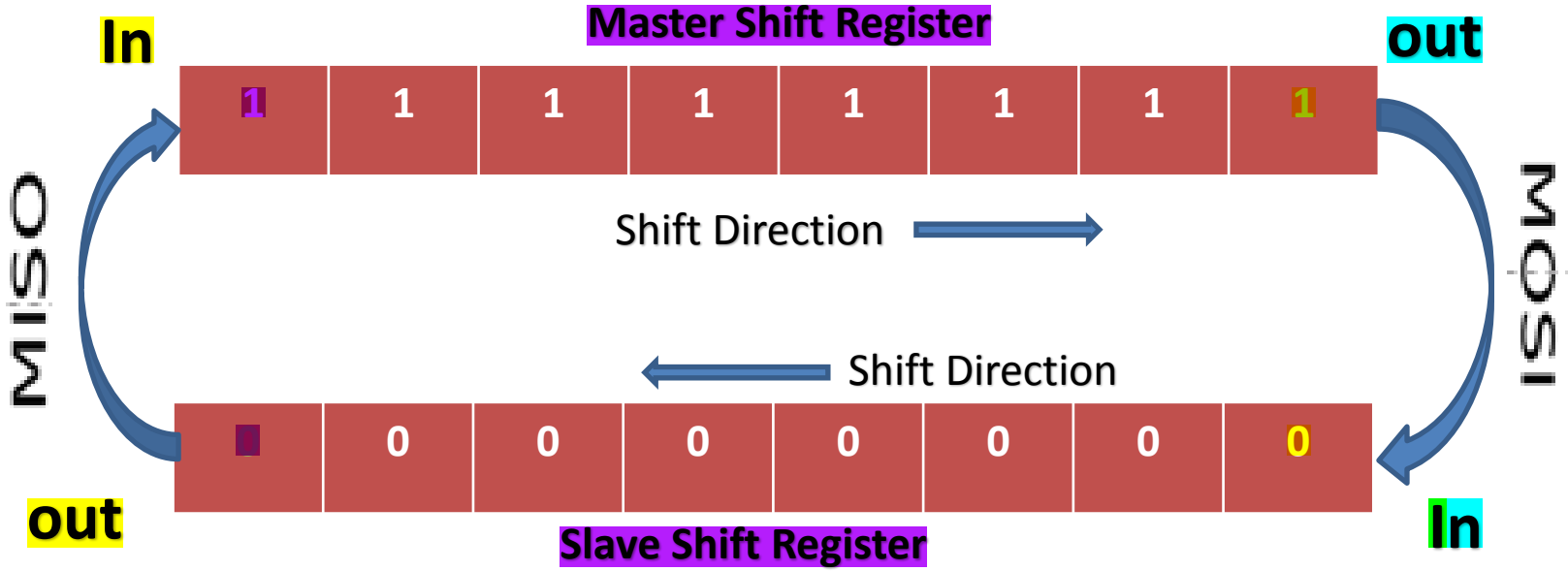
# SPI concept

**THE INTERCONNECTION BETWEEN MASTER AND SLAVE**

The SPI Master initiates the communication cycle when pulling low the Slave Select SS pin of the desired Slave.



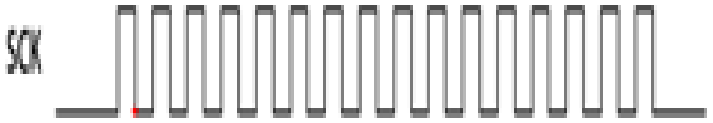

Master and Slave prepare the data to be sent in their respective Shift Registers.



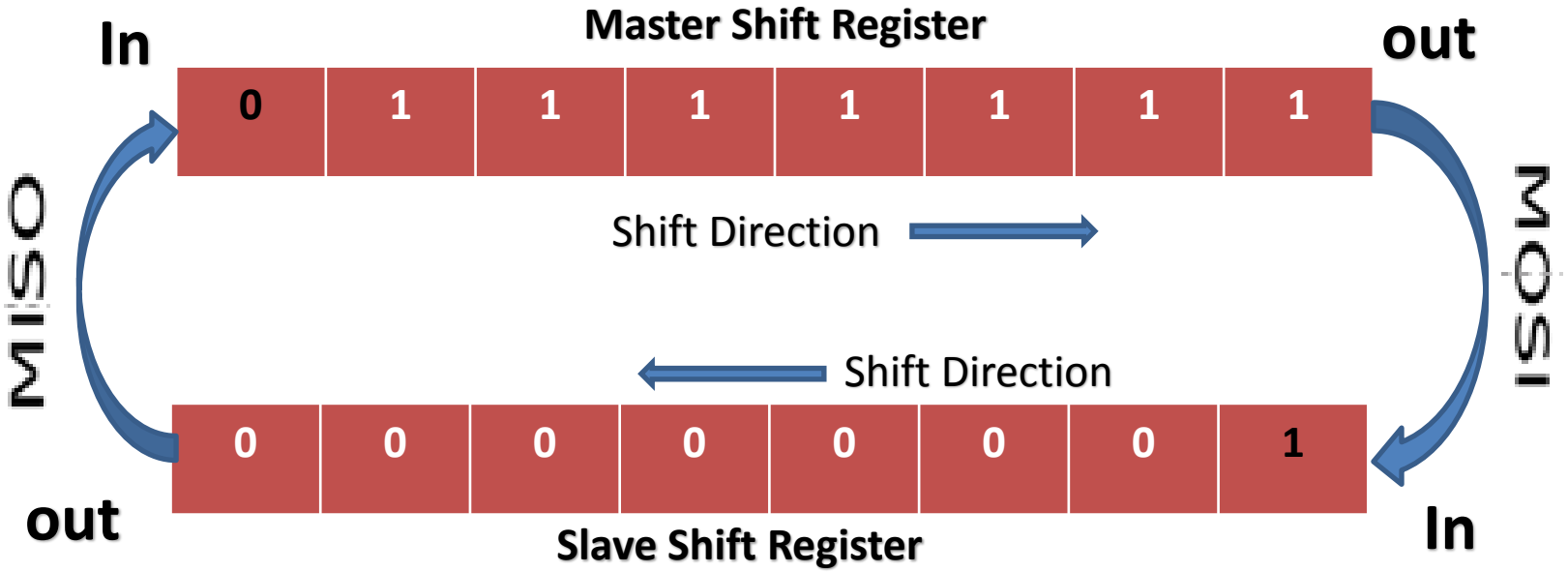
# SPI concept

**SPI DATA TRANSMISSION AND RECEIVE**

the Master generates the required clock pulses on the SCK line to interchange data.




Data is always shifted from Master to Slave on MOSI, line, and from Slave to Master on MISO, line.



LAB

Write SPI driver code, build a network with one of your colleagues and exchange data between together.

# Time To Code

# The End …

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