UNIVERSITY of DENVER

Lab 3: Directions

Student : Abdullah Bohamad

Instructor: Dr Goncalo Martins

Date of Experiment: Friday, 3 / October / 2025

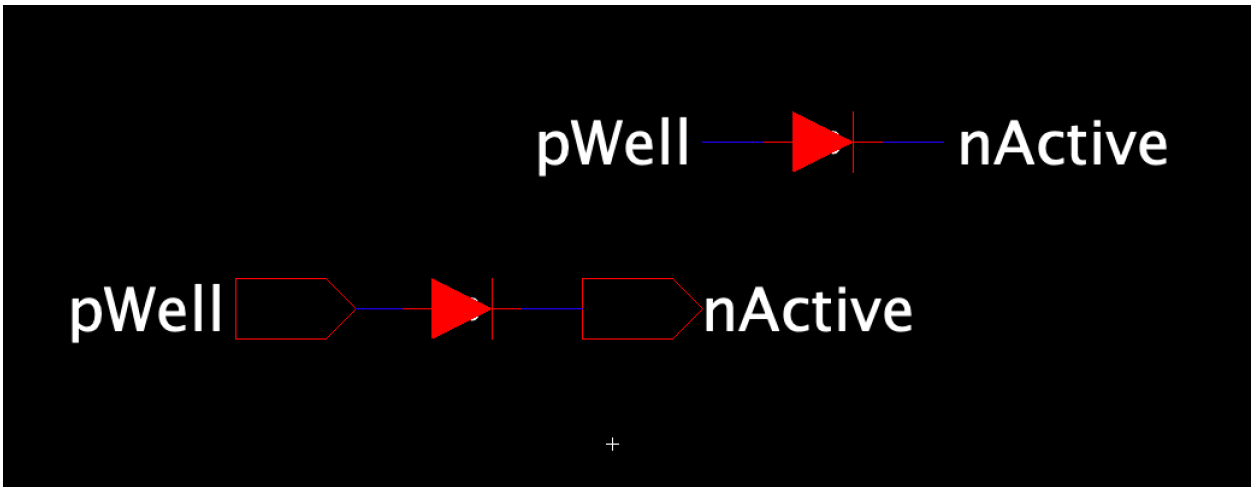
Introduction:

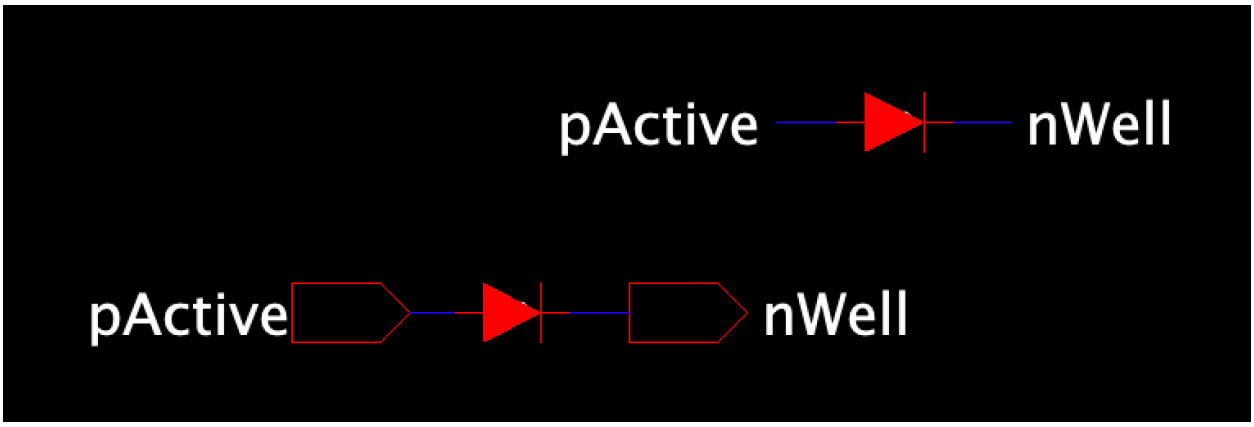
The design and implementation of padframes with built-in electrostatic discharge (ESD) protection is an essential step in modern VLSI fabrication. In this lab, the objective is to create a die that enables direct access to the terminals of an NMOS transistor through a padframe, while ensuring that each external connection is safeguarded against potential ESD events. This requires careful integration of protective PN junction diodes, properly structured pad cells, and a continuous VDD/GND bus system within a square padframe layout.

The lab emphasizes both schematic and layout perspectives. From a schematic standpoint, the pWell–nActive and pActive–nWell diodes must be modeled to demonstrate their protective behavior. Similarly, the pad cell must incorporate ESD diodes in order to clamp high transient voltages to safe levels. On the layout side, proper placement, well/substrate contacts, and guard rings are required to guarantee functionality and physical design rule compliance.

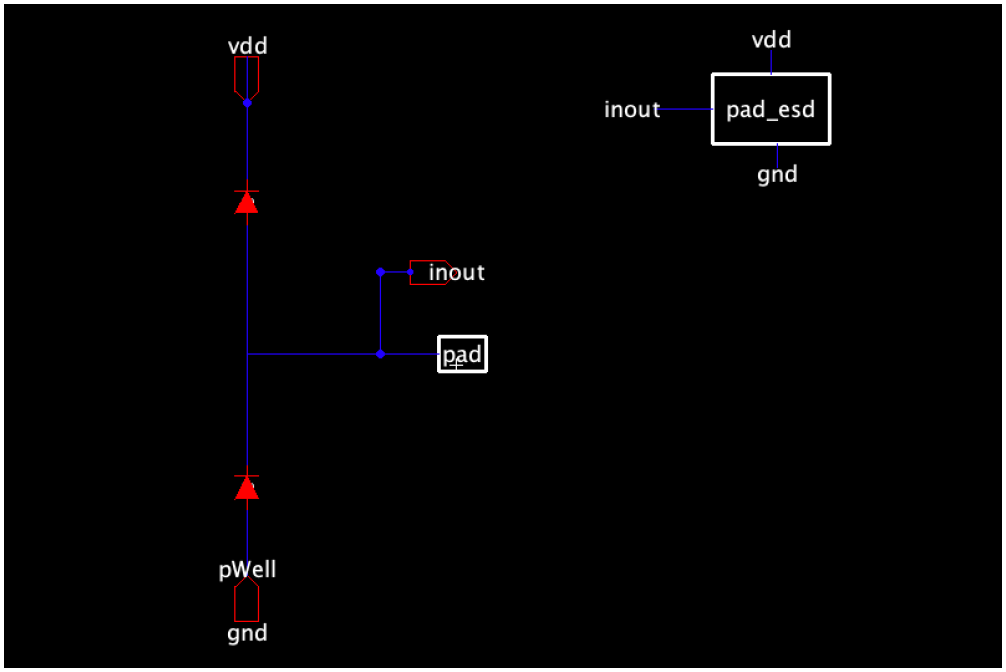
Schematics:

The schematic of the pWell-nActive and pActive-nWell diodes.

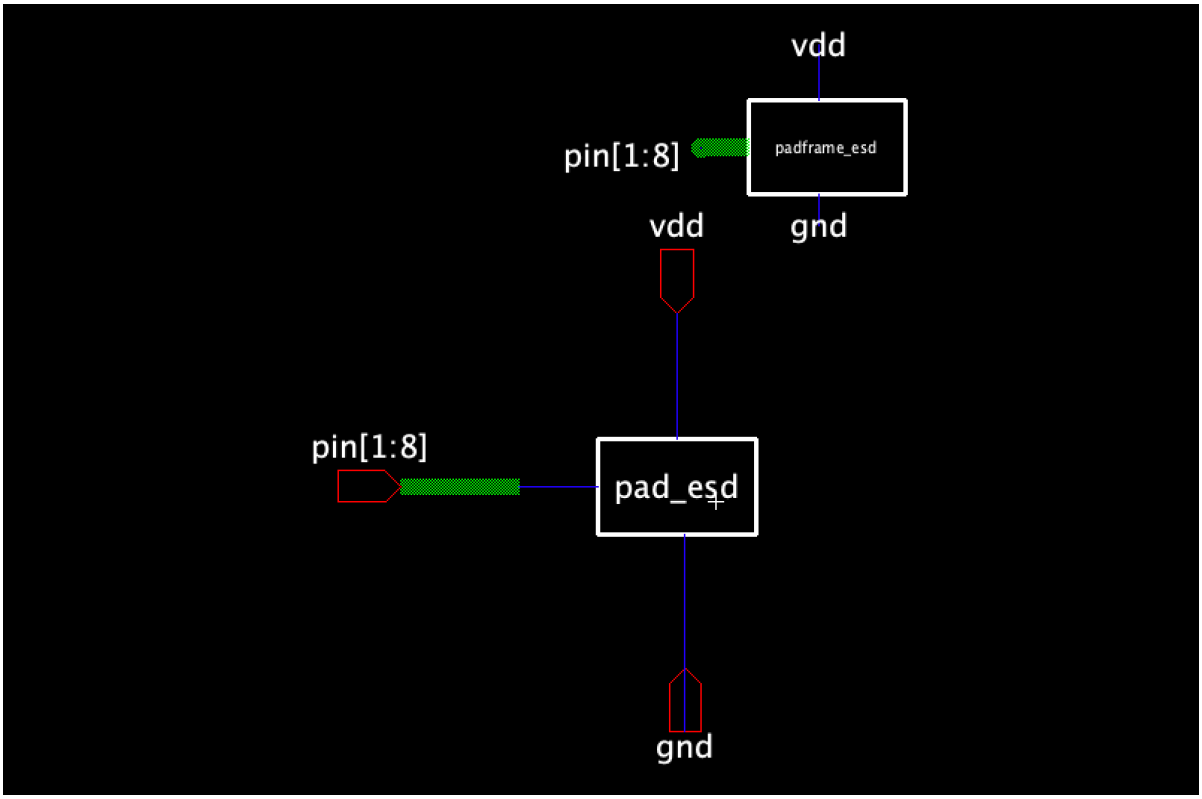




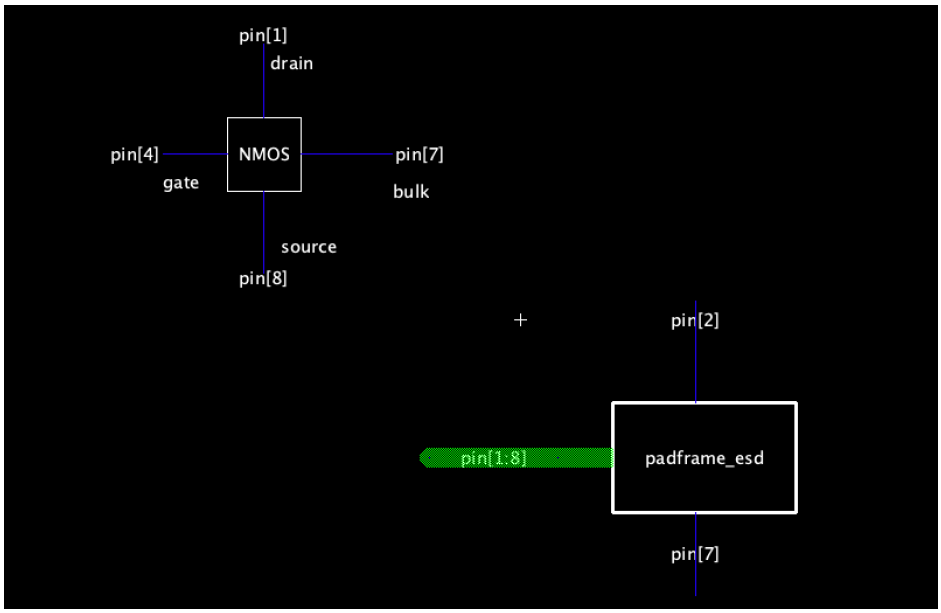
The schematic of the pad cell with ESD protection.



The schematic of the padframe with the VDD and GND bus connected together. The padframe should be a square and you should design it to have the minimum number of required pad cells to connect all the NMOS pinouts.



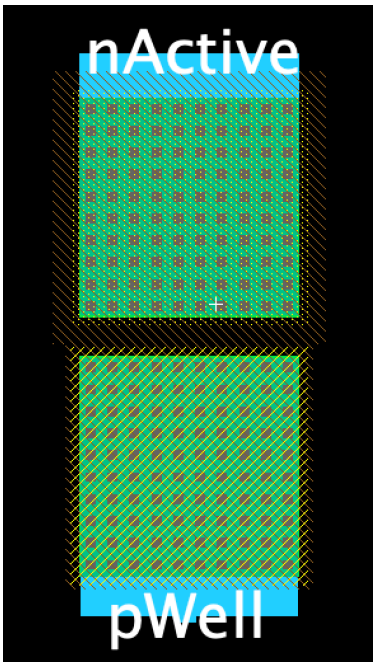
The schematic of the padframe with the NMOS.

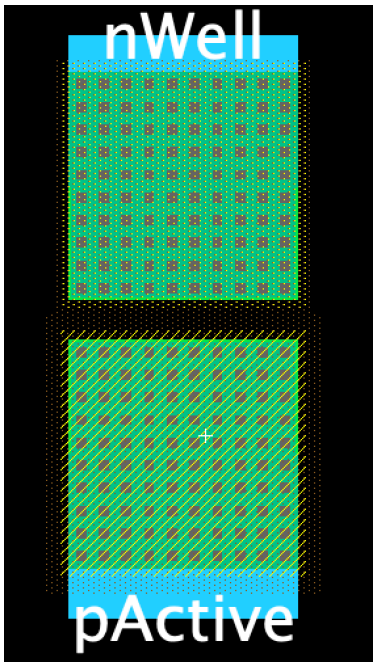


For the schematic designs, each decision was guided by the dual objectives of functionality and reliability. The inclusion of pWell–nActive and pActive–nWell diodes was essential to realize basic ESD protection, since these junctions provide a direct path for discharging high transient voltages to the supply rails, thereby safeguarding the NMOS and surrounding circuitry. A dual-diode clamp structure was chosen for each pad because it ensures protection against both positive and negative ESD events. The pad cell schematic incorporates these diodes along with proper substrate and well ties to maintain correct biasing and prevent latch-up. A minimal number of pad cells was selected to expose the NMOS terminals while also providing VDD and GND connections, reducing design complexity without sacrificing access to critical device nodes. The padframe was constructed as a square to follow standard layout conventions and to ensure uniform distribution of power and ground buses, simplifying integration and verification. Finally, tying the NMOS bulk to the appropriate potential (either source or a dedicated pad) was considered to balance design flexibility with pin efficiency, ensuring that the schematic provides both accurate device characterization and robust protection.

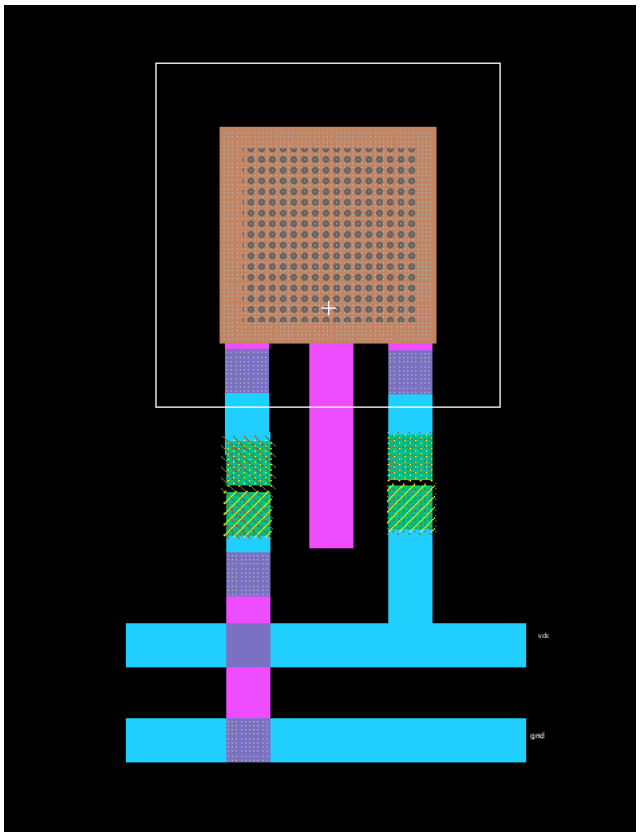
Layouts:

- The layout of the pWell-nActive and pActive-nWell diodes

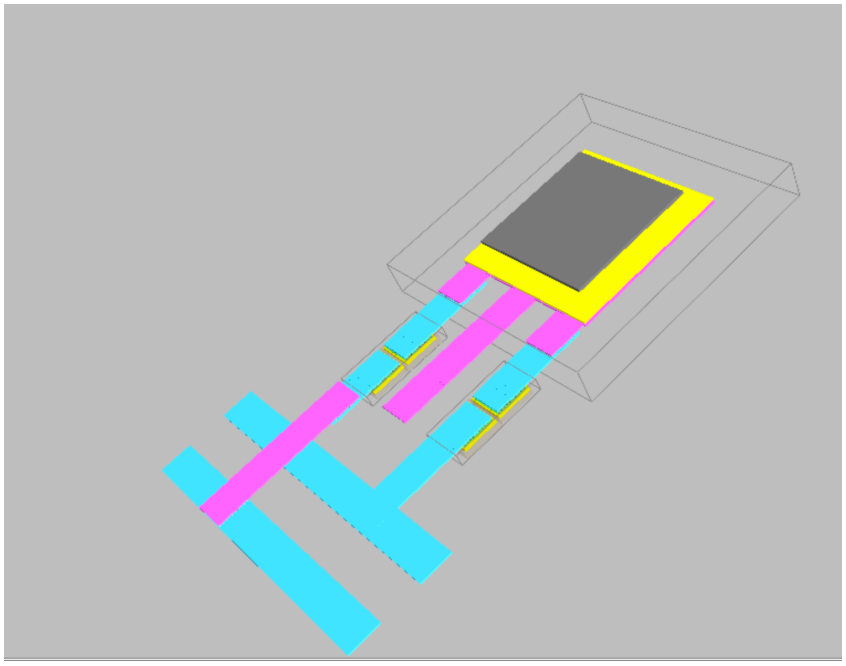




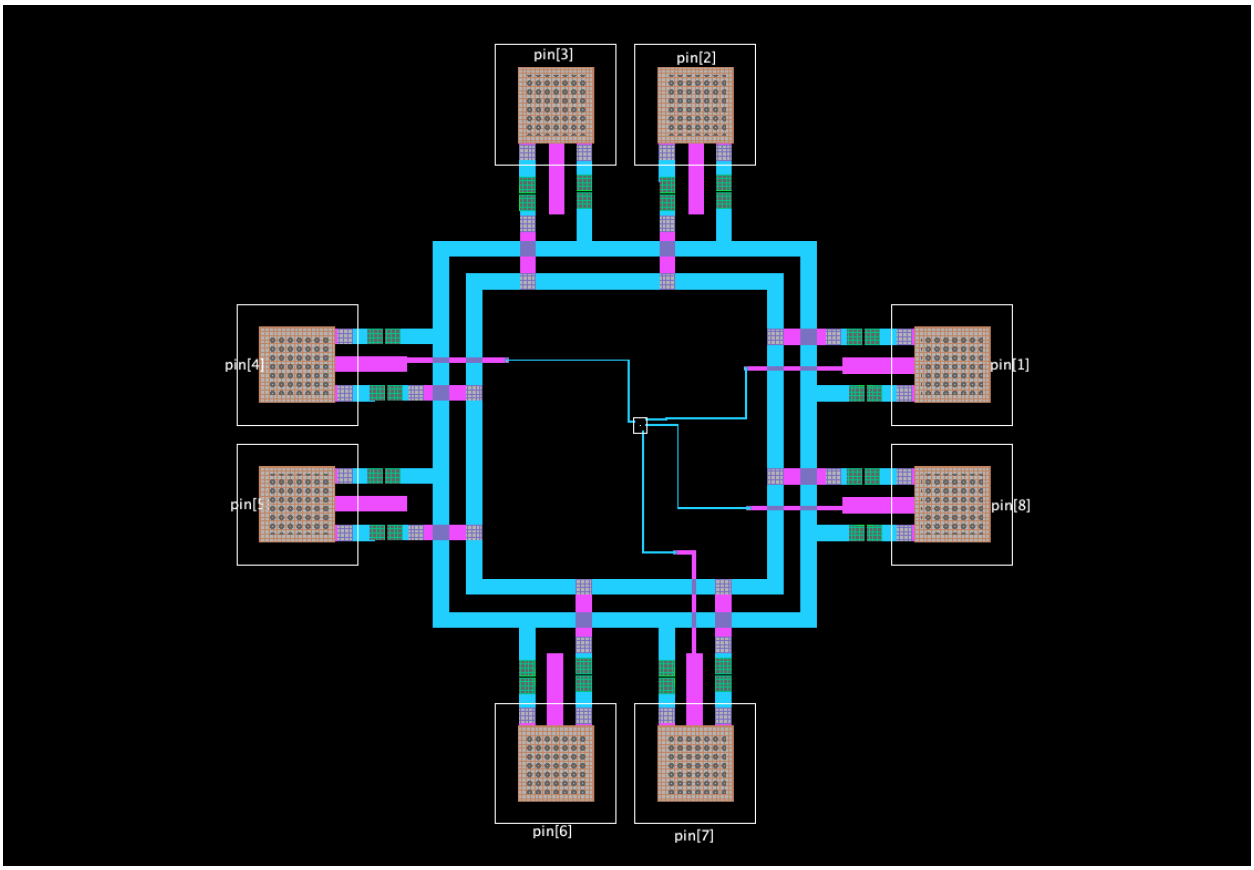
- The layout of the pad cell with the ESD protection



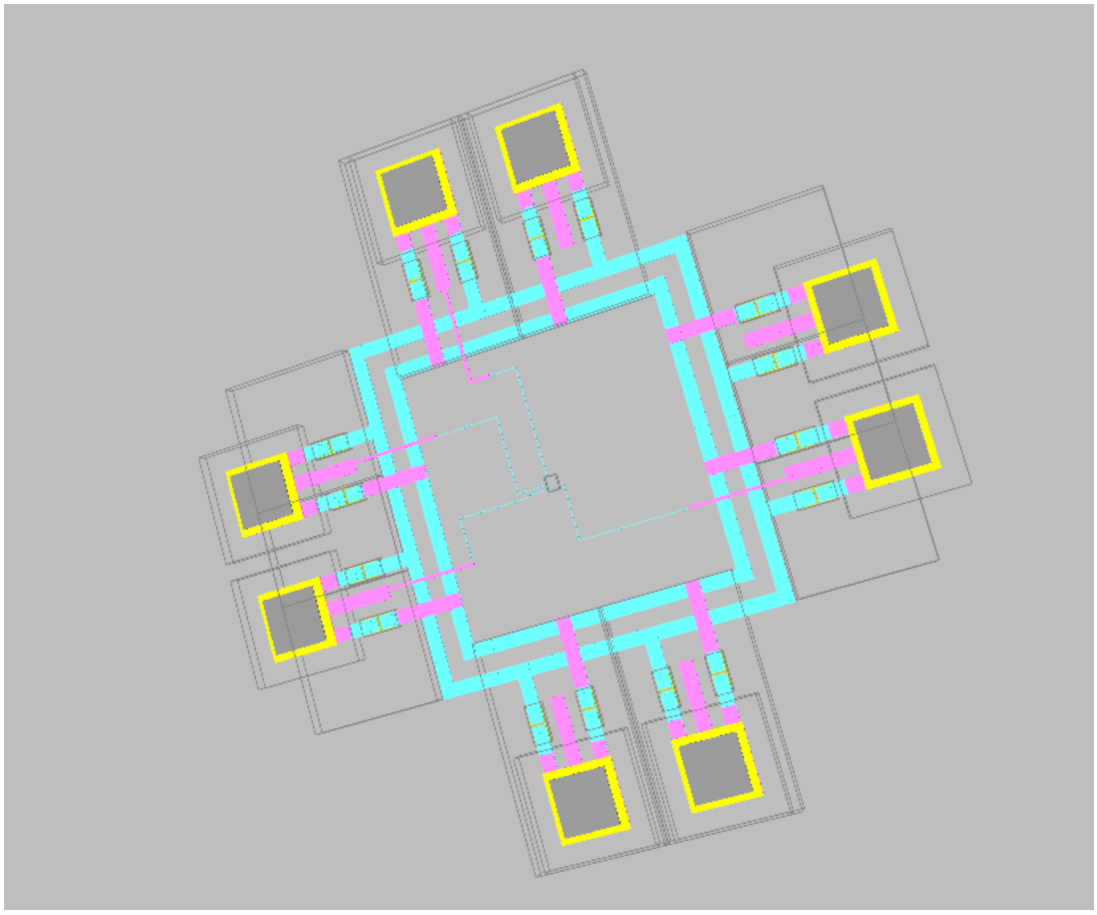
- 3D view of the pad cell with the ESD protection



- The layout of the padframe with the NMOS inside of it.



- 3D view of the padframe with the NMOS inside of it.



In the layout design, the key priority was to ensure both physical correctness under design rules and robustness of the overall padframe structure. The pWell–nActive and pActive–nWell diodes were laid out with sufficient diffusion area to handle expected ESD currents, and were surrounded by guard rings and tied wells/substrates to prevent latch-up and parasitic conduction. The pad cell layout incorporated these diodes adjacent to the pad diffusion, with metal routing chosen to minimize series resistance and ensure a low-impedance discharge path. Adequate spacing and contact density were maintained to satisfy design rule checks (DRC) and maximize current handling capability. The padframe was built as a symmetric square ring with continuous VDD and GND buses on each side to provide even power distribution and a clear return path for ESD currents. Corner cells were included where necessary to maintain bus continuity and satisfy padframe closure rules. The NMOS device was placed centrally within the padframe, with routing optimized to minimize parasitics and ensure straightforward connections from the transistor terminals to their respective pads. Overall, the layout decisions reflected a balance between compact design, compliance with process constraints, and the reliability required for safe operation under ESD stress.

Conclusion:

In conclusion, this lab was a challenging but valuable exercise that required careful attention to both schematic and layout design. Implementing the padframe with basic ESD protection involved multiple steps, creating and verifying diodes, pad cells, and the final integrated frame around the NMOS, each of which demanded significant effort and precision. While the workload was substantial, the process provided a deeper understanding of how padframes and ESD networks are integrated into real chip designs, and highlighted the importance of balancing functionality, reliability, and design-rule compliance in VLSI implementation.