UNIVERSITY of DENVER

Lab 1: Directions

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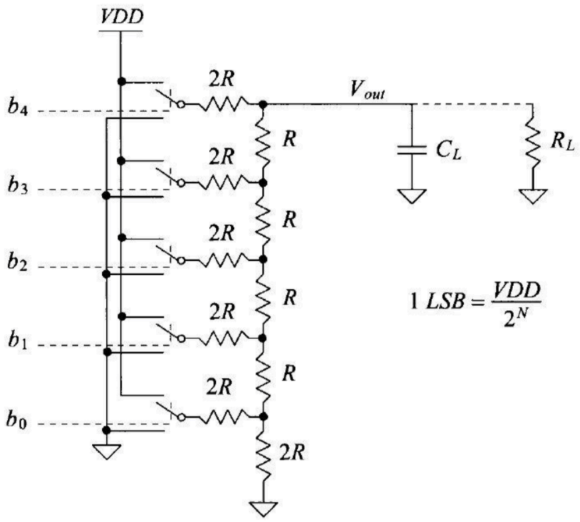
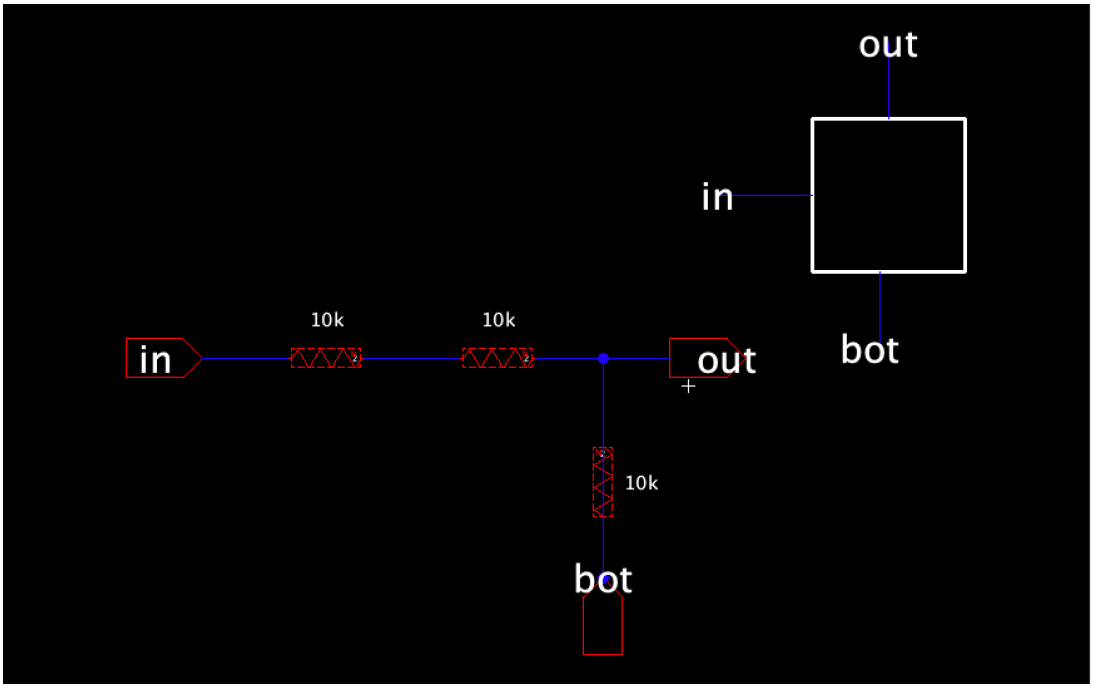
Introduction:

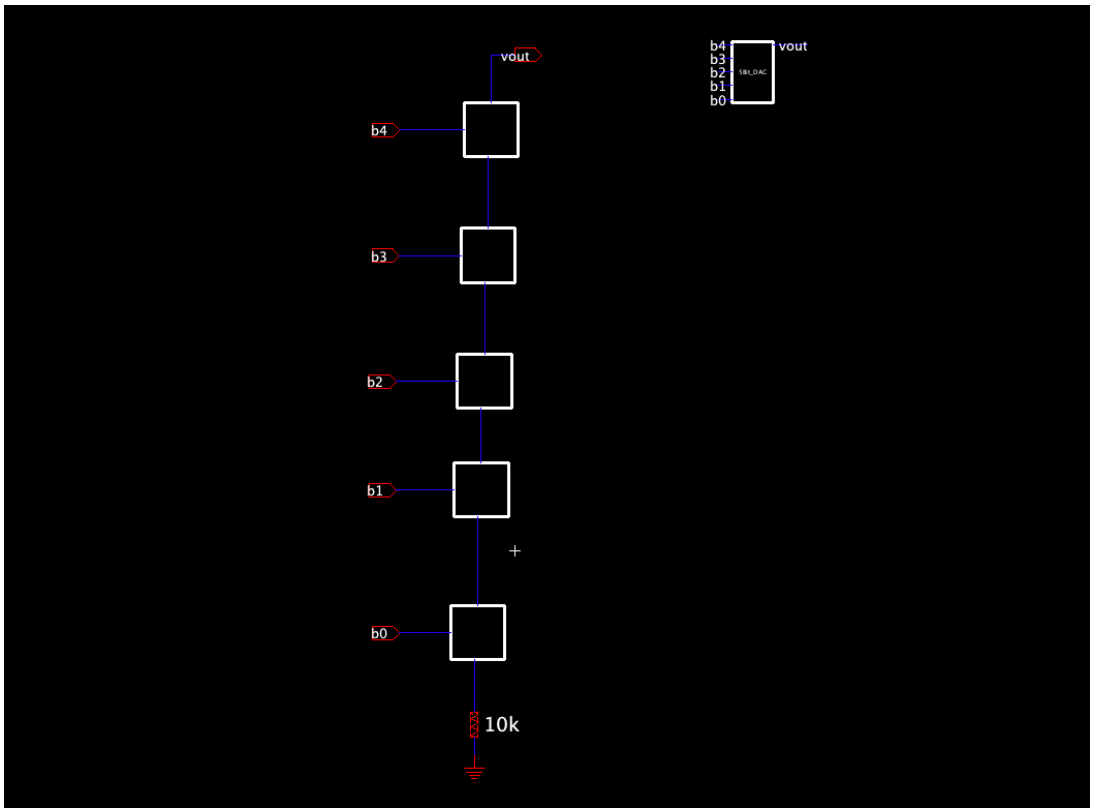
In this lab, a 5-bit R-2R ladder digital-to-analog converter (DAC) is designed and analyzed using n-well resistors. The objective is to understand the operation of an R-2R ladder, calculate its output resistance, and evaluate its behavior when driving capacitive and resistive loads. The lab involves creating the schematic, predicting and simulating the delay for a 10 pF load, and verifying that the DAC produces correct output voltages for different digital inputs. In addition, the layout of the DAC is implemented using n-well resistors, with attention to proper geometry, parasitic effects, and verification through DRC and LVS checks.



Schematics:

The design of a 5-bit DAC using an n-well R of 10k. The 2R resistor are implemented with two separate 10k resistors in series.





Q) Find and explain how to determine the output resistance of the DAC.
Set all independent sources to zero (ground VDD and all bit inputs), then find the Thevenin resistance seen at Vout.

1. Start at the LSB (b0):
   Two 2R branches meet at b0 (one to ground, one to the b0 switch). With the source grounded, they're in parallel:
   $Req_1 = (2R \parallel 2R) = (2R \cdot 2R) / (2R + 2R) = 4R^2 / 4R = R$

2. Move to b1:
   Req_1 is in series with the interstage resistor $R \rightarrow R + Req_1 = R + R = 2R$
   That result is in parallel with the 2R branch at b1:
   $Req_2 = (2R \parallel 2R) = R$

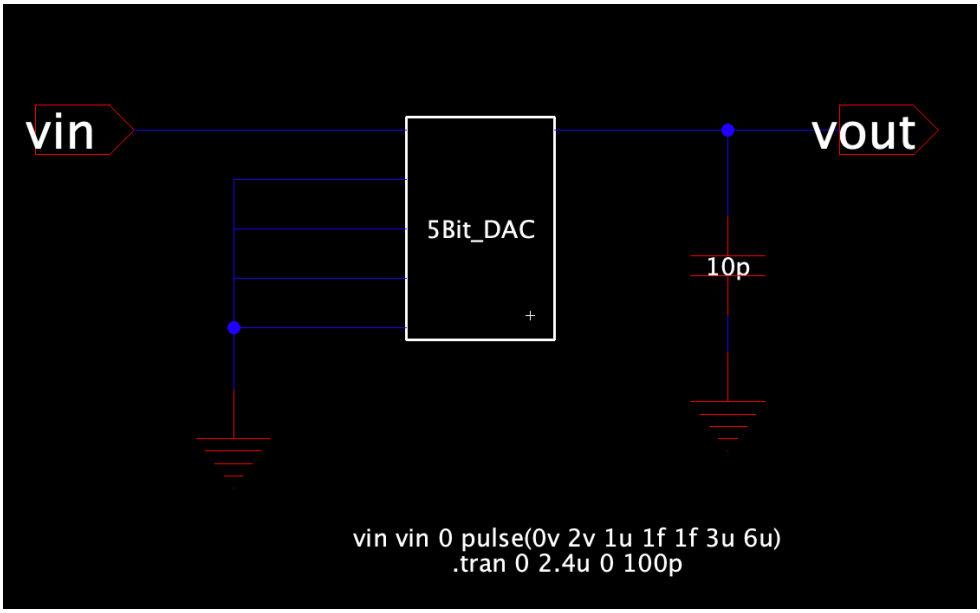
3. Repeat for each higher bit (pattern):
   At each node bn, the "look-back" toward the LSB simplifies to R. Adding the series R gives 2R, which in parallel with the local 2R collapses back to R. So from any bn toward the LSB, the equivalent is R.

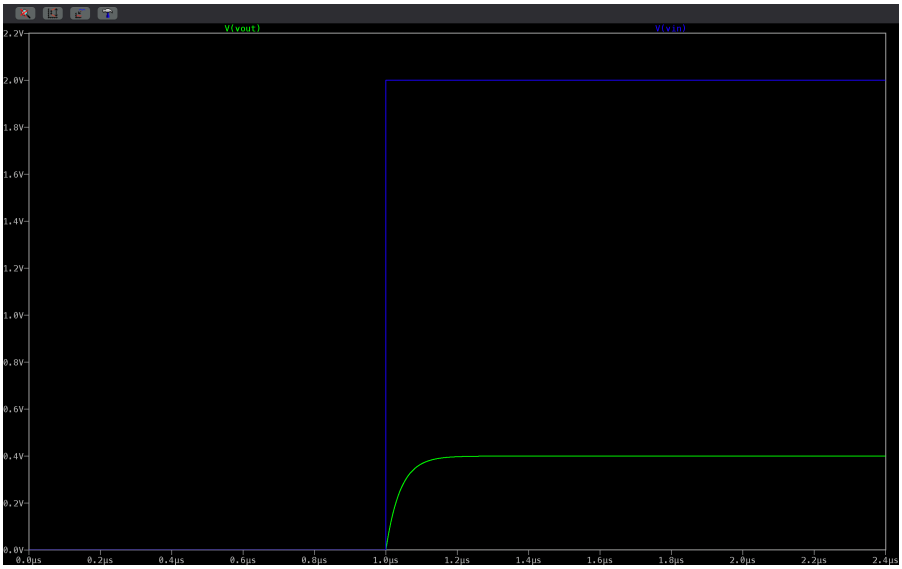
4. At the MSB (b4) and Vout:
   Looking from b4 toward the LSB → R. Add the final series R to Vout → 2R.
   This 2R is in parallel with the MSB's 2R branch:
   $Rout = (2R \parallel 2R) = (2R \cdot 2R) / (2R + 2R) = R$

Result: The R-2R ladder's output resistance is R (independent of input code). With R = 10 kΩ, Rout = 10 kΩ.

- Delay, driving a load

Ground all DAC inputs except B4. Connect B4 to a pulse source (0 to VDD) and show, and predict using 0.7RC, the delay the DAC has driving a 10pF load.





Verifying the simulation results match with hand calculations:

The figures above present the DAC simulation when driving a 10 pF load capacitor. A pulse ranging from 0 V to 2 V is applied to Vin, while the remaining inputs are tied to ground. To

approximate the delay, the DAC output can be modeled as an RC circuit, with the delay estimated using the expression:

$t\_delay \approx 0.7 \times Rout \times CL$

where Rout is the DAC's output resistance and CL is the external capacitance.

In this case, Rout = 10 kΩ and CL = 10 pF. Substituting these values gives:

$t\_delay \approx 0.7 \times (10 \times 10^{3}\ \Omega) \times (10 \times 10^{-12}\ F)$
$t\_delay \approx 0.7 \times 10^{-7}\ s$
$t\_delay \approx 70\ ns$

This means the output should take roughly 70 ns to rise to 50% of its final value. With VDD = 2 V, the expected steady-state output is:

$Vfinal = (16 / 2^{5}) \times VDD = 0.5 \times 2\ V = 1\ V$

The simulation confirms this prediction. The output voltage settles at 1 V, and the delay can be observed by measuring the time it takes for the output to reach 0.5 V. The input pulse begins at t = 1.0 μs, and the output crosses 0.5 V at about t = 1.07 μs. Therefore:

$tsimulated = 1.07\ \mu s - 1.0\ \mu s = 0.07\ \mu s = 70\ ns$

This simulated delay aligns perfectly with the theoretical calculation.

- Simulations to verify your design functions correctly

Applying different values to the input of the DAC and check if the output has the correct voltage.

To verify proper functionality of the 5-bit DAC (as required by the lab), simulations were carried out using different digital input codes and compared against theoretical expectations. For an R-2R DAC, the output voltage is defined by:

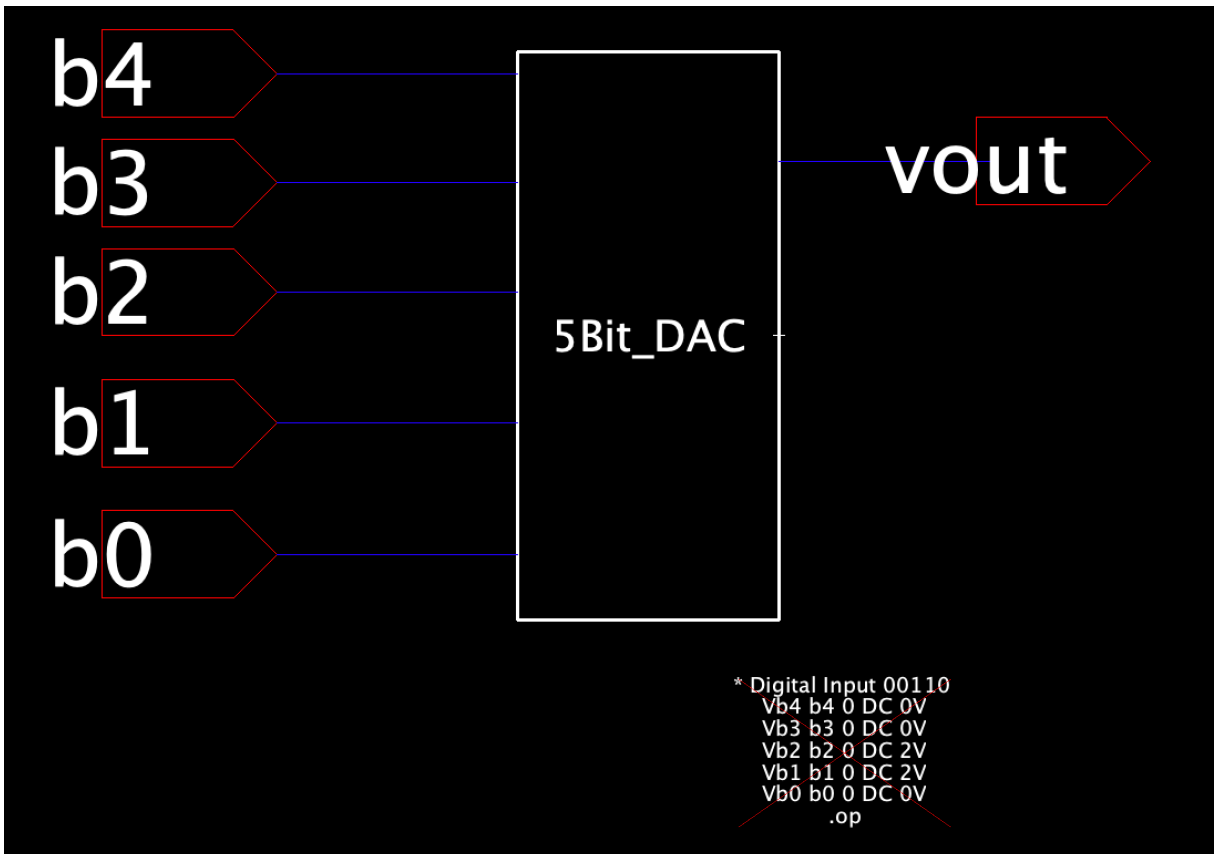
$Vout = (Input\ Decimal\ Value / 2^{N}) \times VDD$

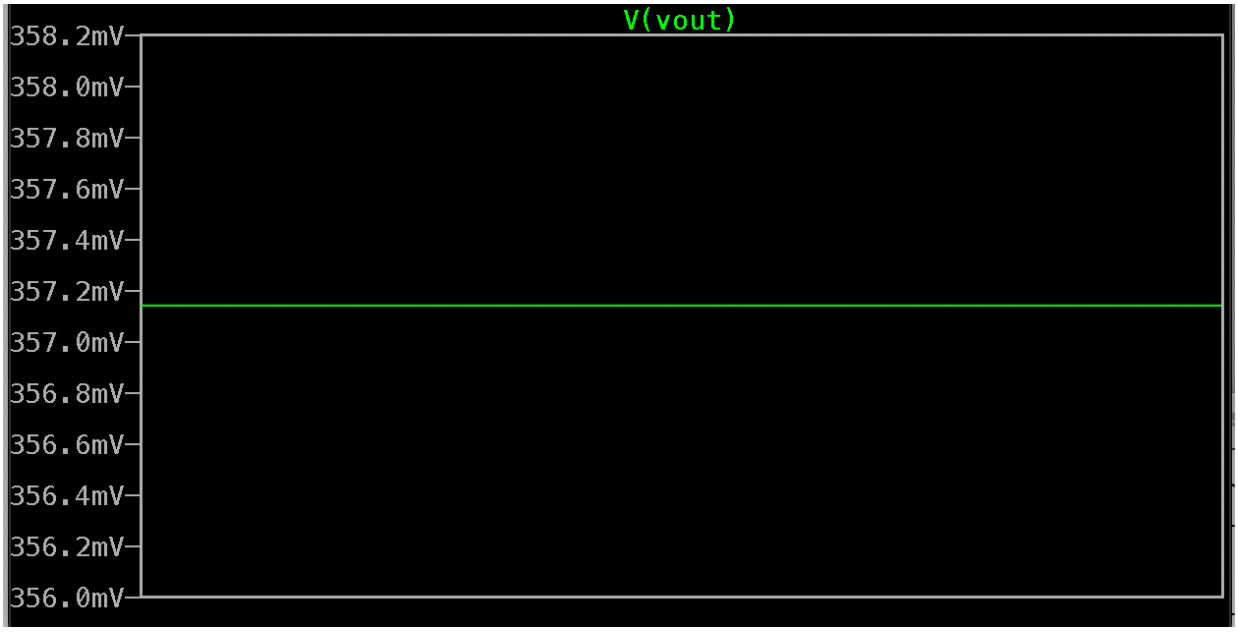
where N is the number of bits (N = 5 in this case) and VDD = 2 V.

As an example, for the input code **00110**, the decimal equivalent is 6. Substituting into the formula gives:

$Vout = (6 / 32) \times 2 = 0.375\ V$

The simulated output for this case was approximately 375 mV, which closely matches the theoretical prediction and is well within an acceptable margin of error.

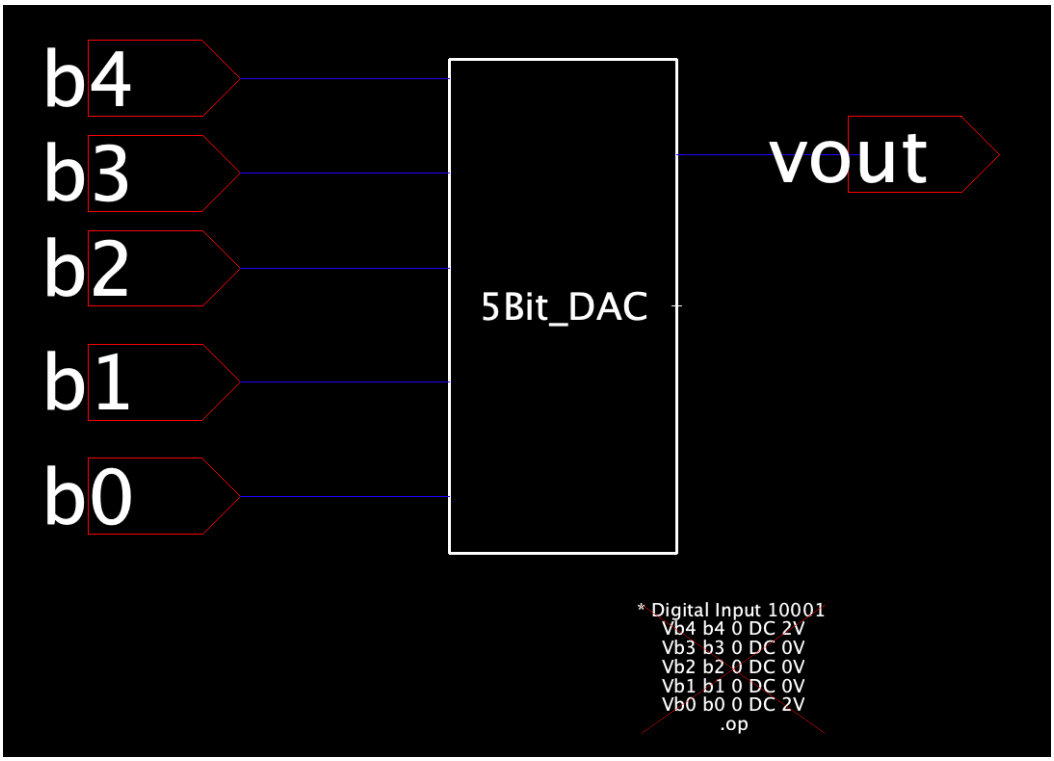


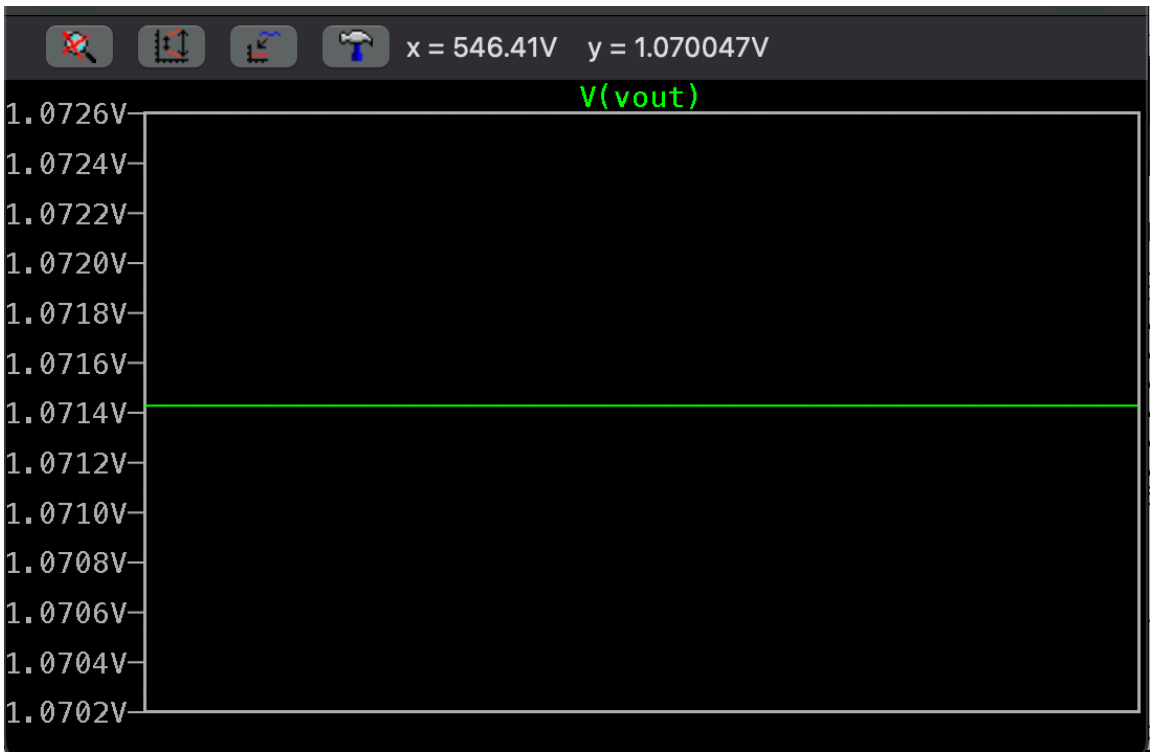


For the input code **10001**, the decimal equivalent is 17. Substituting into the formula gives:

Vout = (17 / 32) × 2 = 1.0625 V

In simulation, the DAC output was measured at approximately **1.07142 V**, which is in close agreement with the theoretical result and demonstrates the expected linearity of the R-2R ladder.

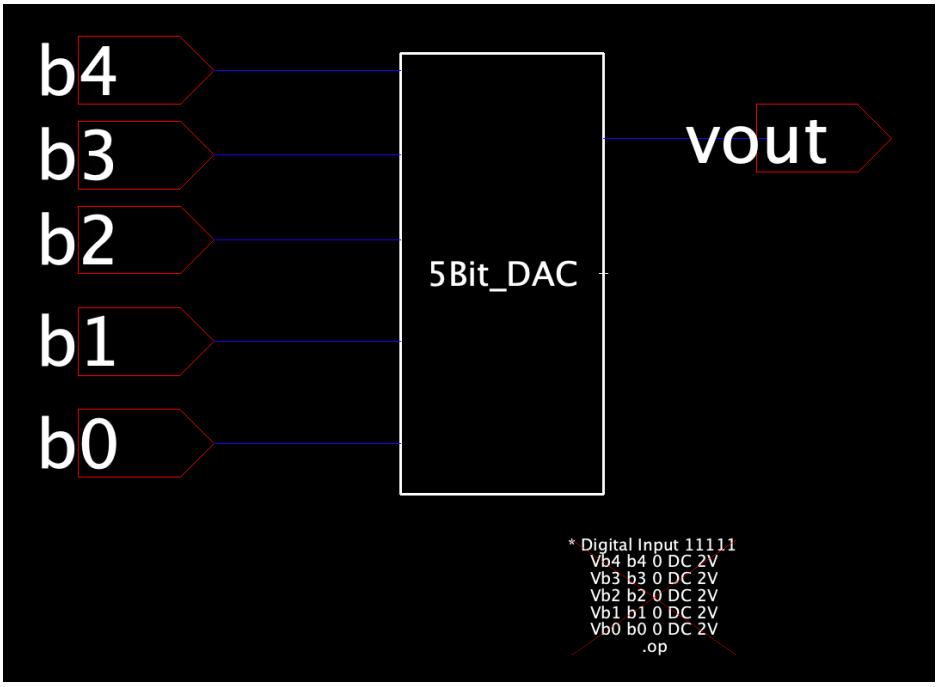


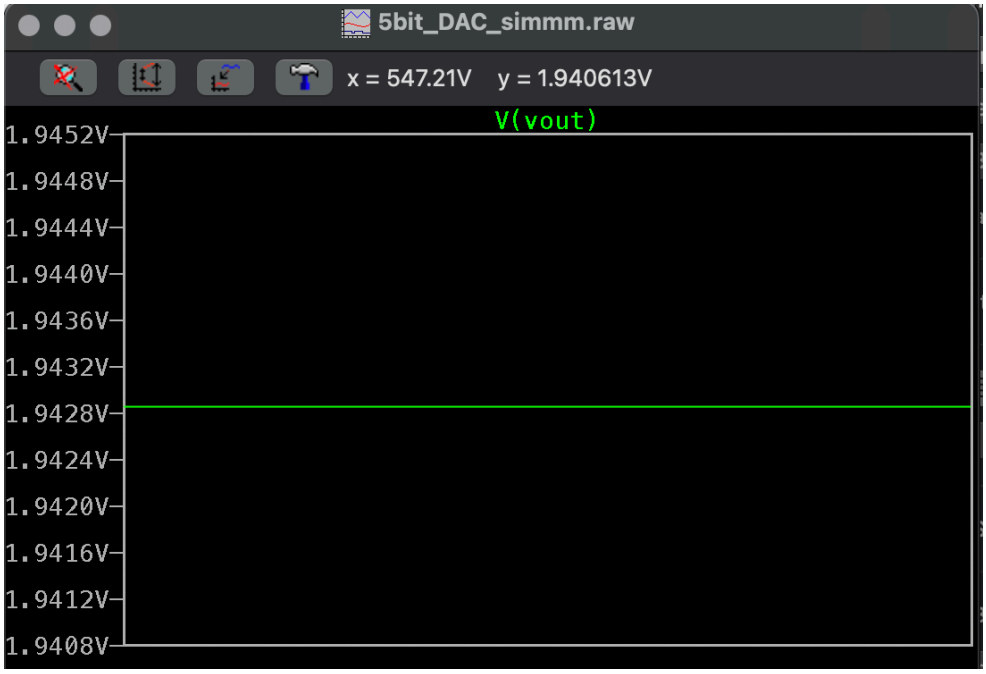


For the input code **11111**, the decimal equivalent is 31. Substituting into the equation gives:

Vout = (31 / 32) × 2 = 1.9375 V

In simulation, the measured output should be close to **1.943 V**, confirming that the DAC approaches but does not quite reach the full supply voltage, which is expected behavior for an R-2R ladder.





Explain what happens if the DAC drives a 10k load

When the DAC output is connected to a 10 kΩ resistive load, its behavior is impacted by the DAC's internal output resistance, which is also 10 kΩ. Together, the internal resistance and the external load form a simple voltage divider.

The DAC can be modeled as an ideal voltage source (Vunloaded) in series with Rout. The actual voltage delivered to the load (Vloaded) is then given by:

$$V_{loaded} = V_{unloaded} \times (R_L / (R_{out} + R_L))$$

With Rout = 10 kΩ and RL = 10 kΩ:

$$V_{loaded} = V_{unloaded} \times (10\ k\Omega / (10\ k\Omega + 10\ k\Omega))$$
$$V_{loaded} = V_{unloaded} \times (10\ k\Omega / 20\ k\Omega)$$
$$V_{loaded} = V_{unloaded} \times 0.5$$

This shows that the output voltage is cut in half compared to the unloaded case.

In practice, this is problematic because it reduces the accuracy of the DAC output and introduces distortion. Ideally, a DAC should drive loads without significantly altering the voltage it produces, but with a load comparable to its output resistance, the output level is no longer reliable. This highlights the importance of using a buffer or ensuring that the load resistance is much larger than the DAC's output resistance.

Layout:

Using the n-well to layout a 10k resistor

The resistance of an n-well resistor is given by the formula:

$$R = R_s \times (L / W)$$

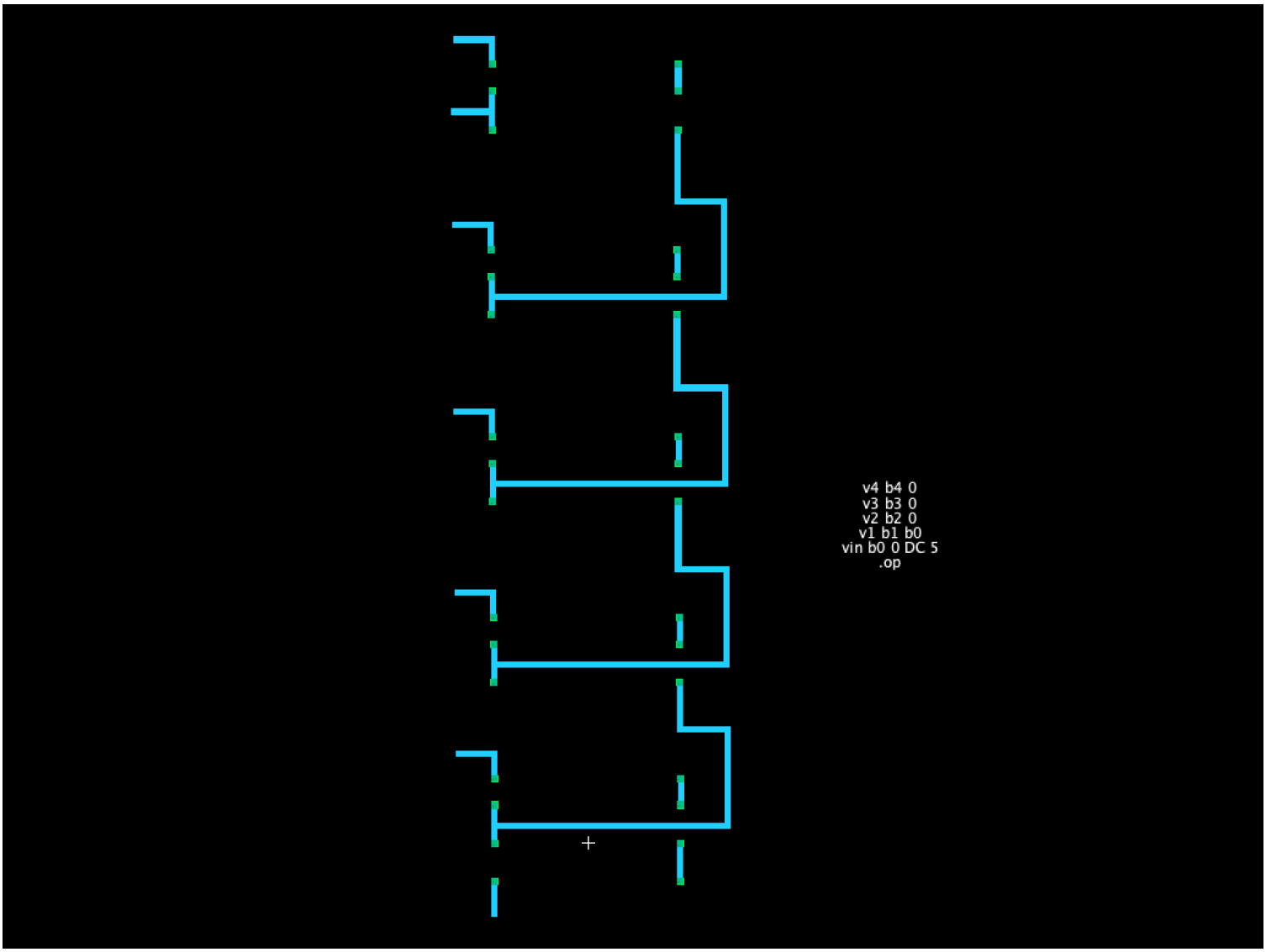
where R is the target resistance, Rs is the sheet resistance, L is the length, and W is the width. In this case, R = 10,000 Ω and Rs = 855 Ω/square. Choosing a width of 12 μm, the equation becomes:

$$10{,}000 = 855 \times (L / 12)$$

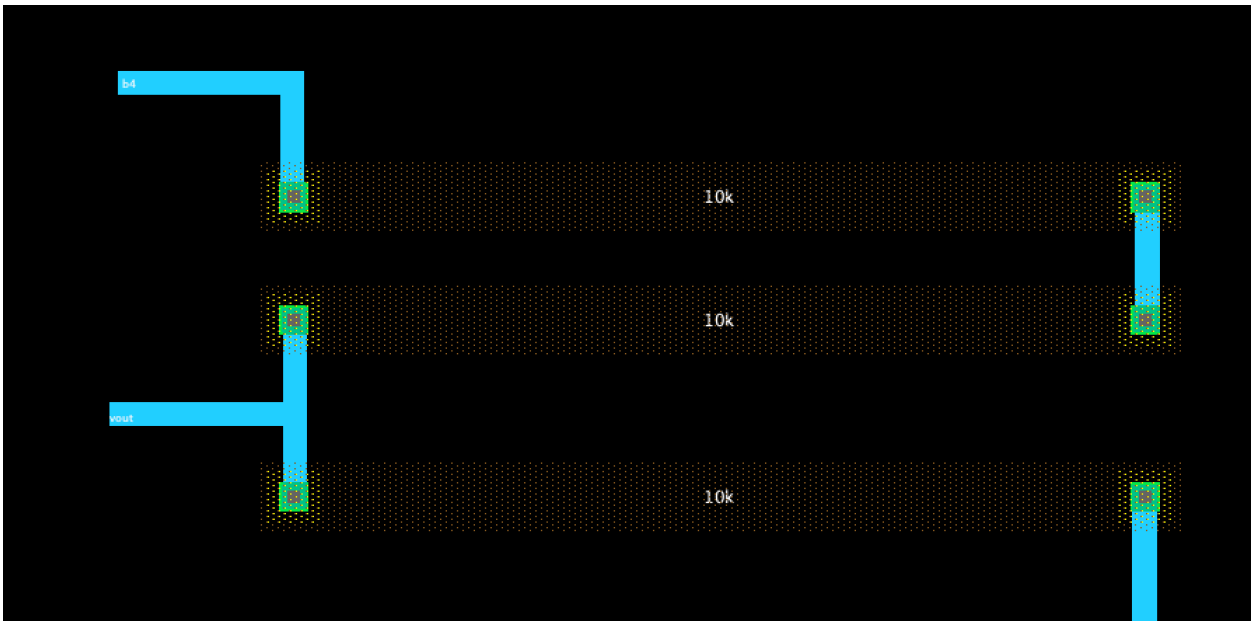
$$L = (10{,}000 \times 12) / 855 = 140.35\ \mu m$$

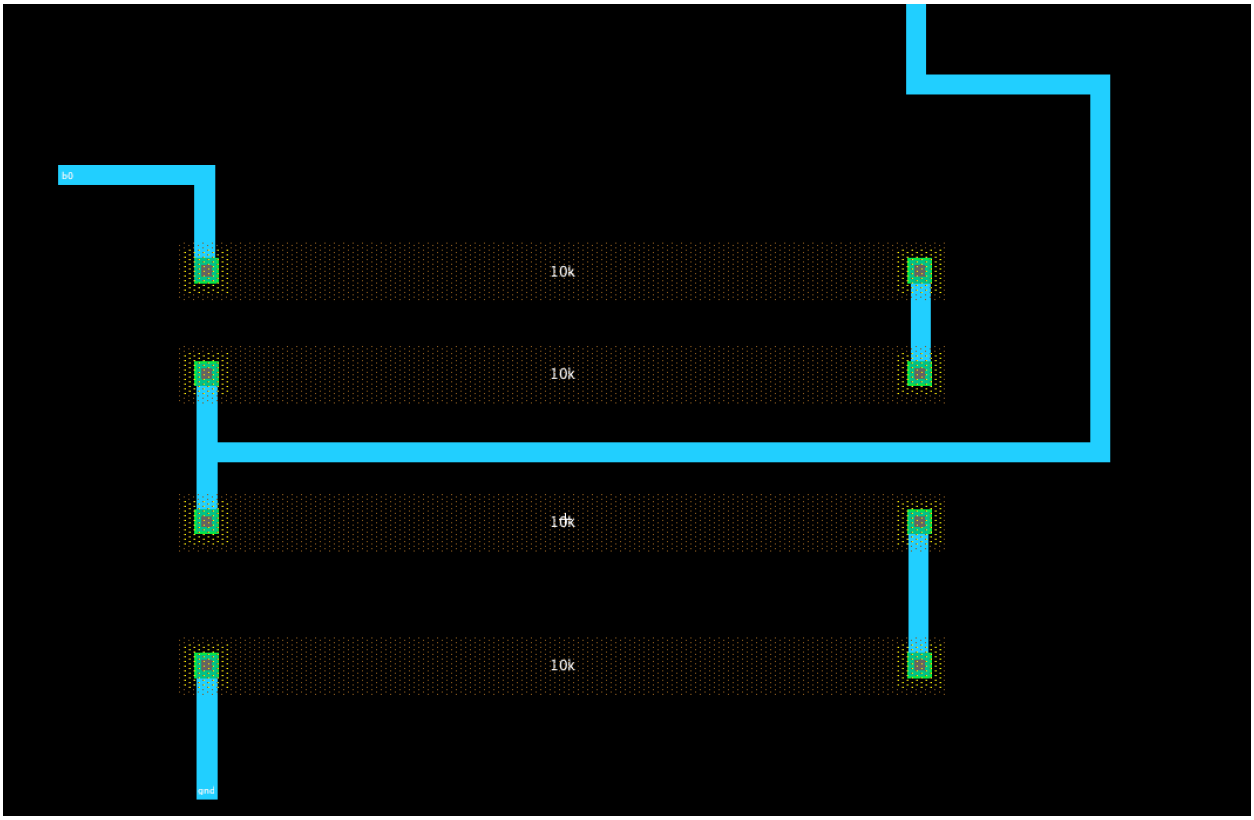
Therefore, using W = 12 μm and L = 140.35 μm produces a resistor of approximately 10 kΩ. This sizing was implemented in Electric VLSI successfully, and the extracted resistance matched the design target.

```
(Layout DRC):
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 18 networks
Checking cell `5Bit_DAC{lay}'
No errors/warnings found
0 errors and 0 warnings found (took 0.013 secs)
(Layout LVS):
Hierarchical NCC every cell in the design: cell `5Bit_DAC{sch}' cell `5Bit_DAC{lay}'
Comparing: Lab
1
_
_
DAC:5Bit_DAC{sch} with: Lab
1
_
_
DAC:5Bit_DAC{lay}
exports match, topologies match, sizes not checked in 0.084 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.089 seconds.
(Schematic DRC):
Checking schematic cell 'SingleCell{sch}'No errors found
Checking schematic cell `5Bit_DAC{sch}'
No errors found
Checking icon cell 'SingleCell;1{ic}'
No errors found
Checking icon cell `5Bit_DAC{ic}'
No errors found
0 errors and 0 warnings found (took 0.001 secs
```



Zoom in for a better view:





Conclusion:

This lab demonstrated the design, analysis, and layout of a 5-bit R-2R ladder DAC using n-well resistors. The output resistance was shown to be constant at 10 kΩ, and the predicted delay of 70 ns for a 10 pF load closely matched the simulation results. Simulations confirmed that the DAC produced the correct output voltages for various digital inputs, although slight deviations were observed when driving a resistive load due to the voltage divider effect. The layout exercise reinforced the importance of resistor geometry, grid alignment, and parasitic considerations, with final verification through DRC and LVS ensuring design correctness. Overall, the lab provided practical experience in both the theoretical and implementation aspects of mixed-signal circuit design.