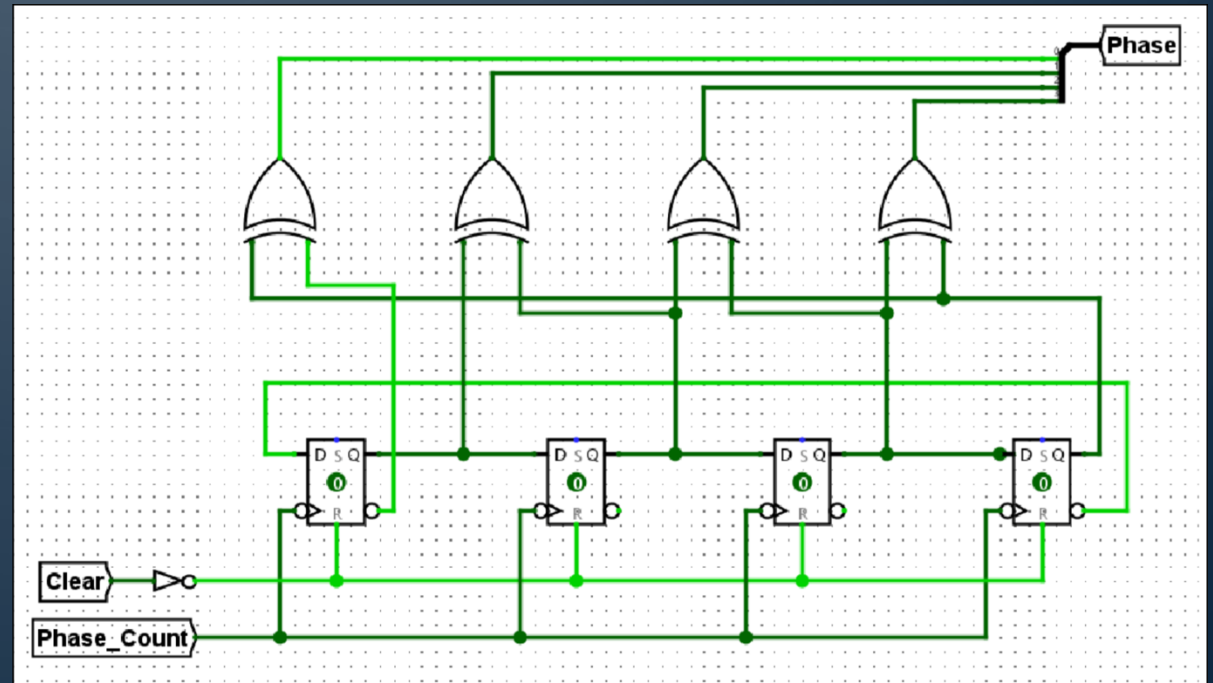


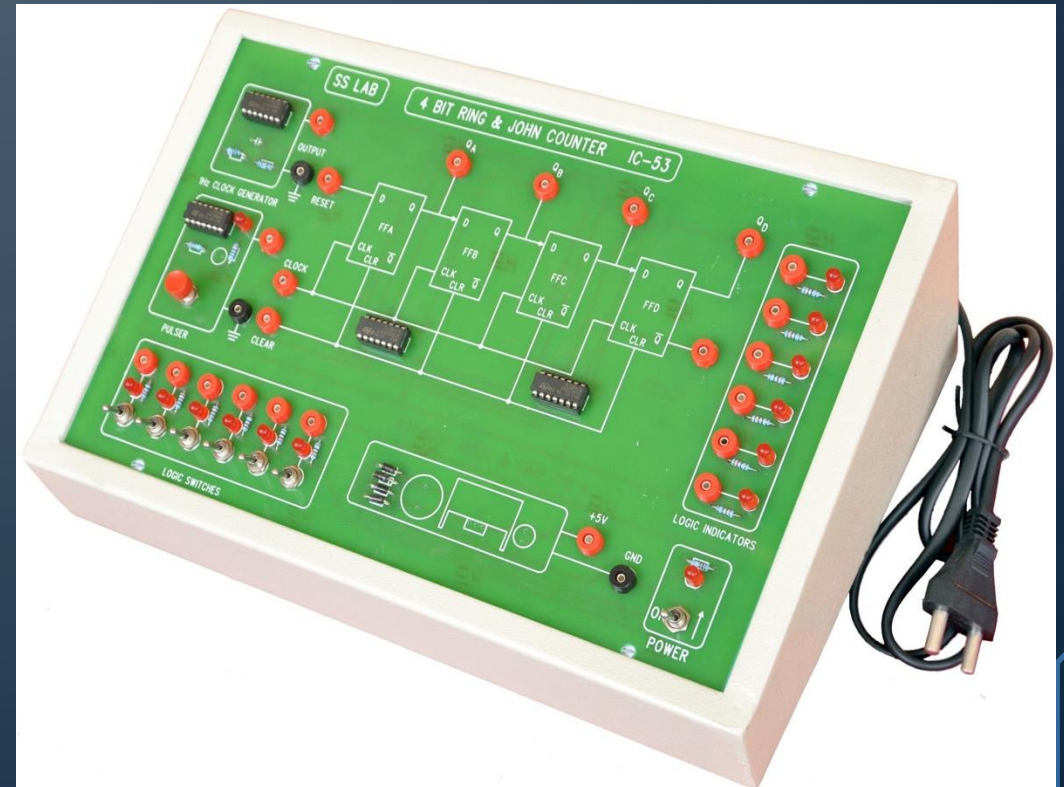
FINAL PROJECT: 4-BIT RING COUNTER

ABDULLAH BOHAMAD



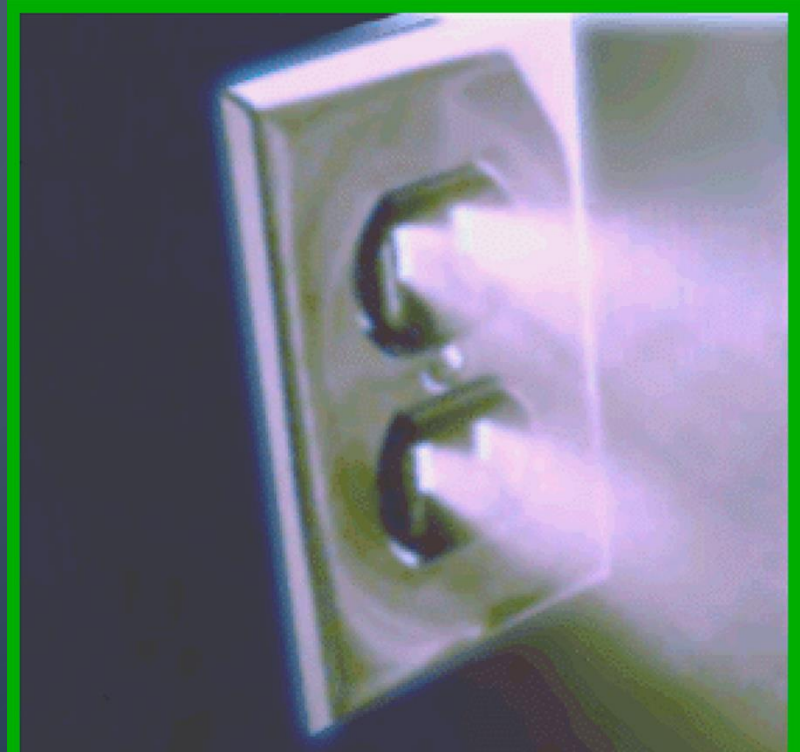
INTRODUCTION TO RING COUNTERS

- Digital counters used for timing/sequencing.
- Ring counter moves a single '1' through flip-flops.
- Applications: clocks, LED chasers, state machines.



TOOLS AND COMPONENTS

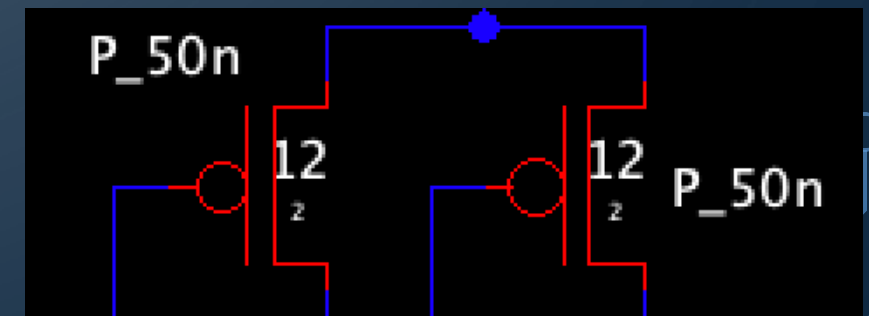
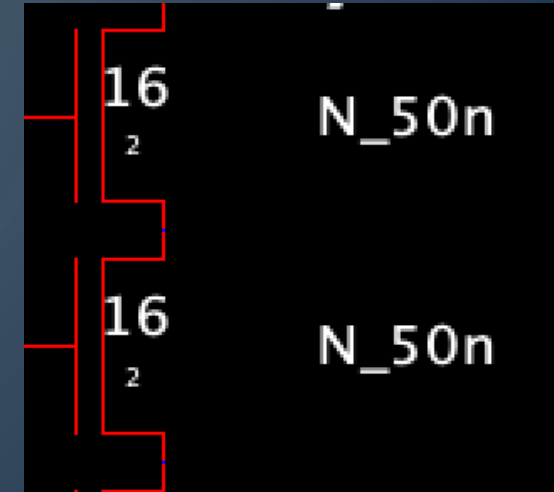
- Electric VLSI Design System.
- SPICE simulations.
- muddLib07 standard cell library.
- Custom D flip-flop required.



The Electric™
VLSI Design System
Version 9.08



ASSIGNING SPICE MODELS TO PMOS AND NMOS

- Used SPICE transistor models from muddLib07.
- **N_50n** → assigned to all NMOS devices.
- **P_50n** → assigned to all PMOS devices.
- Ensured accurate device behavior during simulation.

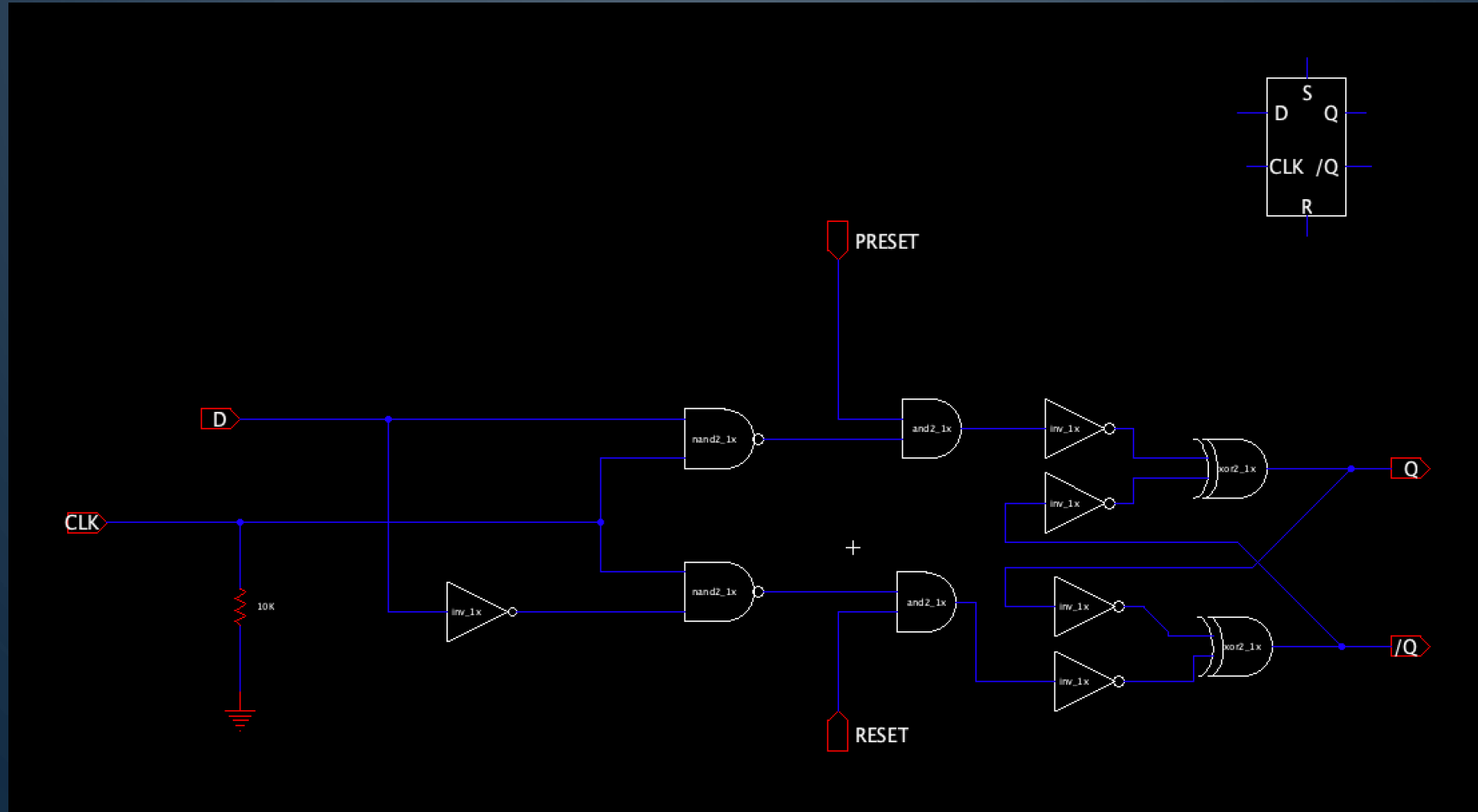




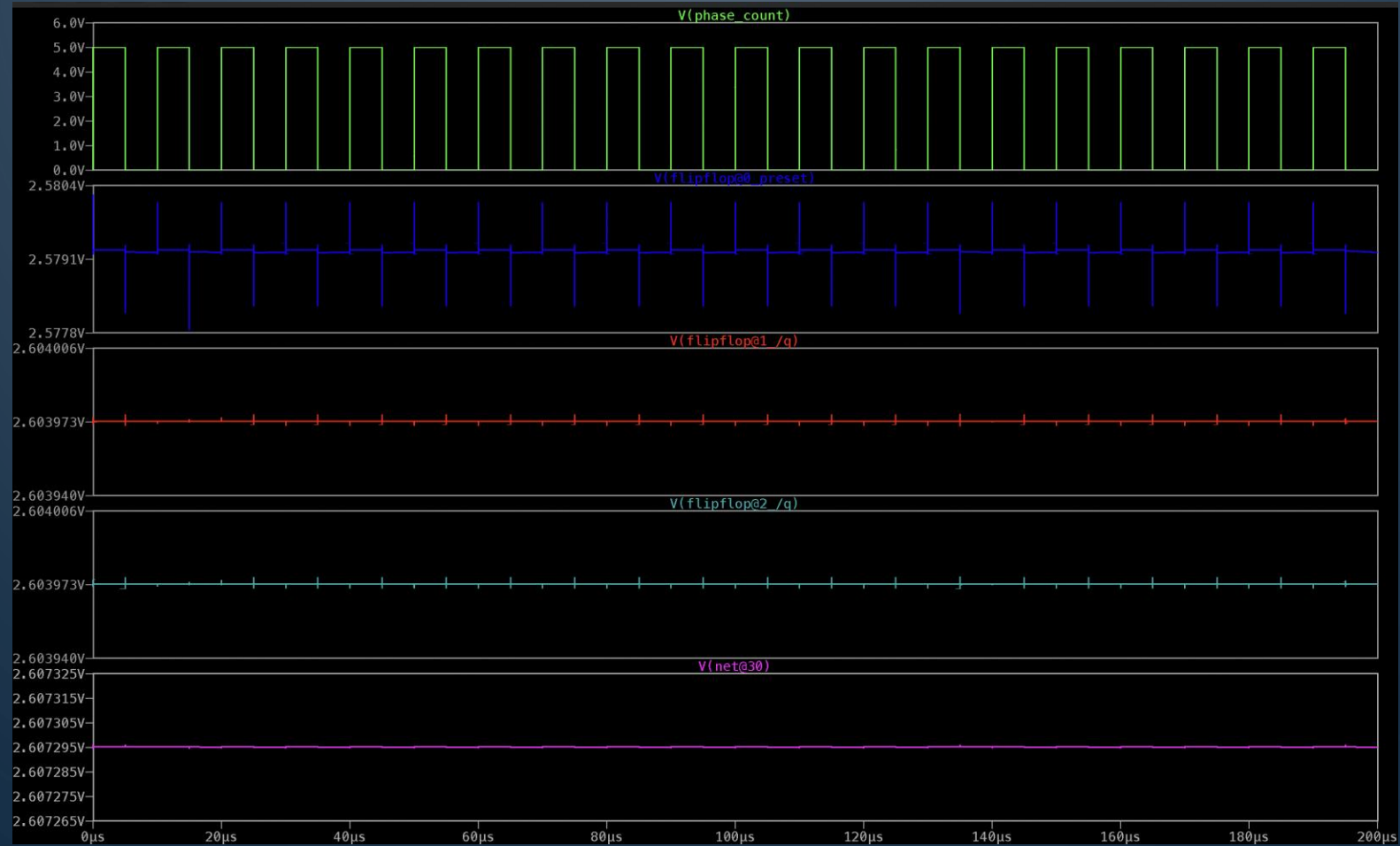
EARLY ATTEMPTS & **FAILURES**

- First custom flip-flop unstable.
 - Mid-level voltages around 2.6 V.
 - Incorrect preset/reset behavior.
 - Missing proper initialization.
- 
- 

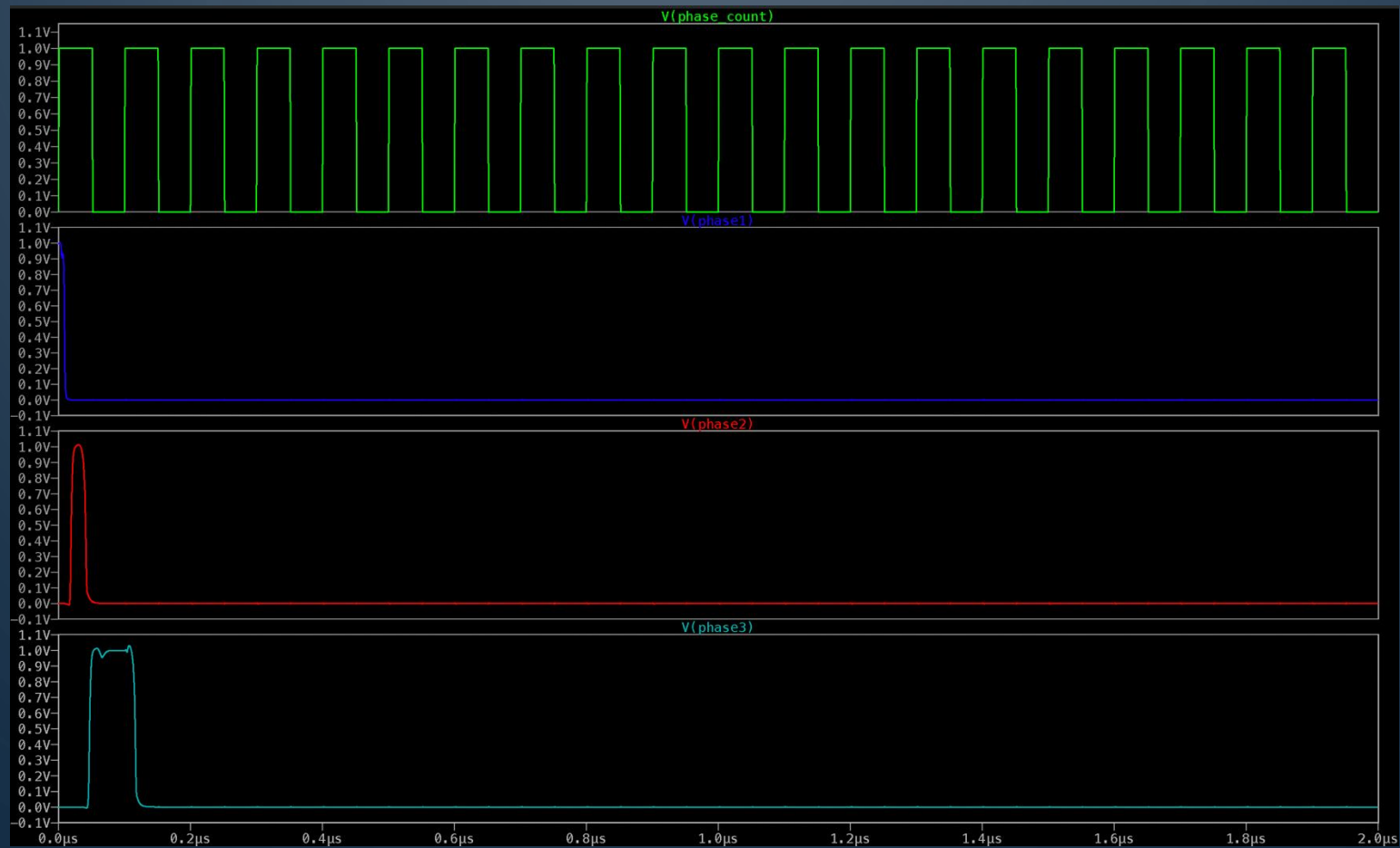
EARLY ATTEMPTS & FAILURES



EARLY ATTEMPTS & FAILURES



EARLY ATTEMPTS & FAILURES

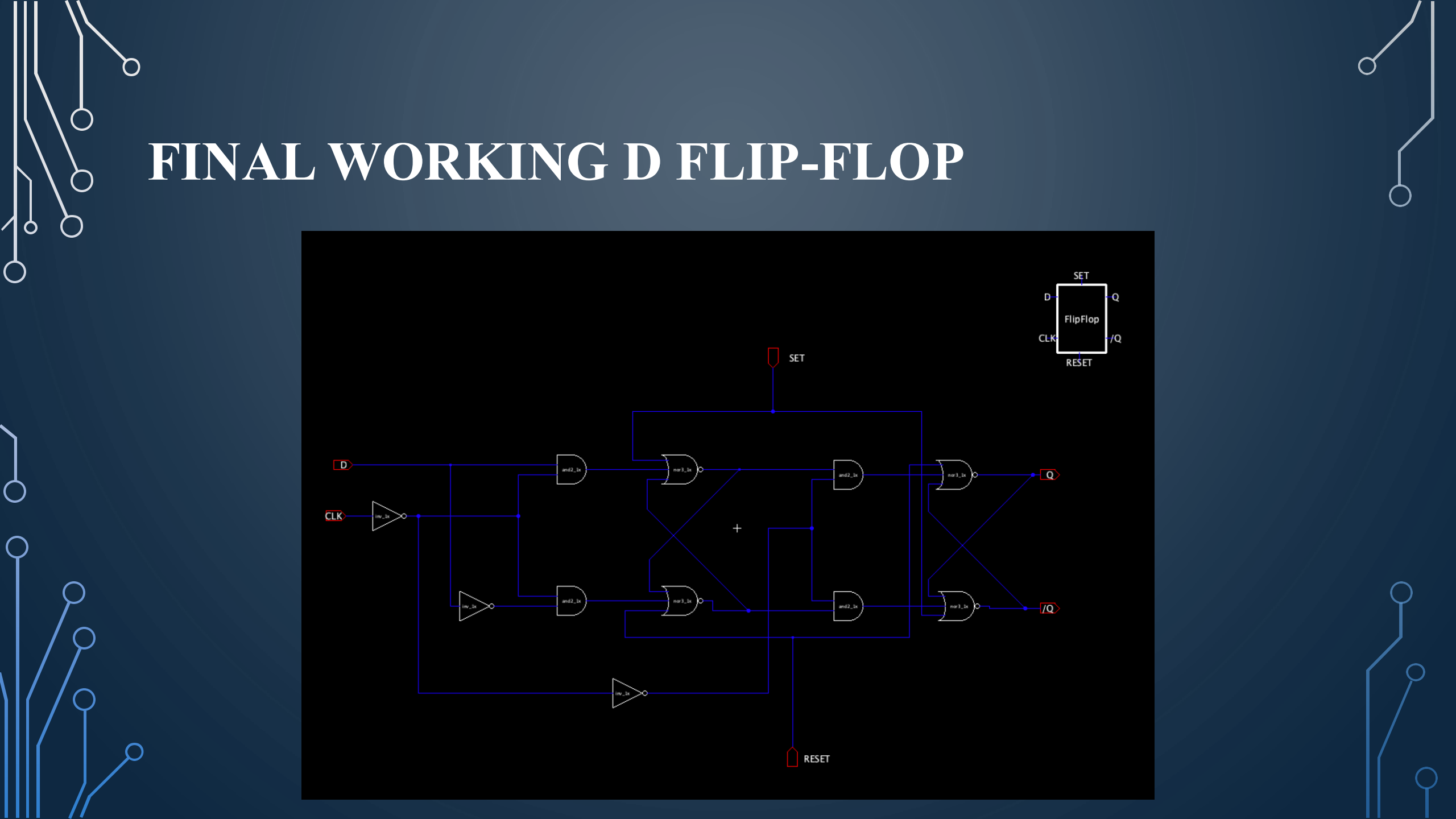


FINAL WORKING D FLIP-FLOP

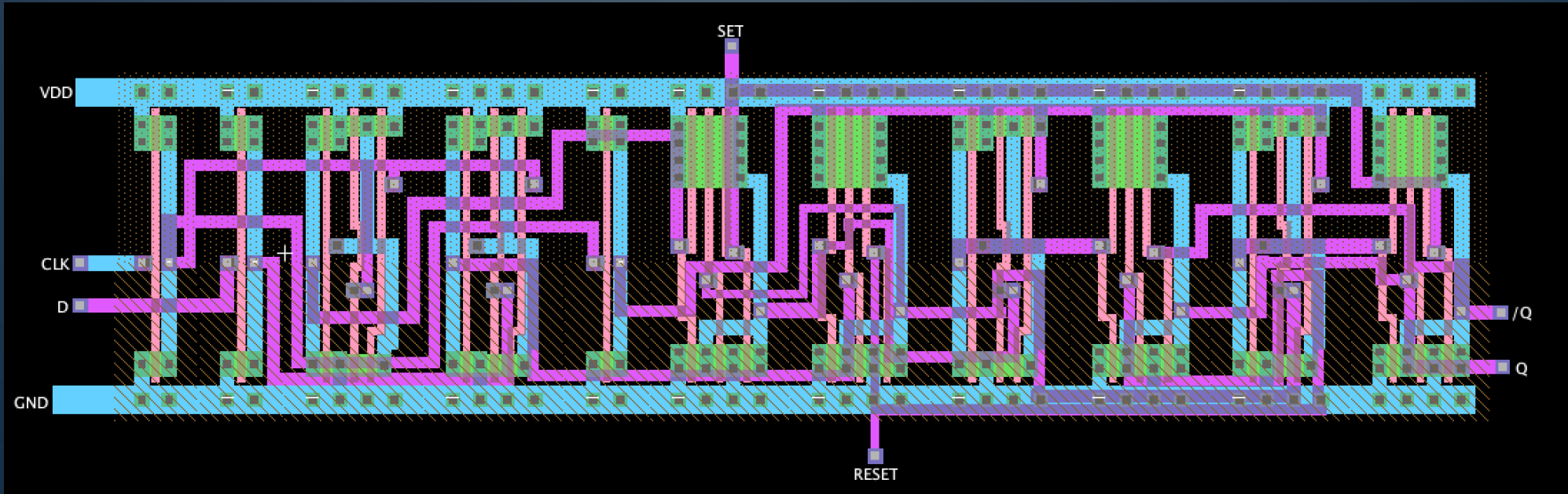
- Reorganized gating and feedback.
- Clock-controlled AND gates.
- Regenerative NOR latch.
- Clean Q and \bar{Q} outputs.

FINAL WORKING D FLIP-FLOP

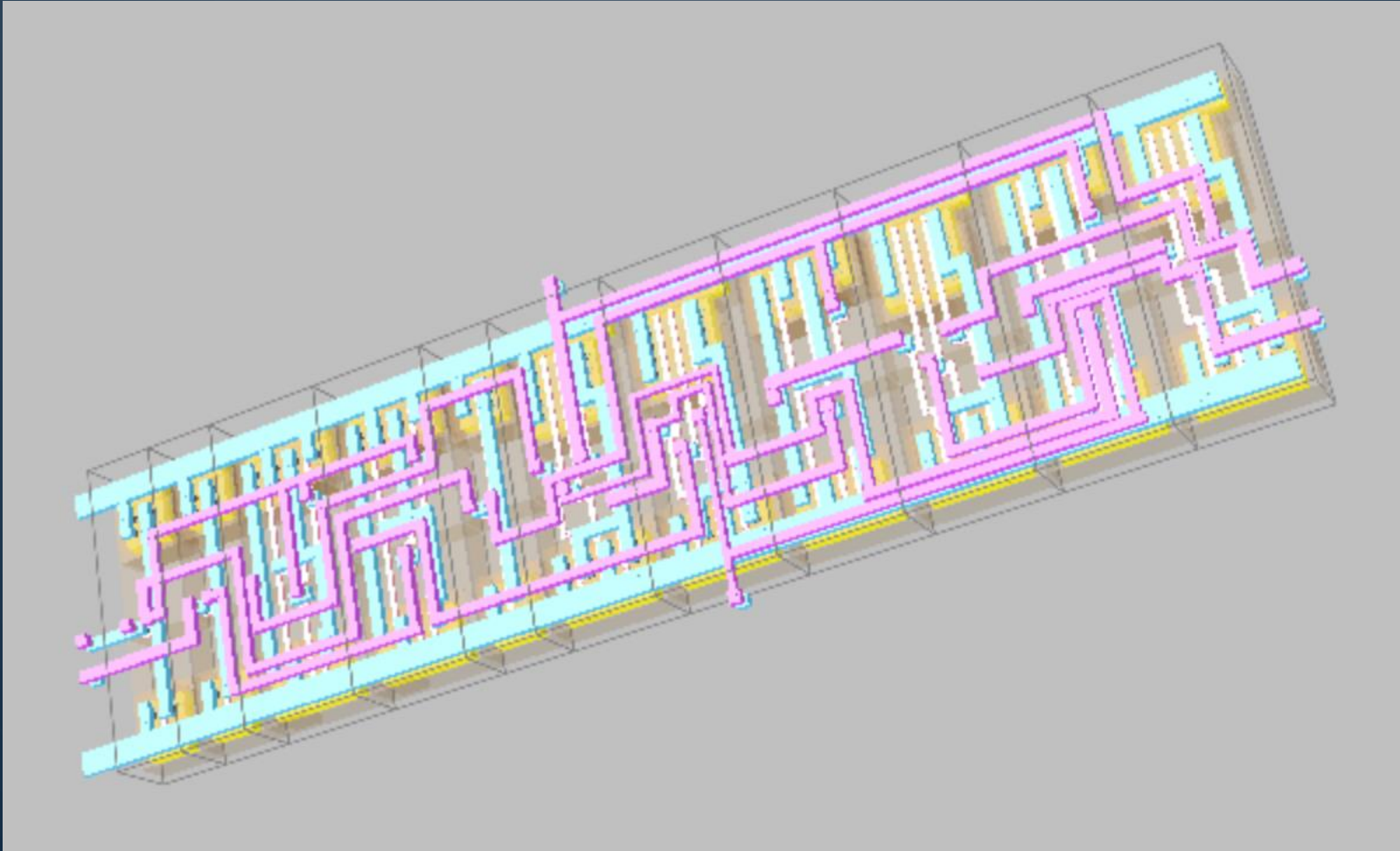
The diagram illustrates a final working D flip-flop circuit. It features a central logic block with a '+' symbol, representing an adder or a similar combinational logic element. The circuit includes several inputs: D, CLK, SET, and RESET. The D input is connected to the top input of the central block. The CLK input is connected to the clock input of the flip-flop. The SET and RESET inputs are connected to the set and reset inputs of the flip-flop. The circuit also includes several intermediate logic gates (AND, OR, NOT) and a final output stage that produces the Q and /Q signals. A legend in the top right corner identifies the flip-flop symbol and its inputs/outputs: SET, D, CLK, RESET, Q, and /Q.



FINAL WORKING D FLIP-FLOP



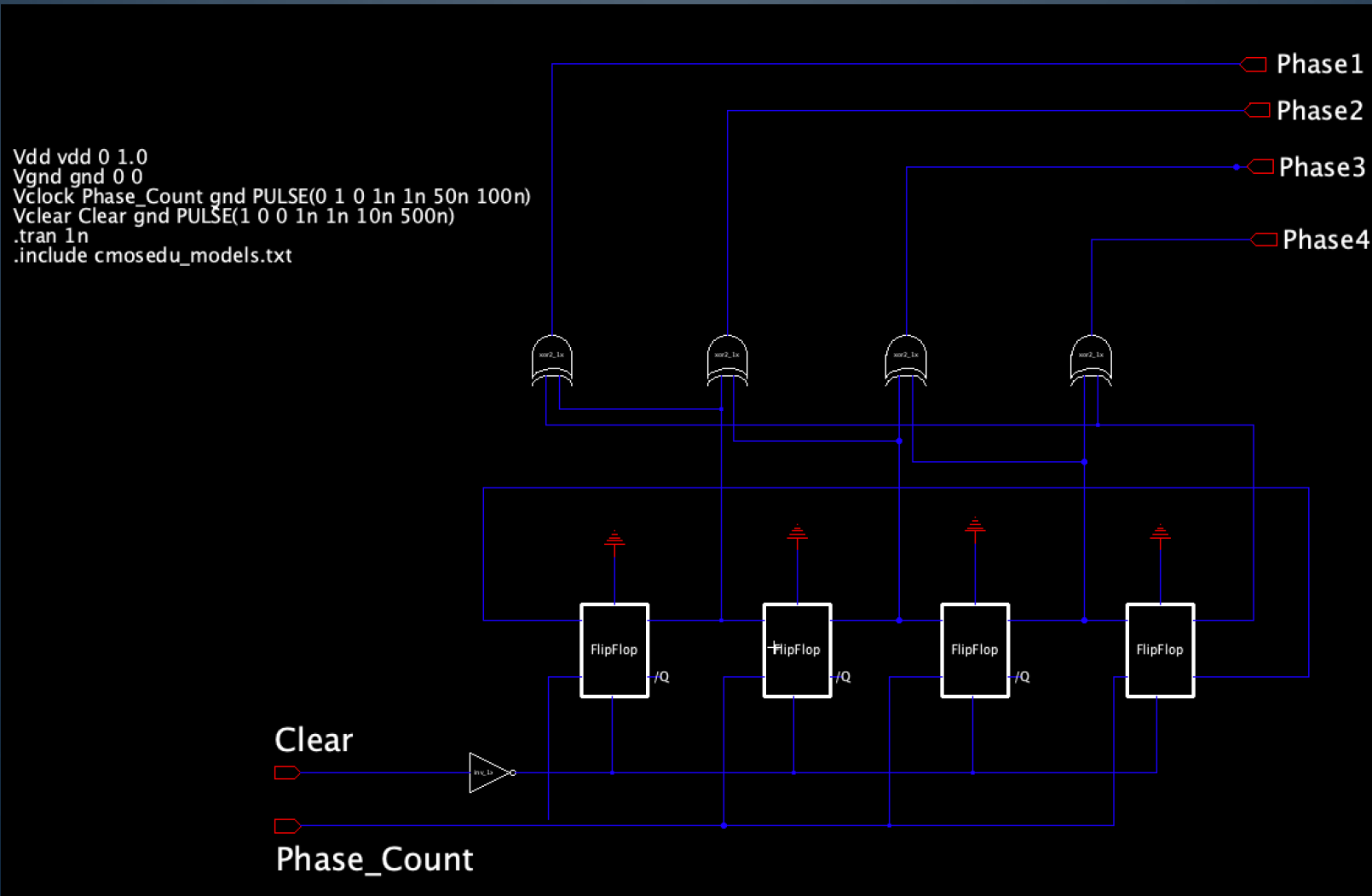
FINAL WORKING D FLIP-FLOP



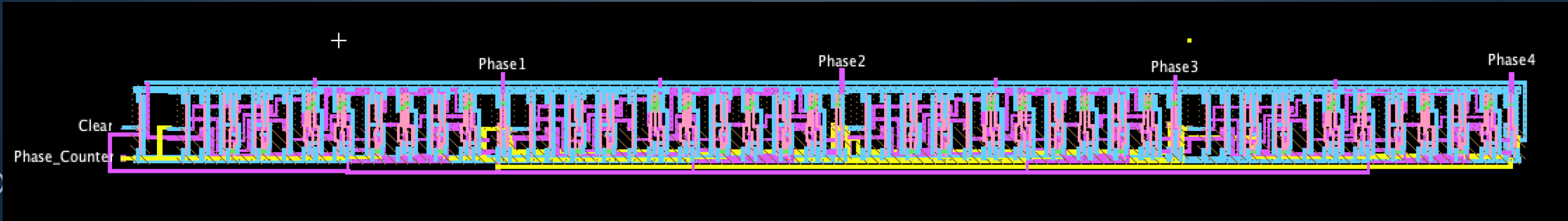
FINAL RING COUNTER OPERATION

- Four D-flip-flops in a ring.
- XOR-based transitions.
- Active-low Clear sets initial state.
- Waveforms show correct
Phase1→Phase2→Phase3→Phase4 sequence.

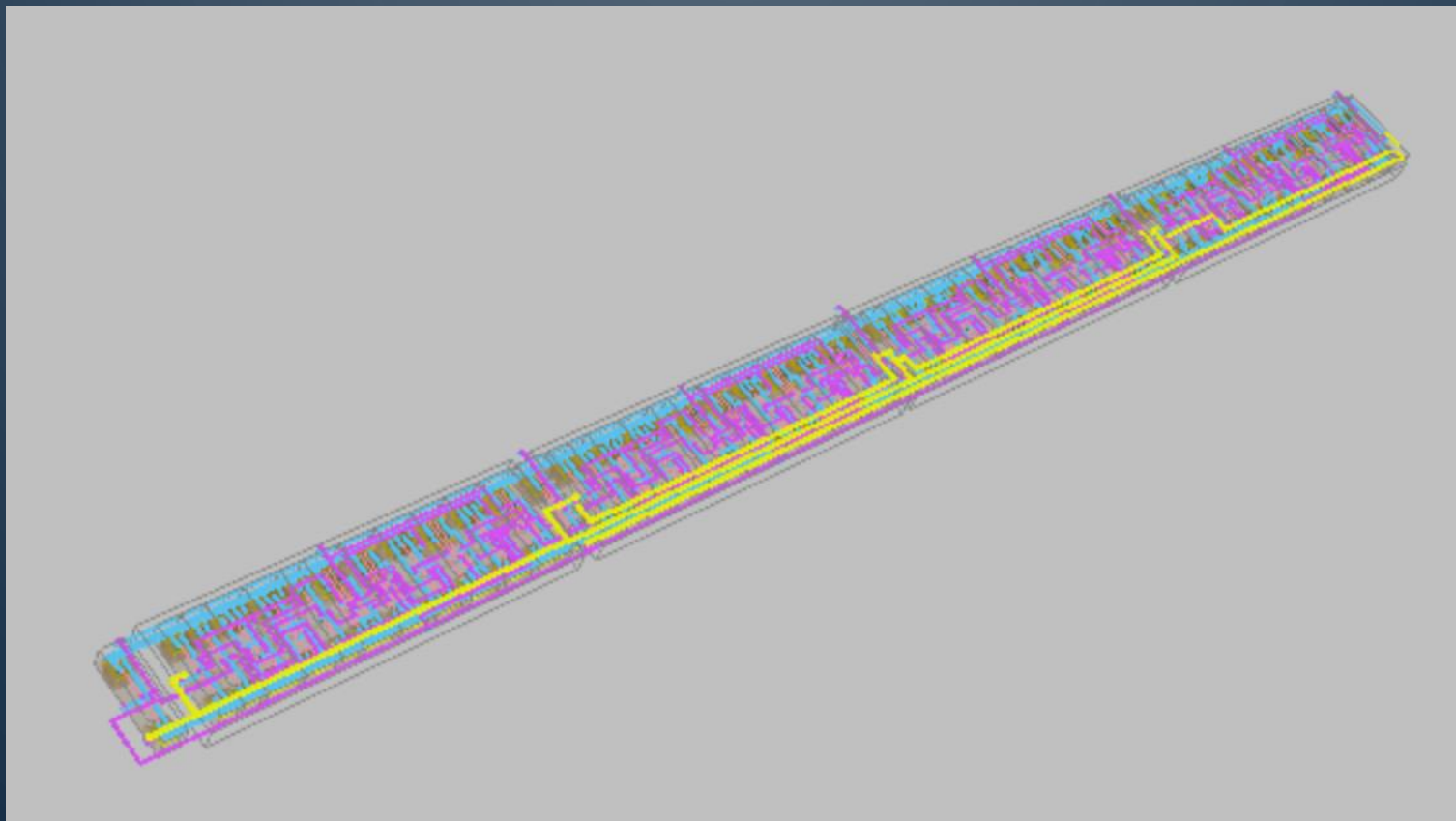
FINAL RING COUNTER OPERATION



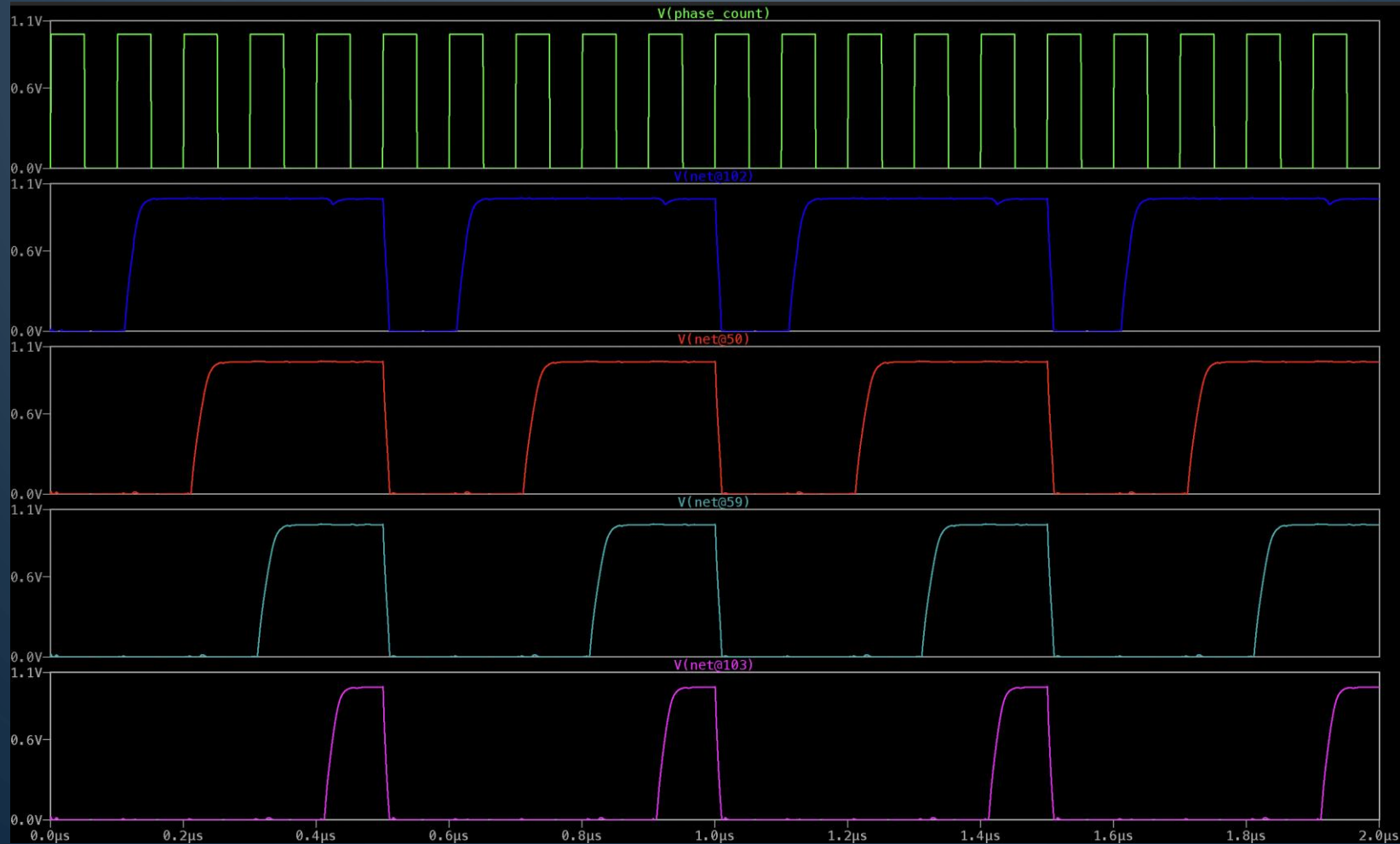
FINAL RING COUNTER OPERATION



FINAL RING COUNTER OPERATION



FINAL RING COUNTER OPERATION



A decorative graphic on the left side of the slide, consisting of white and light blue lines that resemble a circuit board or a stylized tree. The lines are vertical and horizontal, with small circles at the ends, creating a complex, branching pattern.

**THANK YOU FOR YOUR
ATTENTION!**