UNIVERSITY of DENVER

Lab 6: DC-to-DC Converter

Student : Abdullah Bohamad

Instructor: Dr Goncalo Martins

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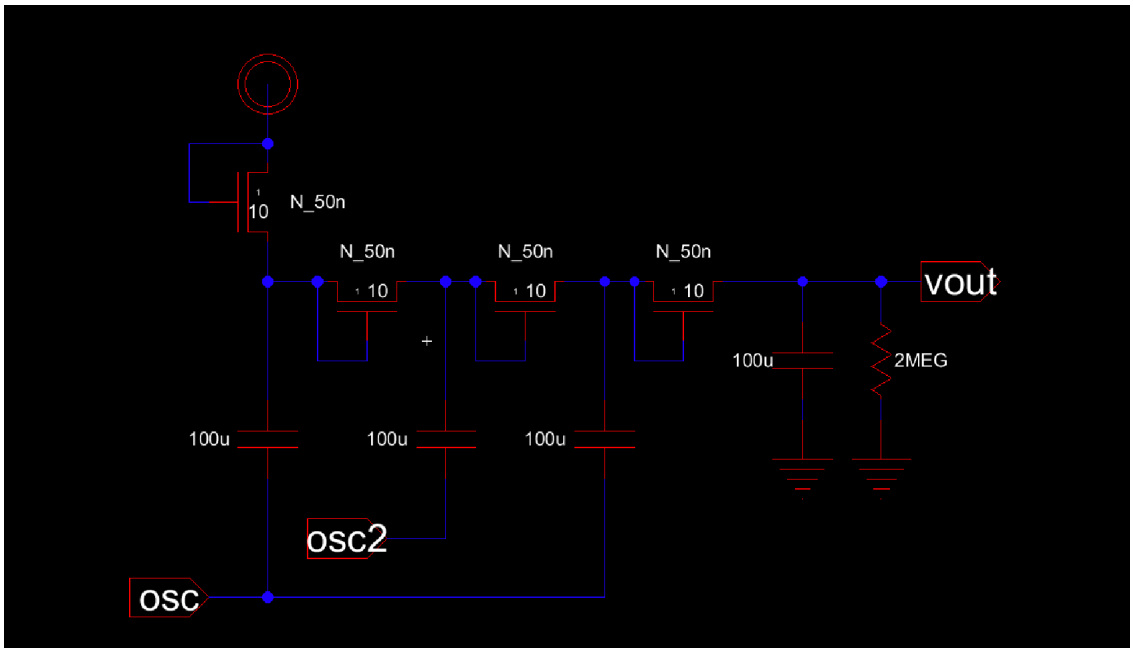
Introduction:

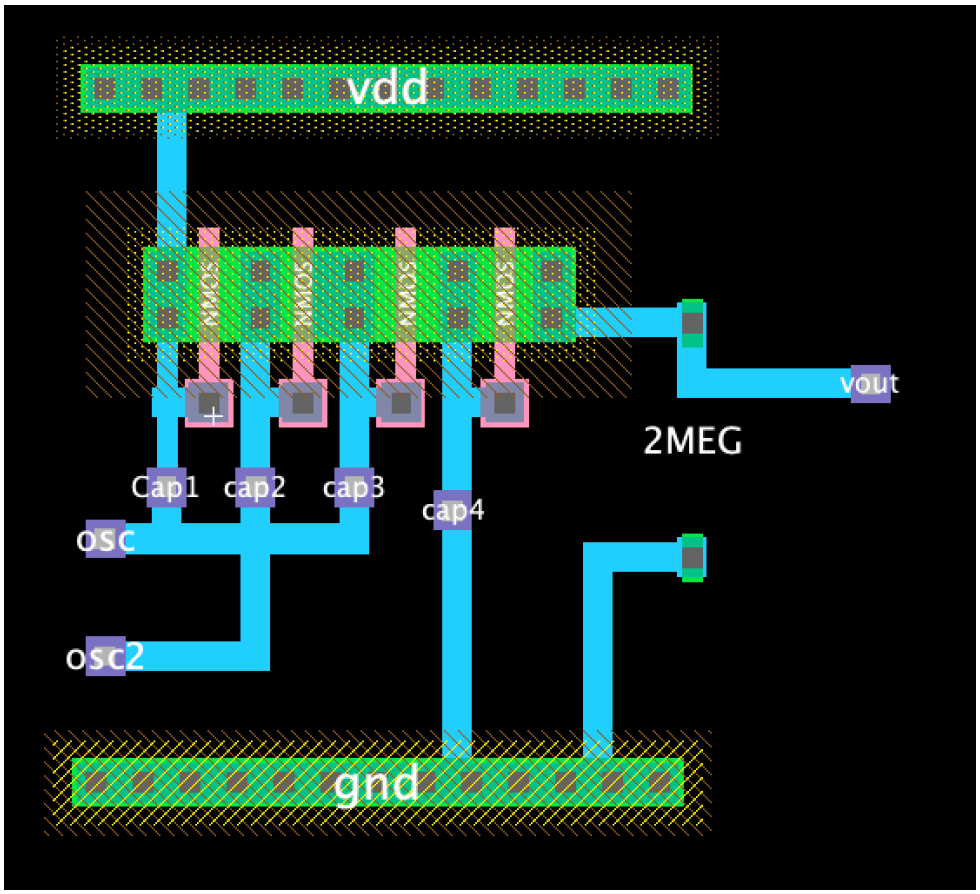
The purpose of this lab is to design and simulate a DC-to-DC charge pump regulator capable of producing a stable 2 V output to drive a 2 MΩ load. The lab involves developing a 3-stage charge pump, a 5-stage charge pump, a ring oscillator with an enable control to generate the required clock signals, and a regulator circuit to maintain the desired voltage level. Each component is first created and tested individually through schematic, layout, and SPICE simulation, then integrated into a complete system to verify proper operation. This lab emphasizes understanding switched-capacitor voltage conversion and the integration of analog and digital circuit elements in a practical VLSI design context

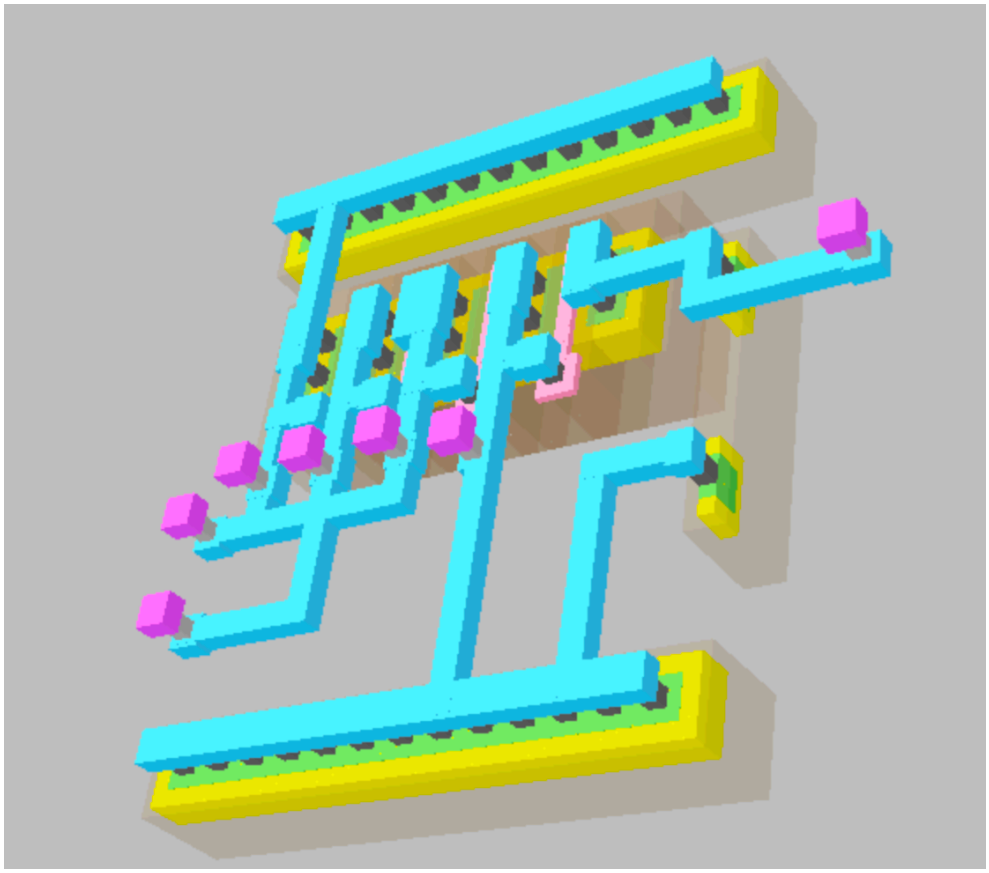
Part 1:

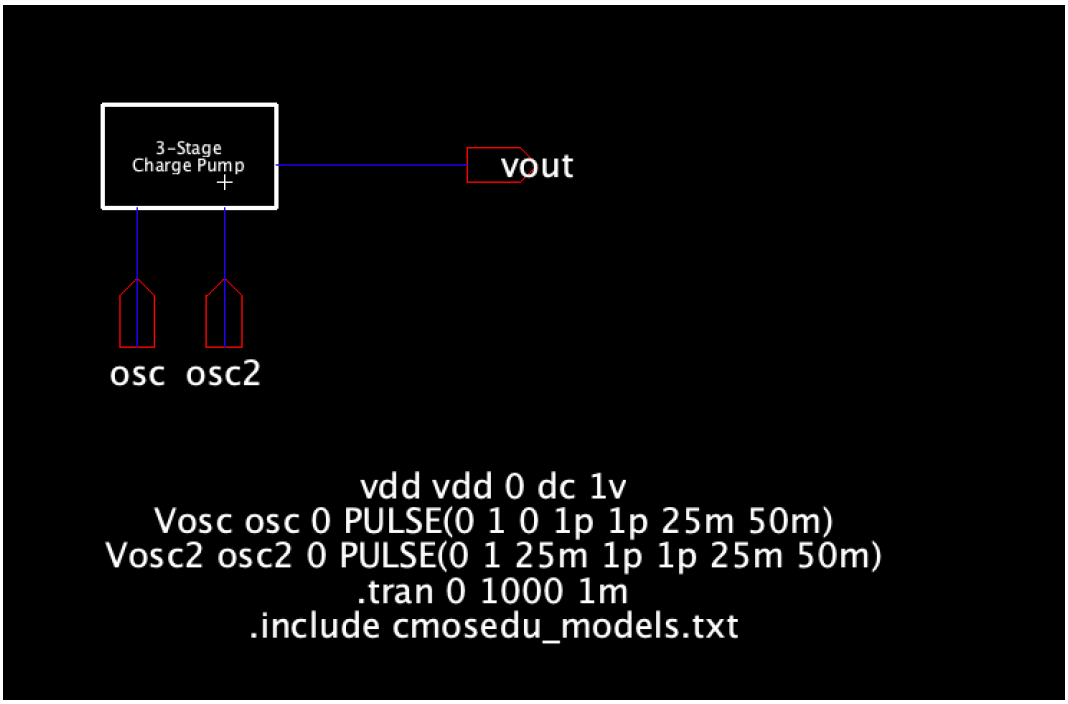
In Part 1 of this lab, the goal is to design and simulate the fundamental building blocks of the DC-to-DC charge pump regulator. This includes developing a 3-stage charge pump, a 5-stage charge pump, a ring oscillator with an enable pin, and a regulator circuit to control the output voltage. Each circuit is first created at the schematic level, followed by layout design and SPICE simulation to verify correct functionality. Completing these individual modules establishes the foundation for the full DC-to-DC converter system to be integrated and tested in Part 2

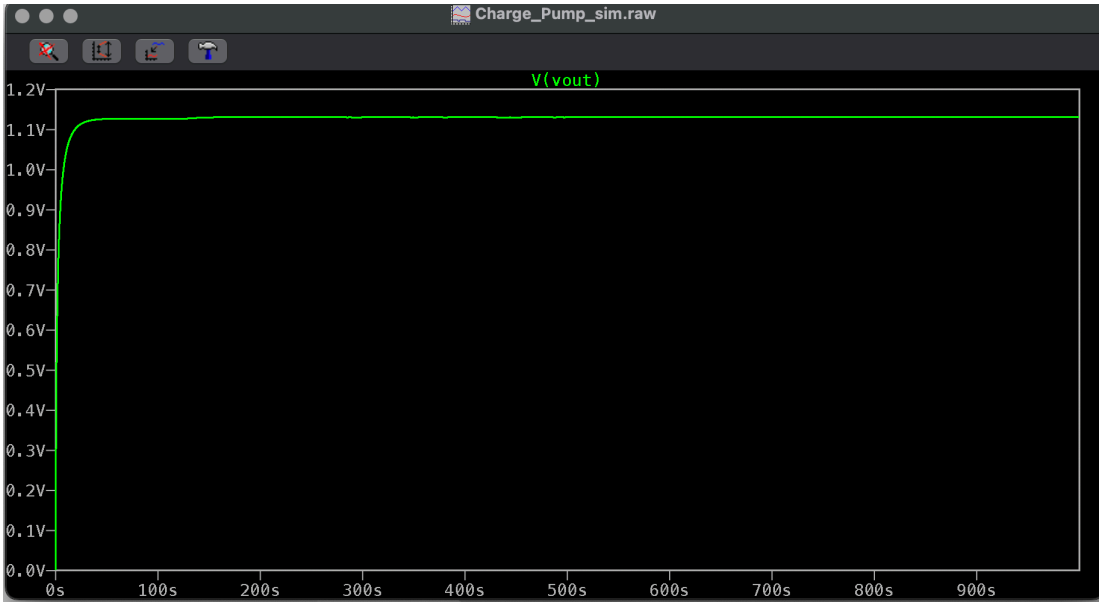
3 stage charge pump:



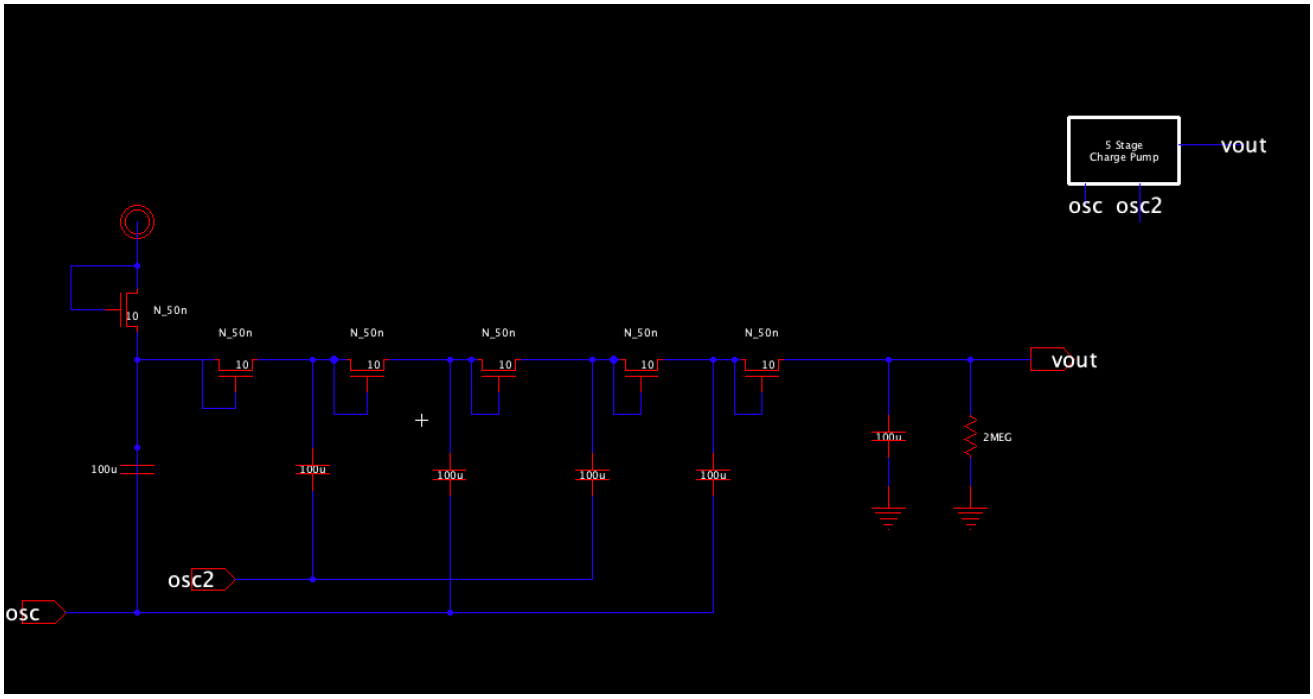

vdd
NMOS
NMOS
NMOS
NMOS
vout
2MEG
Cap1
cap2
cap3
cap4
osc
osc2
gnd

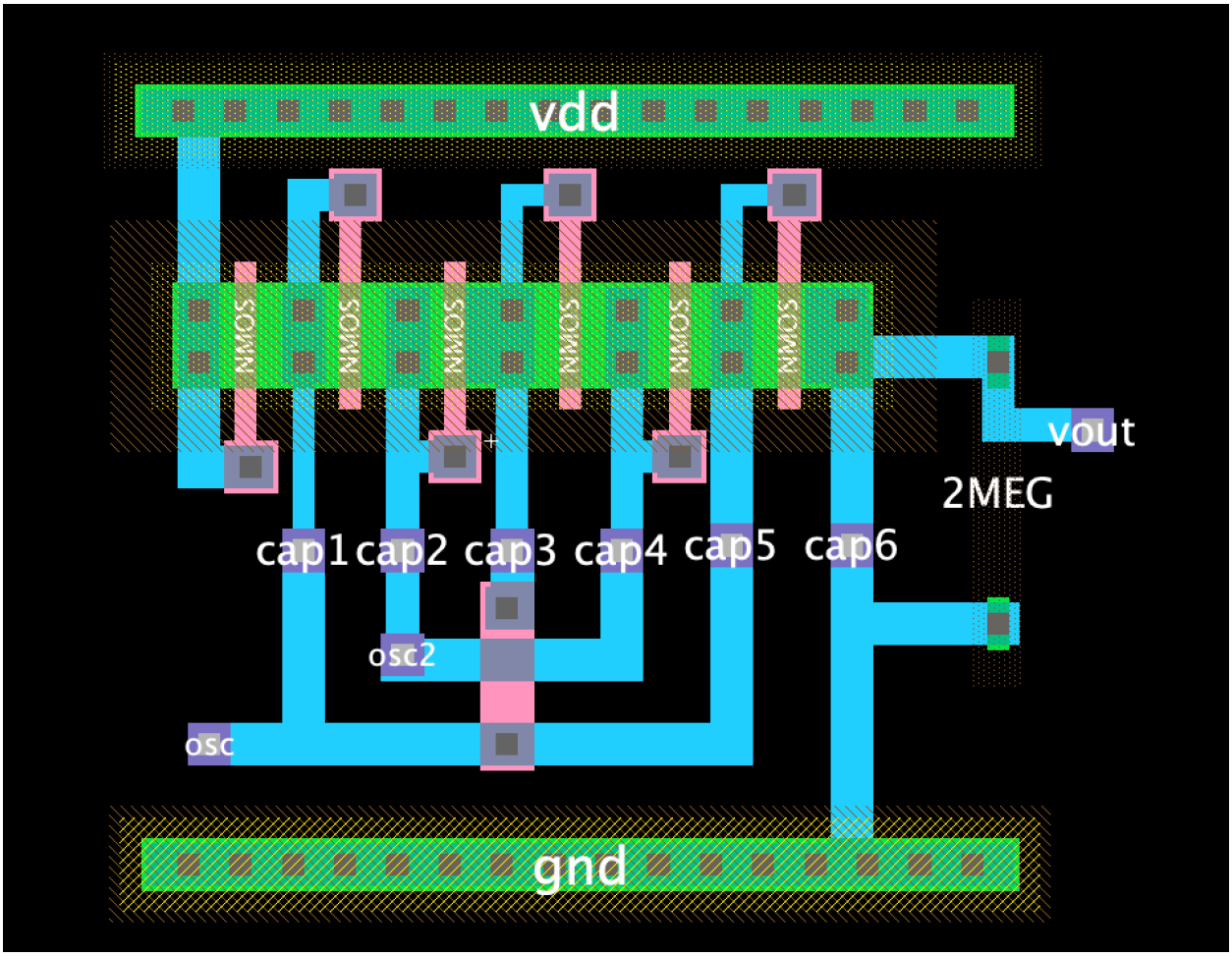


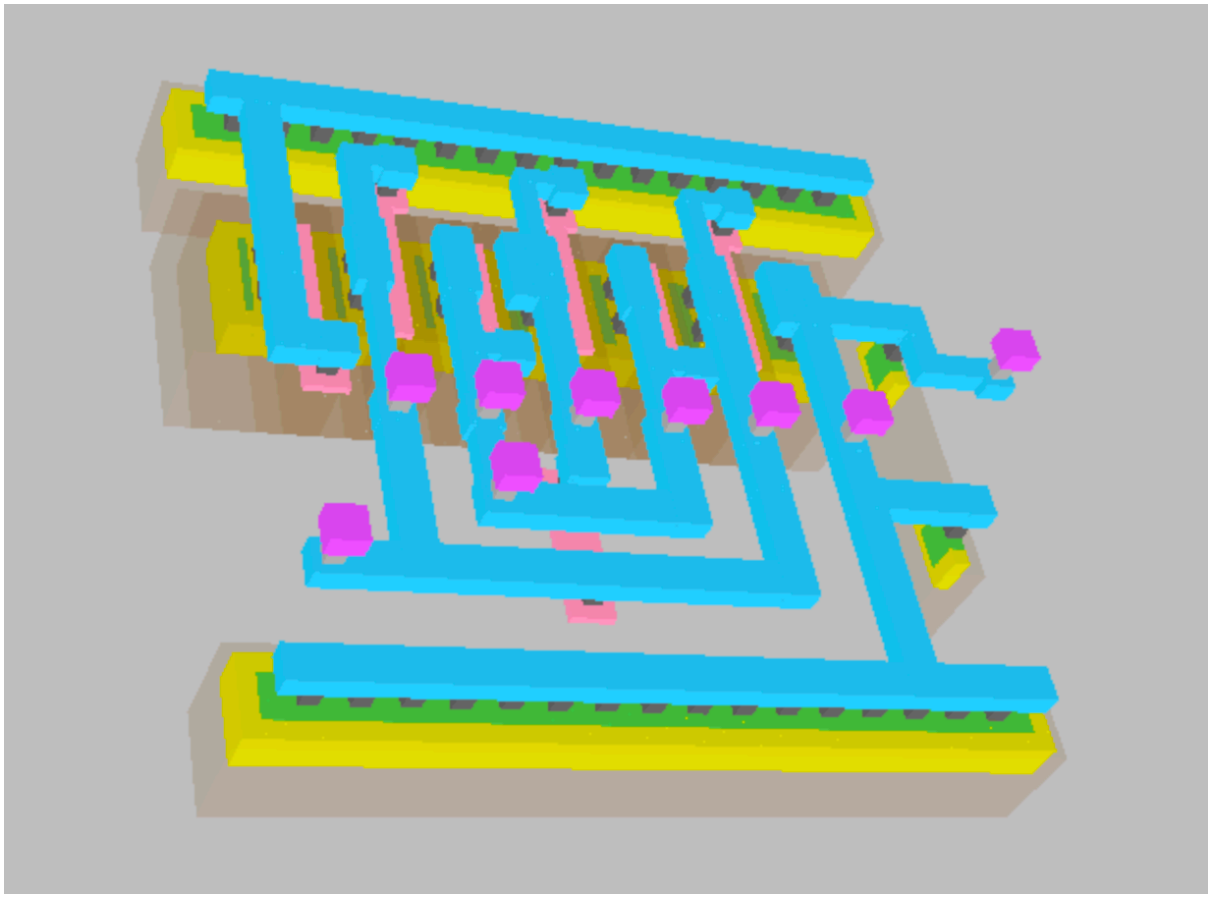

3-Stage
Charge Pump
vout
osc
osc2
vdd vdd 0 dc 1v
Vosc osc 0 PULSE(0 1 0 1p 1p 25m 50m)
Vosc2 osc2 0 PULSE(0 1 25m 1p 1p 25m 50m)
.tran 0 1000 1m
.include cmosedu_models.txt

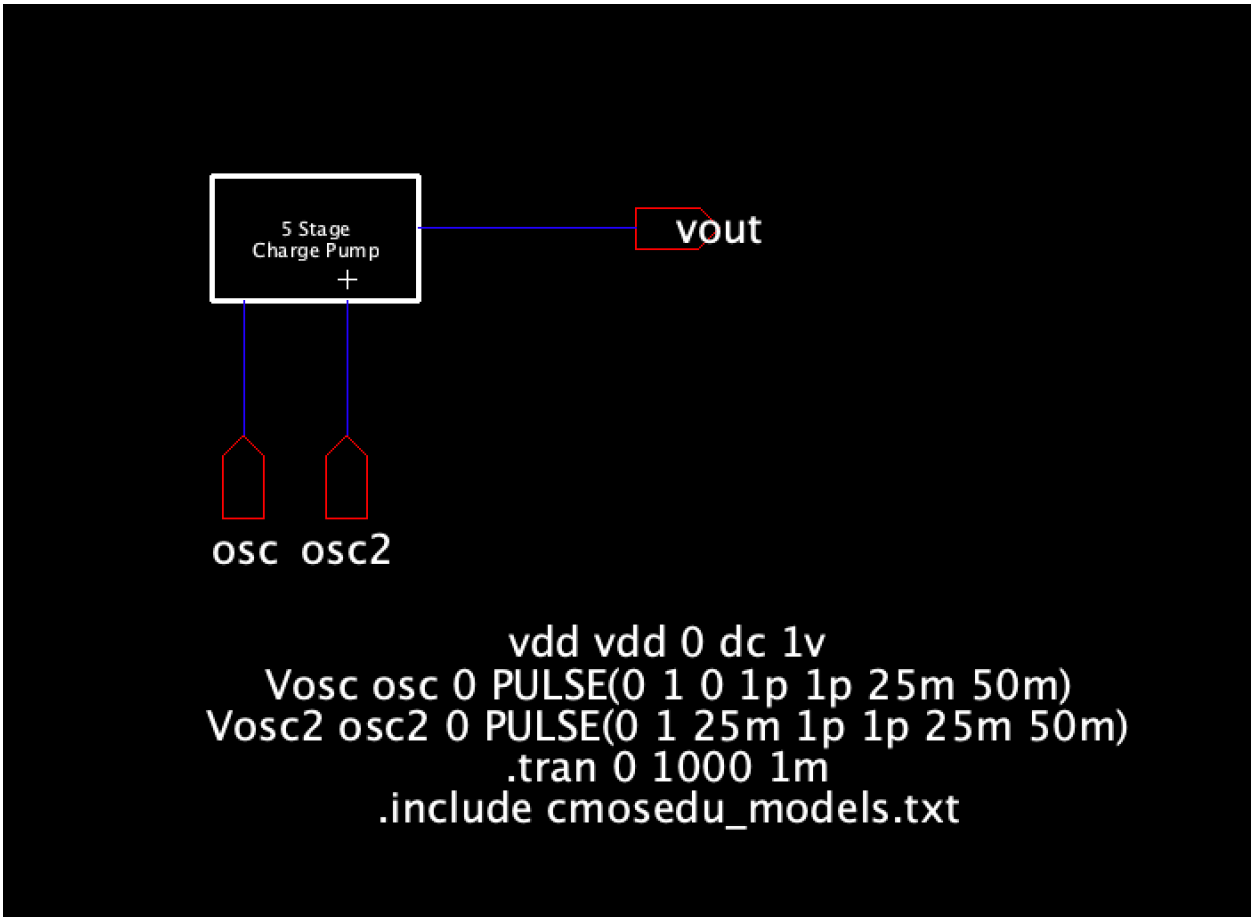

Charge_Pump_sim.raw
V(vout)
1.2V
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0s
100s
200s
300s
400s
500s
600s
700s
800s
900s

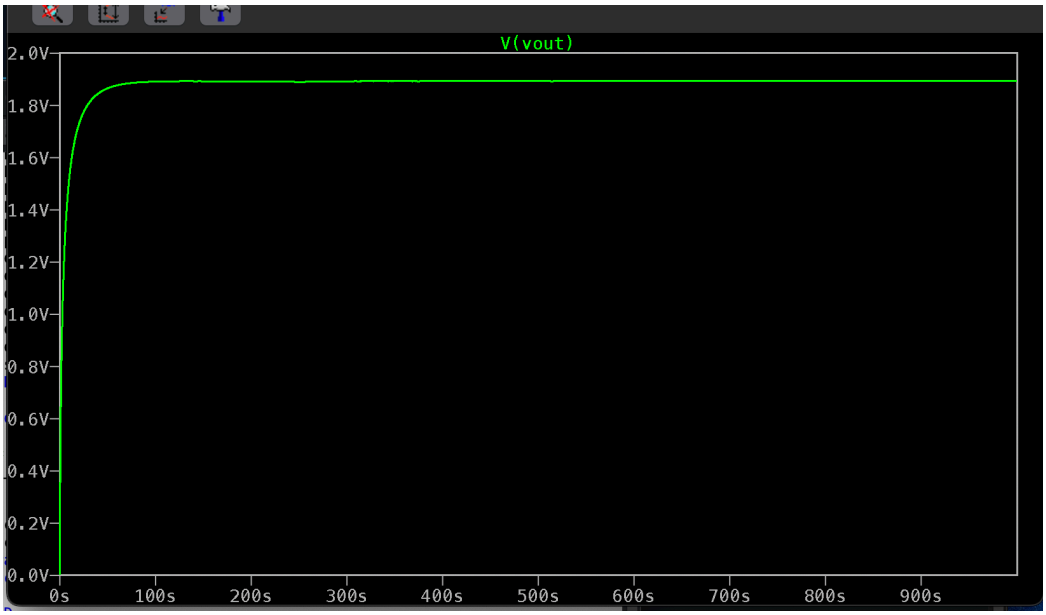
5 stage charge pump:





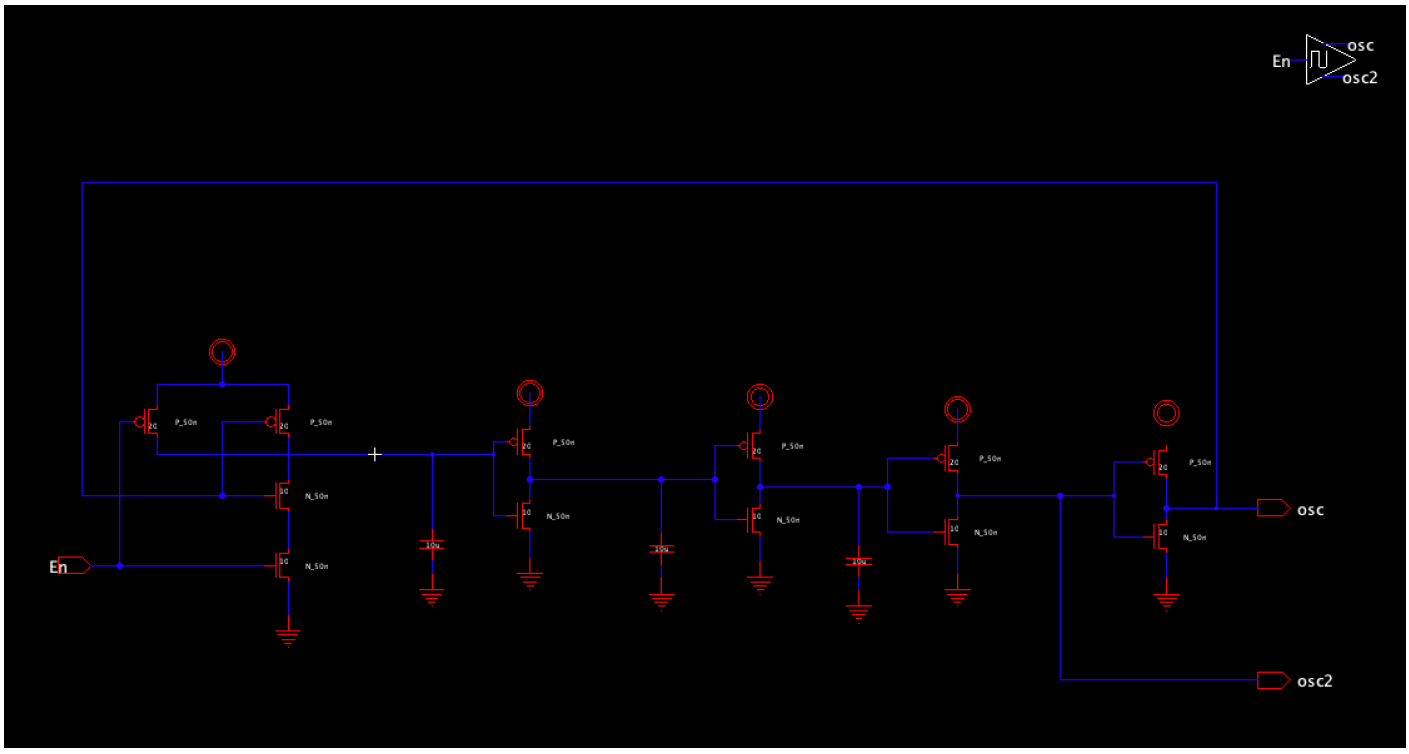


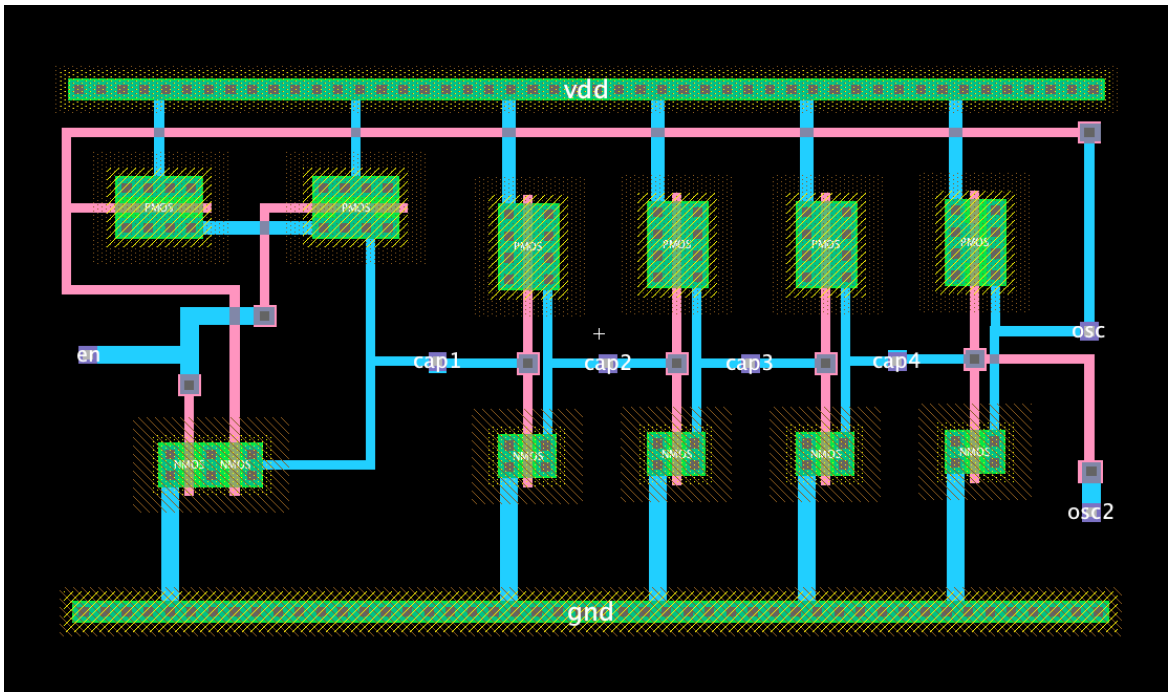

5 Stage
Charge Pump
vout
osc
osc2
vdd vdd 0 dc 1v
Vosc osc 0 PULSE(0 1 0 1p 1p 25m 50m)
Vosc2 osc2 0 PULSE(0 1 25m 1p 1p 25m 50m)
.tran 0 1000 1m
.include cmosedu_models.txt

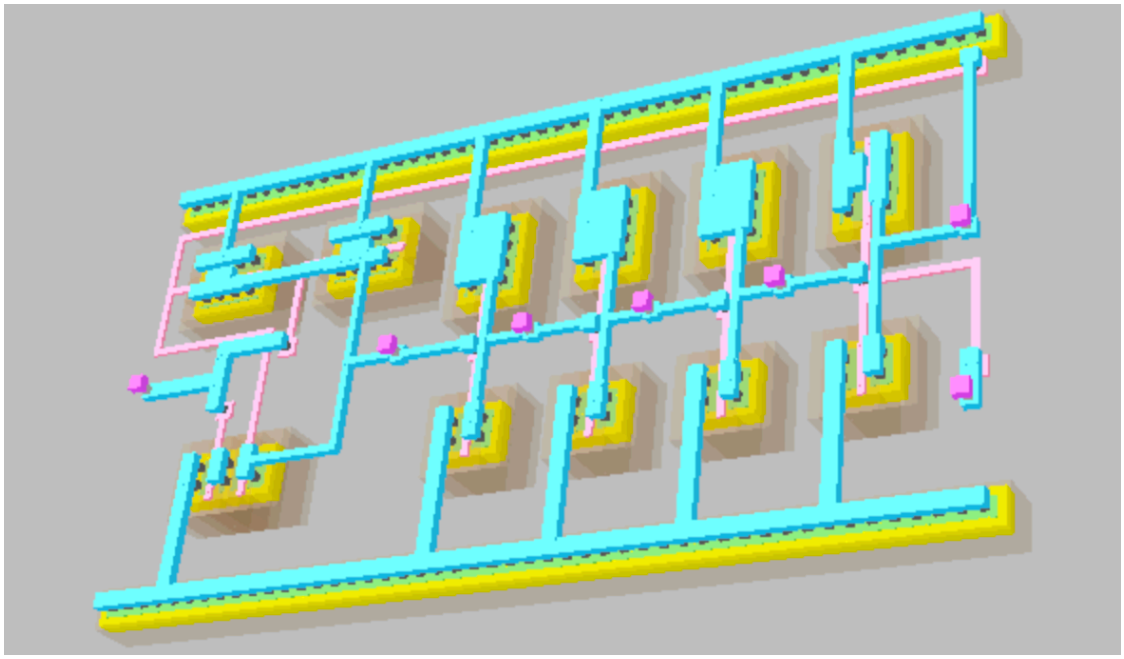


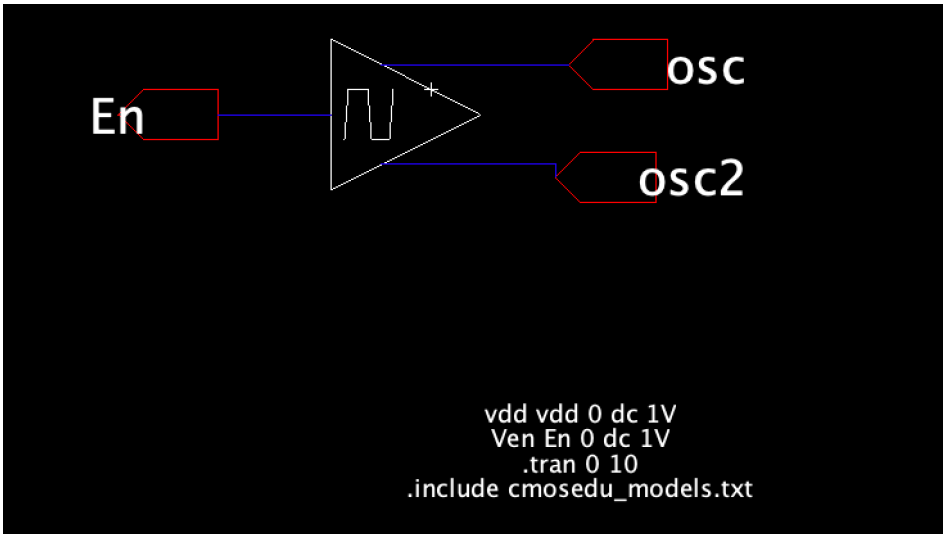
Both 3-stage and 5-stage charge pumps were designed to analyze performance scaling and determine the optimal configuration for the final DC-to-DC converter. The 3-stage design was used primarily for initial validation and functional testing, while the 5-stage charge pump was selected for Part 2 to achieve a higher and more stable output voltage near the 2 V target. Each stage consists of MOSFET switches and pumping capacitors driven by complementary clock phases generated by the ring oscillator. Increasing the number of stages raises the achievable output but also increases parasitic capacitance and voltage losses due to device thresholds, so transistor sizing was carefully chosen to balance efficiency and layout area. SPICE simulations confirmed that the 5-stage pump provided improved output voltage and reduced ripple under a 2 MΩ load.

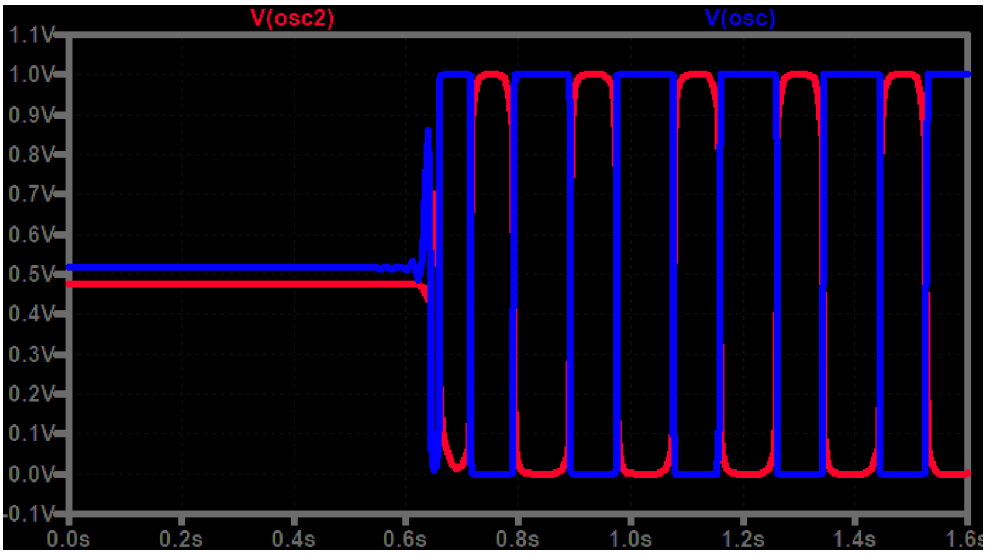
Ring Oscillator:




vdd
PMOS
PMOS
PMOS
PMOS
PMOS
PMOS
en
cap1
cap2
cap3
cap4
osc
NMOS
NMOS
NMOS
NMOS
NMOS
NMOS
osc2
gnd

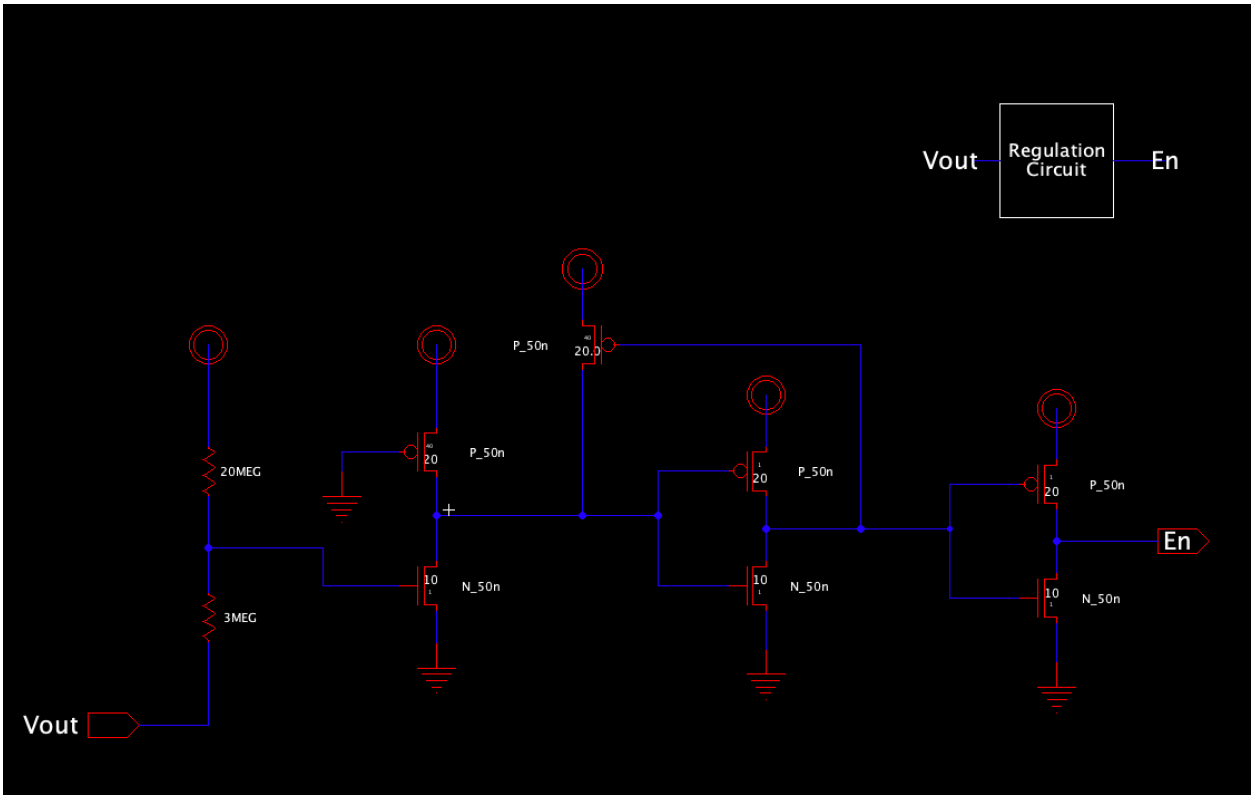


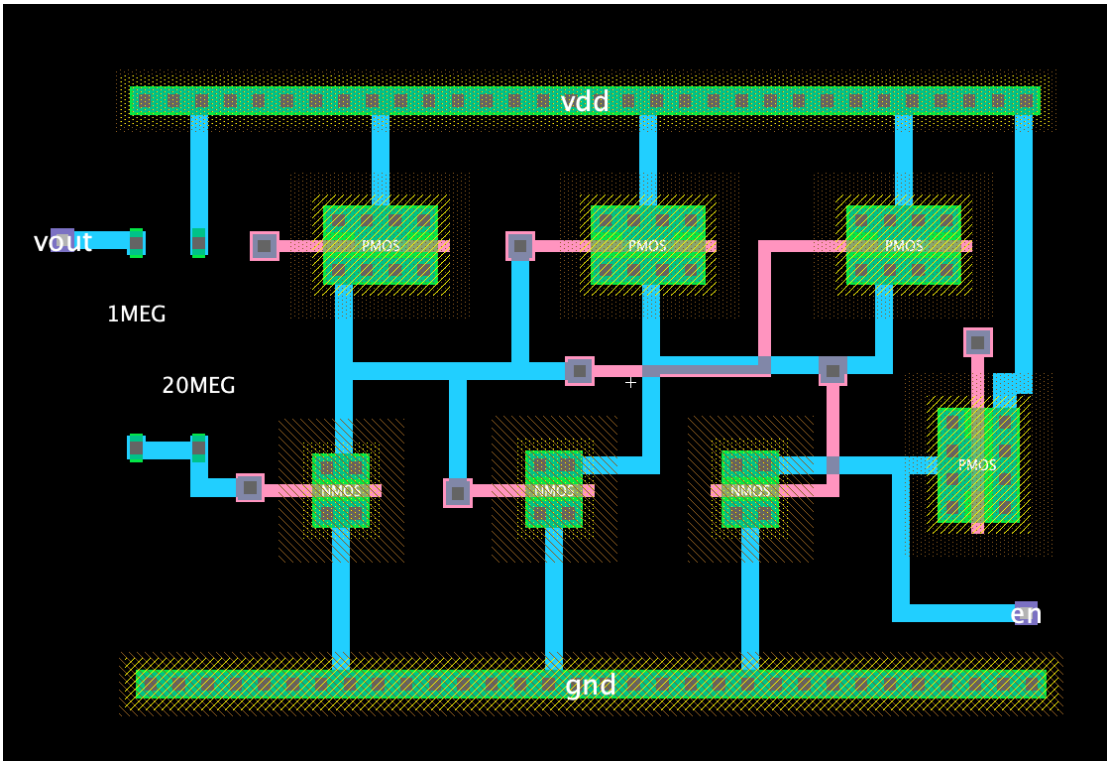

En
osc
osc2
vdd vdd 0 dc 1V
Ven En 0 dc 1V
.tran 0 10
.include cmosedu_models.txt

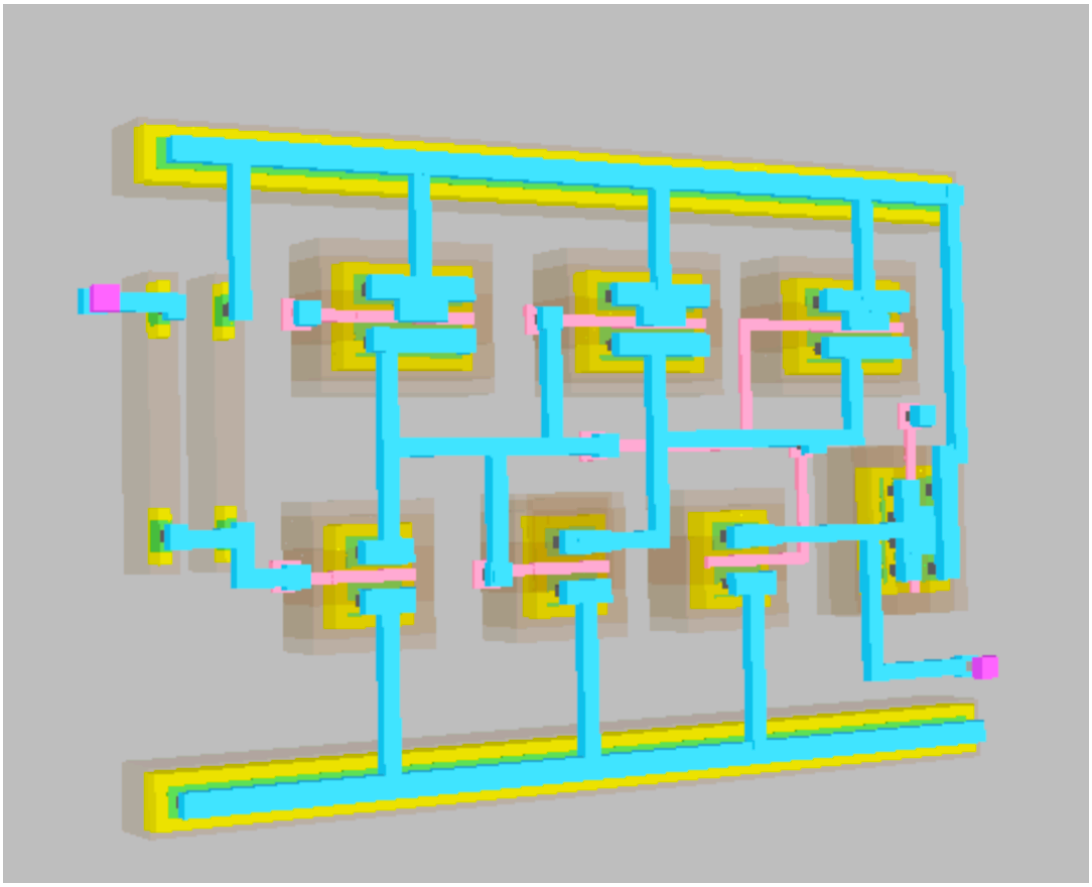


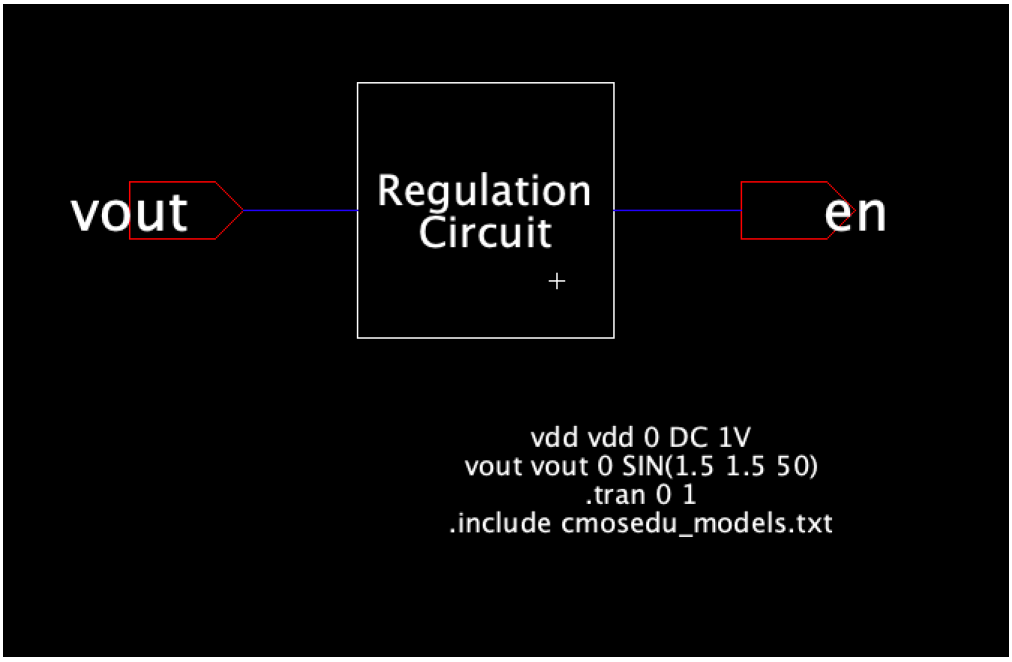
A oscillator was implemented to provide the alternating clock signals necessary for the charge pump operation. The number of stages was chosen to produce a clock frequency high enough to ensure continuous charge transfer but low enough to avoid excessive dynamic power consumption. An enable pin was incorporated so that the oscillator can be disabled by the regulator once the output voltage reaches the desired level, conserving power. Transistor widths and lengths were adjusted to achieve symmetrical rise and fall times, ensuring a stable oscillation waveform. SPICE simulation verified consistent oscillation frequency and amplitude.

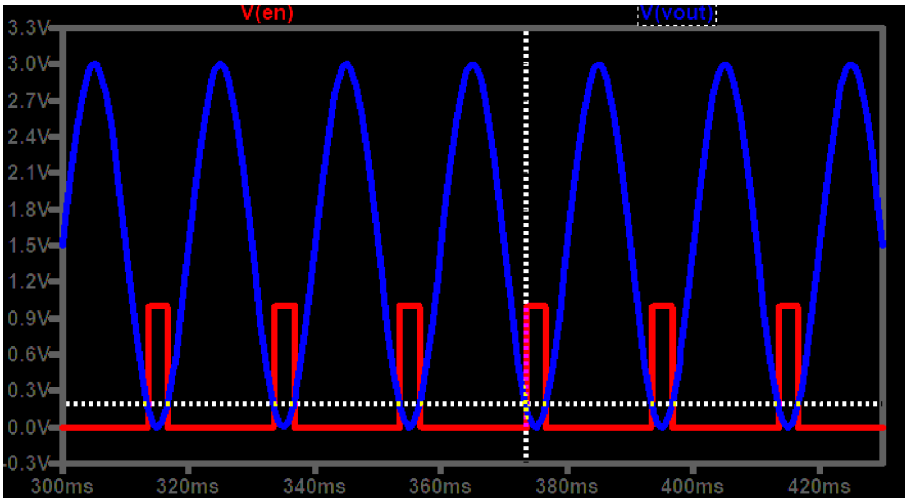
Regulator:




vdd
vout
1MEG
20MEG
PMOS
PMOS
PMOS
PMOS
NMOS
NMOS
NMOS
en
gnd





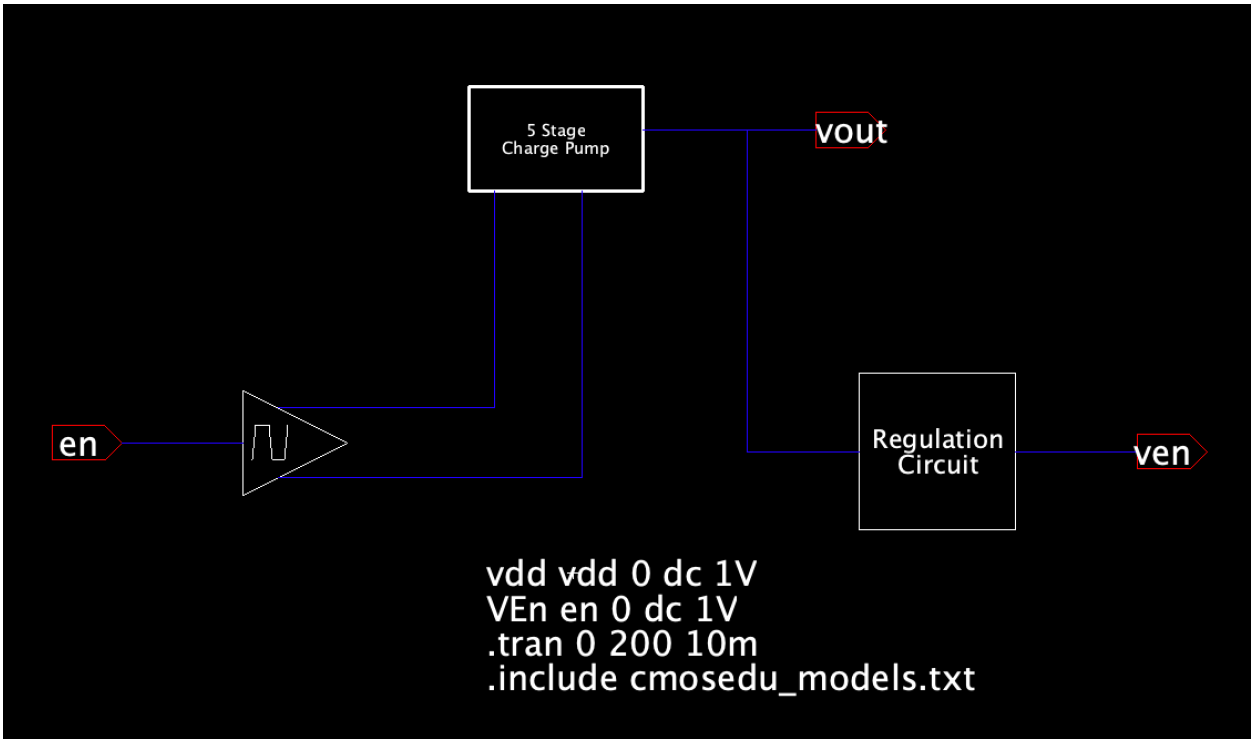


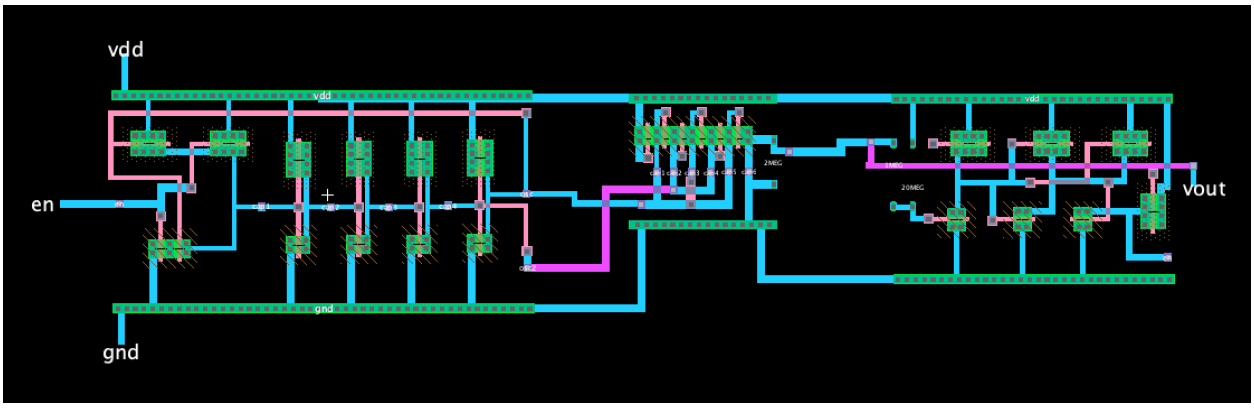
The regulator circuit was designed to monitor the output voltage of the charge pump and control the oscillator's enable signal. When the output reaches approximately 2 V, the regulator disables the oscillator to prevent overcharging, and it re-enables it when the voltage drops below the threshold. A voltage divider and a reference network using transistors with defined threshold voltages were used to set the switching point. This feedback regulation maintains a steady output voltage despite small load variations. Simulation results demonstrated that the regulator responded effectively, keeping the output within the desired range.

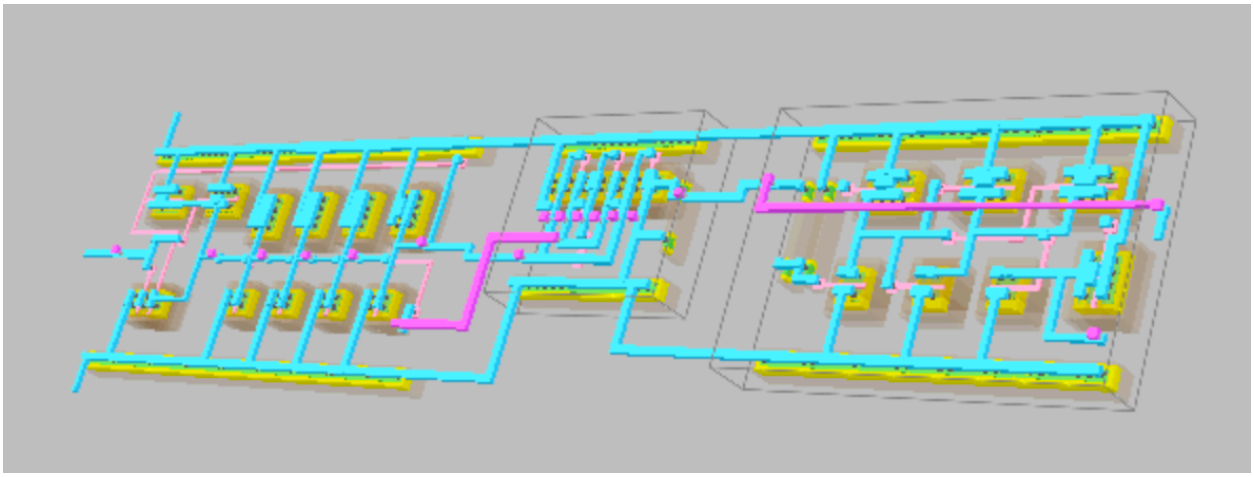
Part 2:

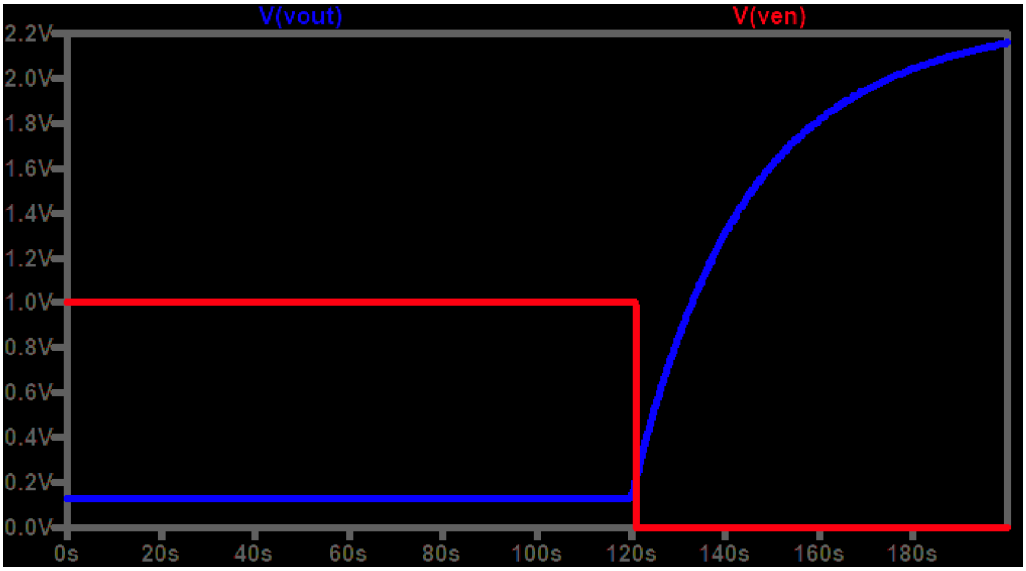
In Part 2 of this lab, the previously designed modules, the 5-stage charge pump, ring oscillator with enable control and regulator circuit are integrated to form a complete DC-to-DC converter system. The objective is to verify the overall operation of the circuit by simulating the combined design in SPICE and confirming that it produces a regulated 2 V output while driving a 2 MΩ load. This stage focuses on ensuring proper interconnection between subcircuits, validating the feedback control behavior, and observing the interaction between the oscillator, charge pump, and regulator. Successful simulation of the integrated system demonstrates a functional on-chip voltage regulator capable of stable DC-to-DC conversion.

DC-to-DC Converter :









Despite successfully integrating the 5-stage charge pump, ring oscillator, and regulation circuit into a complete DC-to-DC converter, the final design did not function as intended. SPICE simulations showed partial voltage buildup, but the output failed to reach the 2 V target, indicating that the system is currently not working fully. Several hours were spent troubleshooting potential issues such as incorrect enable logic, threshold mismatches in the regulator, and timing misalignment between the oscillator and pump stages, but the problem remains unresolved. Nonetheless, the integration process provided valuable insight into mixed signal system behavior, highlighting the challenges of achieving stable regulation and synchronization in a fully on chip voltage conversion design.

Conclusion:

In conclusion, this lab explored the design, layout and simulation of a DC-to-DC charge pump regulator, demonstrating the principles of on-chip voltage conversion using switched capacitor techniques. In Part 1, individual components, the 3-stage and 5-stage charge pumps, ring oscillator with enable control and regulator circuit were successfully designed, laid out and verified through SPICE simulations. These results confirmed proper charge transfer, oscillation behavior and feedback regulation in isolation. In Part 2, the modules were integrated to form a complete converter system intended to provide a regulated 2 V output from a 1 V supply. Although the system integration was completed, the overall circuit did not reach full functionality and the desired regulated output was not achieved despite extensive troubleshooting.

Despite these challenges, the lab provided valuable hands on experience in VLSI power circuit design, hierarchical system integration and simulation based debugging. It emphasized the practical difficulties of coordinating multiple analog and digital blocks within a single chip, such as timing synchronization, parasitic effects and threshold variations. Overall, the project deepened understanding of how DC-to-DC converters operate and highlighted the importance of careful design, verification and iteration in achieving a reliable on chip power regulation system.