UNIVERSITY of DENVER

Lab 2: Directions

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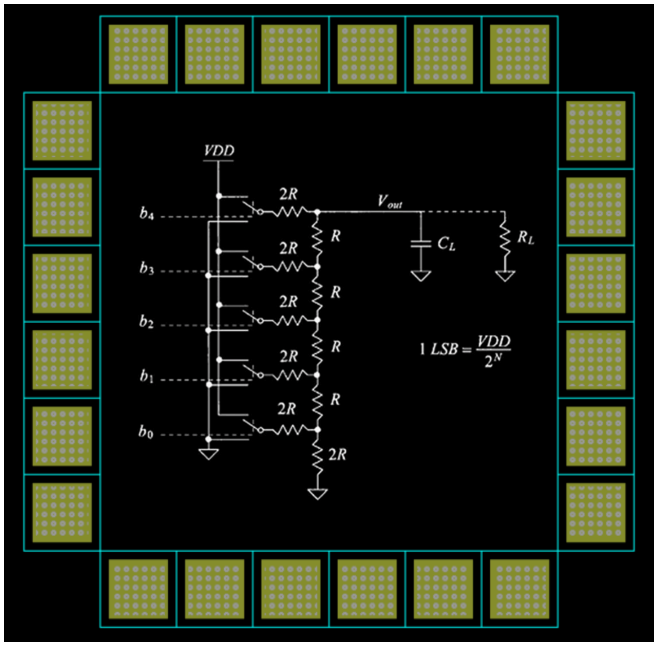
Date of Experiment: Friday, 26 / September / 2025

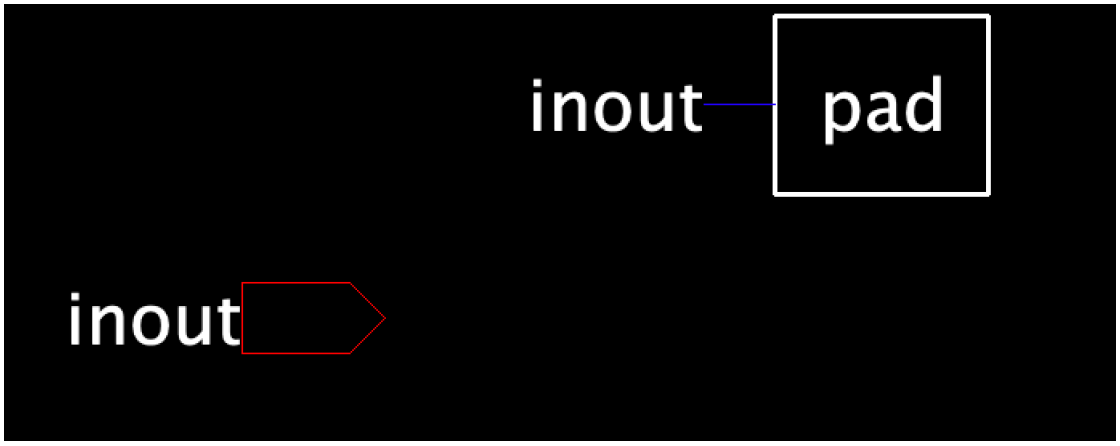
Introduction:

The purpose of this lab is to extend the digital-to-analog converter (DAC) design from Lab 1 by integrating it into a complete die that can interface with the external environment. In very-large-scale integration (VLSI) design, direct connection between on-chip circuits and external signals requires specialized input/output (I/O) structures, which are provided by pad cells and organized within a padframe. This lab involves creating both the schematics and layout of a square padframe that incorporates the DAC at its core, using the minimum number of pad cells necessary to support all DAC pinouts while ensuring proper power, ground, and signal routing. The design process emphasizes functional correctness, efficient pad placement, robust routing, and adherence to standard layout practices, ultimately providing practical experience in transitioning from block-level circuit design to full chip-level implementation.

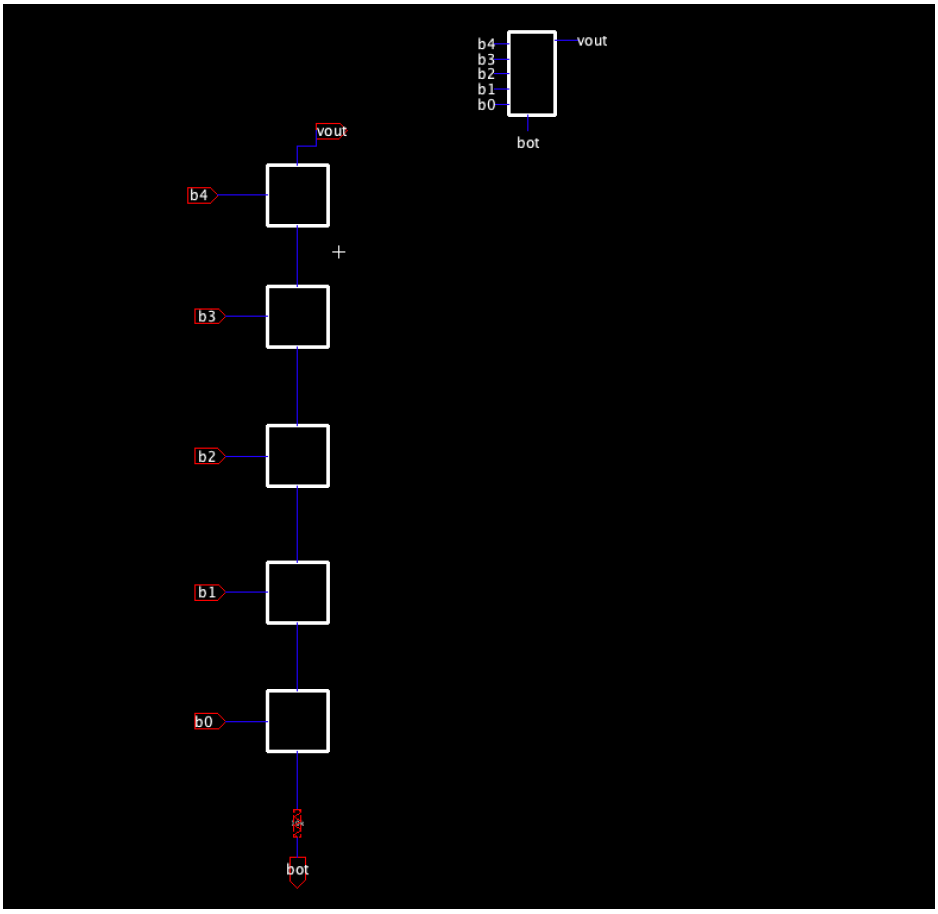


Schematics:

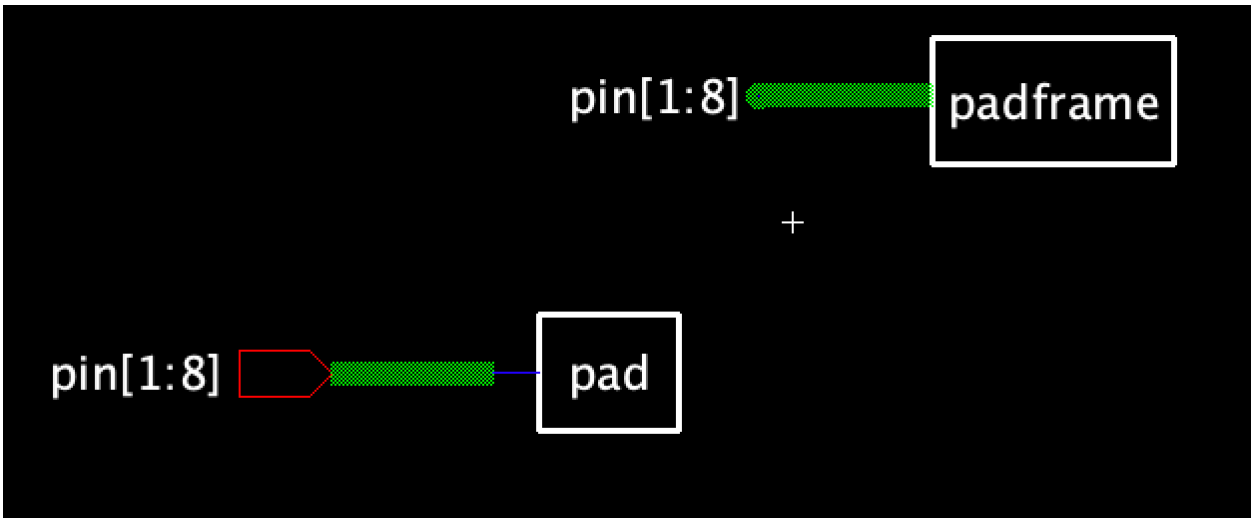
The schematic of the pad:



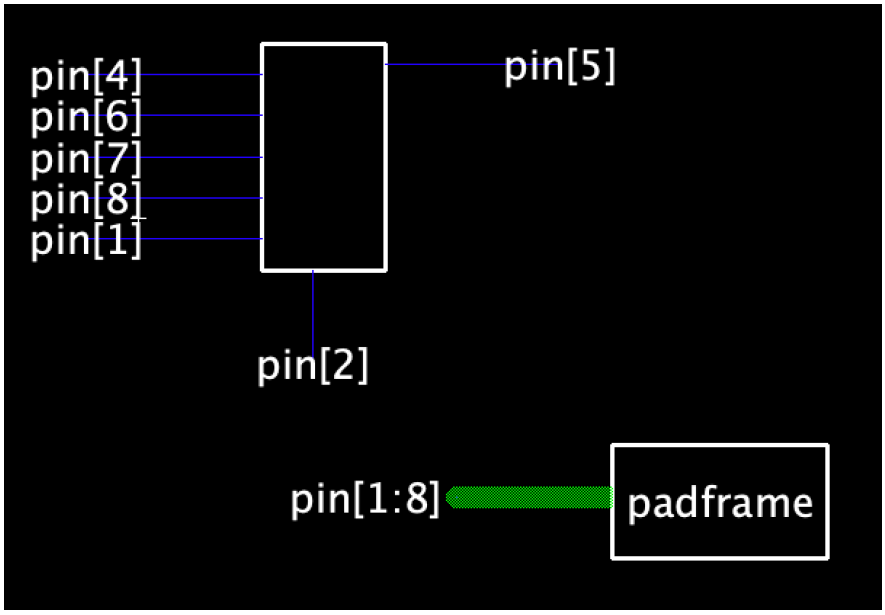
The schematic of the 5bit DAC:



The schematic of the padframe:



The schematic of the final ic (padframe with DAC):

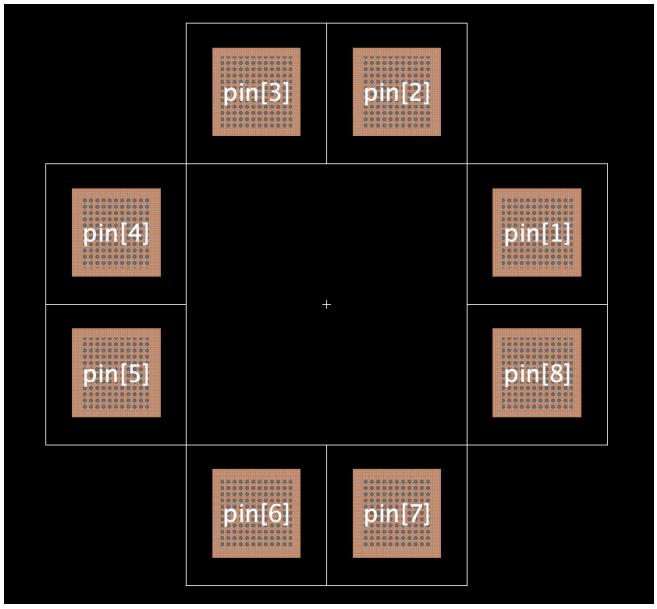


In designing the schematics, the primary consideration was to ensure that the DAC from Lab 1 could be reliably connected to the outside world using the minimum number of pad cells, as required by the lab. Digital inputs were assigned to standard input pad cells with built-in ESD protection to guarantee valid logic levels and safe operation during external interfacing. The analog output of the DAC was routed through a dedicated analog output pad to minimize leakage and preserve signal integrity. Power and ground pads were included for both analog and digital domains to isolate noise-sensitive signals from switching activity and to provide robust return paths for ESD events. This organization allowed the padframe to remain compact while maintaining reliable operation.

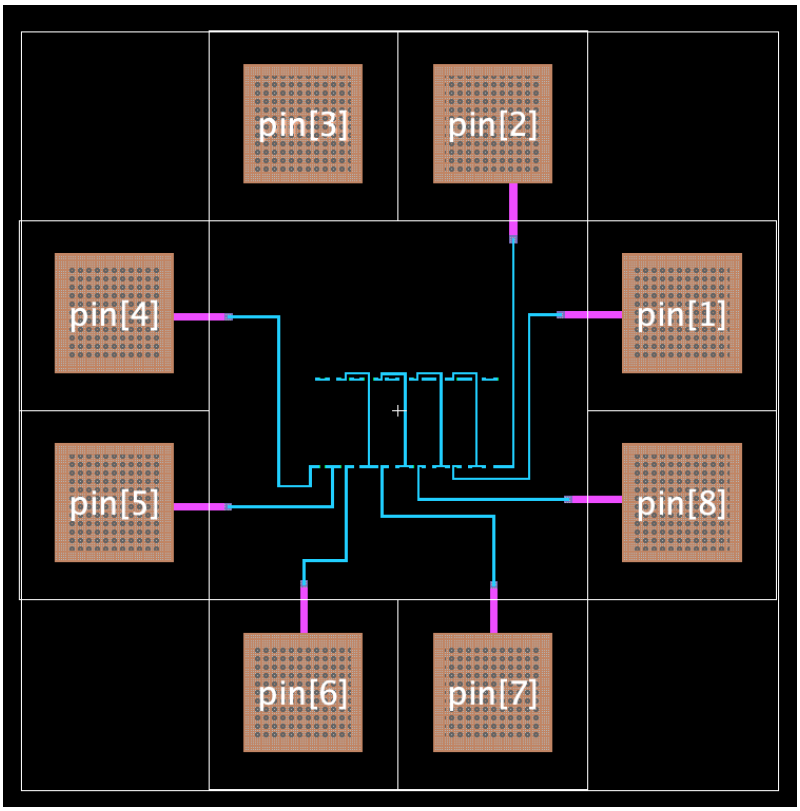
Additionally, pad placement within the schematic was guided by functional grouping and practical routing considerations. Digital input pads were positioned together to simplify interconnects to the DAC's digital pins, while analog pads, including the DAC output and any reference pins, were placed on quieter sides of the frame near their associated supply pads to reduce interference. Corner and filler cells were included only where required by the library to close the padframe and maintain power continuity. By carefully balancing the need for minimal pad usage with the requirements for protection, power integrity, and analog performance, the schematic design ensures both functional correctness and efficient integration of the DAC into a complete chip-level structure.

Layouts:

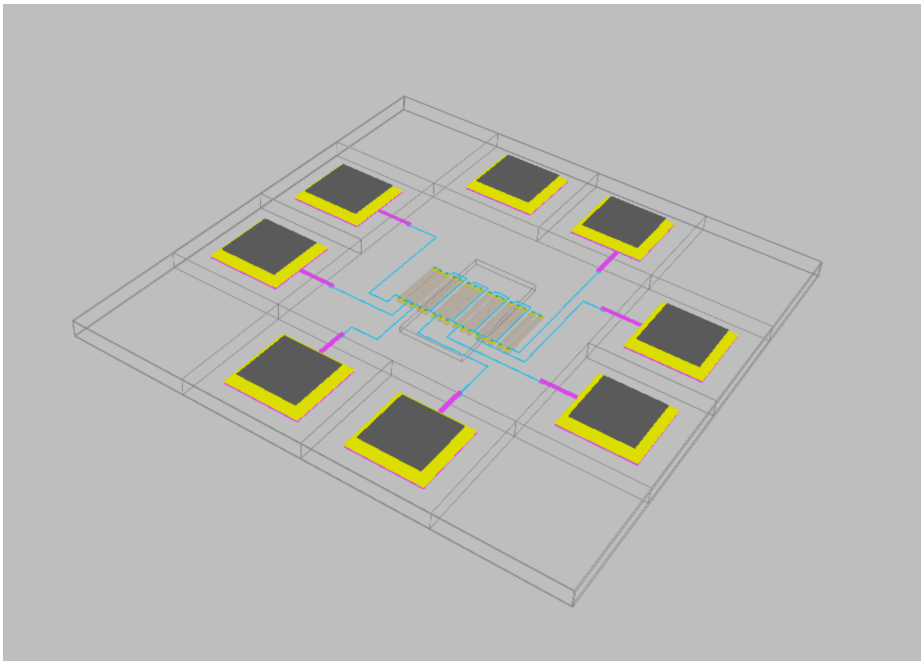
The Layout of the padframe:



The Layout of the final ic (padframe with DAC):



The 3D View of the final ic (padframe with DAC):



In designing the layout, the main objective was to create a compact, square padframe that surrounds the DAC and provides clear, direct routing paths between the internal circuitry and the I/O pads. The DAC was placed centrally within the padframe to minimize interconnect length and ensure balanced routing to all sides. Power and ground pads were distributed symmetrically around the frame to improve current delivery and reduce IR drop while also providing short discharge paths for ESD protection. The analog output and reference pads were placed on sides of the frame away from noisy digital inputs, ensuring reduced coupling and preserving signal integrity. This placement strategy balanced electrical performance with adherence to the lab's requirement for a minimum pad count.

Special attention was given to pad orientation, routing simplicity, and manufacturability. Pads were placed in a consistent order to prevent signal crossing and to align with schematic net names, minimizing the chance of LVS errors. Wide metal traces and appropriate spacing were used for power and ground rails to ensure robust connectivity and compliance with design rules. Corner cells were included to close the padframe and guarantee continuity of the supply rails. By carefully organizing placement, isolating sensitive analog paths, and following standard layout practices, the final layout provides a reliable physical implementation that complements the schematic design while maintaining functional correctness and efficiency.

Conclusion:

In conclusion, this lab successfully demonstrated the integration of the 5-bit DAC from Lab 1 into a complete chip-level design through the creation of both schematics and layout for a square padframe. By carefully selecting pad cells, grouping digital and analog signals appropriately, and minimizing the number of pads while maintaining functionality, the schematic design ensured reliable operation and protection. The layout reinforced these decisions by placing the DAC centrally, distributing power and ground pads symmetrically, and isolating sensitive analog paths from digital switching noise. Together, these design choices provided practical experience in bridging block-level circuit design with full die implementation, highlighting the importance of both functional correctness and physical layout considerations in VLSI design.