UNIVERSITY of DENVER

Lab 4: Directions

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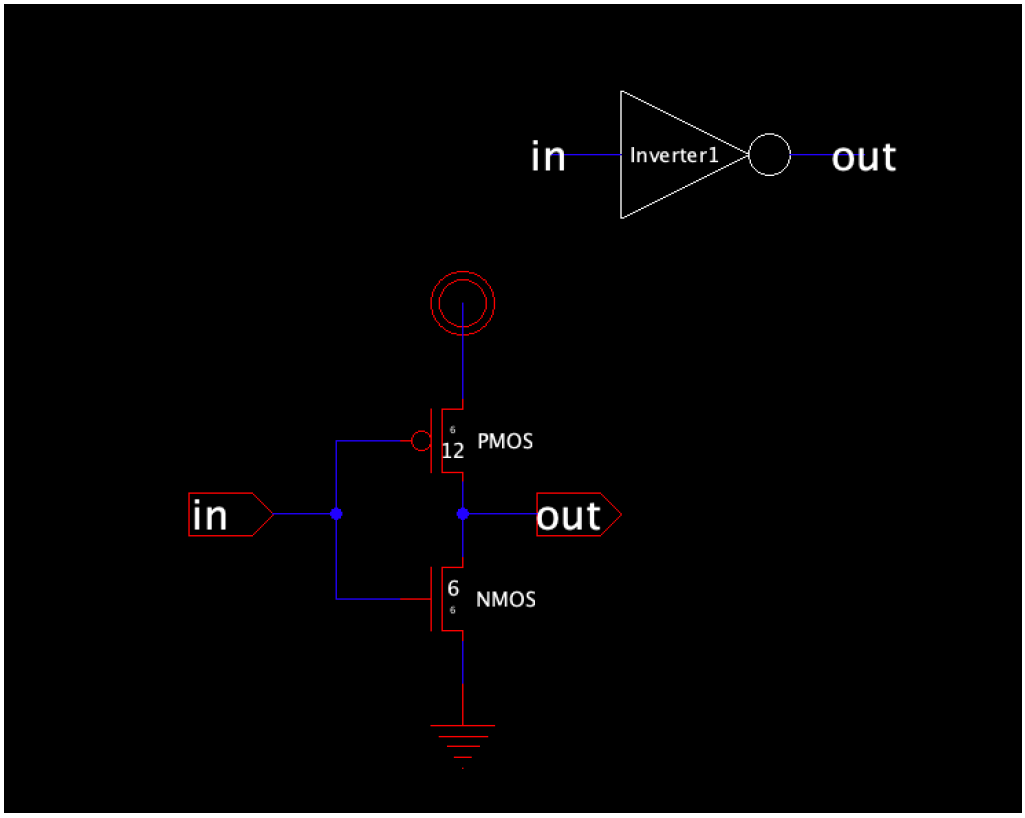
Introduction:

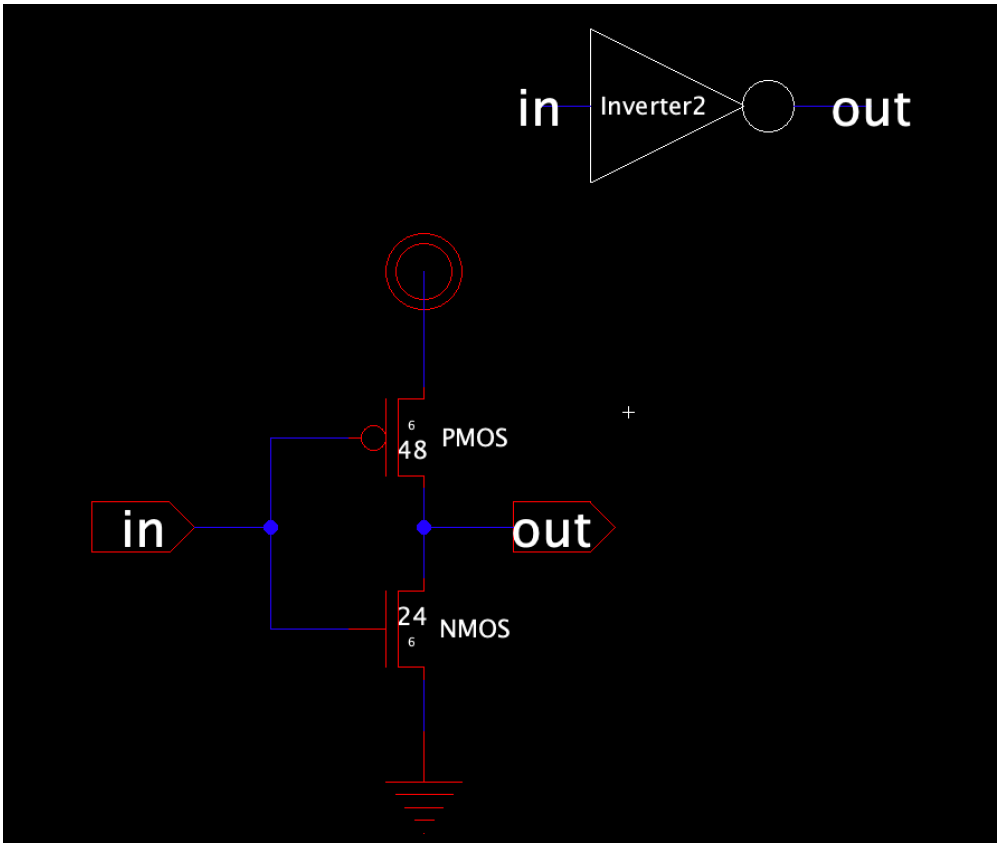
This lab focuses on designing and analyzing CMOS inverters to see how transistor sizing and load conditions affect their performance. Two different inverter versions were built and tested: one with smaller transistors (PMOS 12 µm/6 µm, NMOS 6 µm/6 µm) and another with larger, stronger devices (PMOS 48 µm/6 µm, NMOS 24 µm/6 µm using a multiplier of four). The goal was to understand how increasing transistor width changes the switching point, speed, and ability to drive larger capacitive loads.

By running both DC and transient simulations, we measured the voltage transfer curve, identified the trip point (V_M), and compared how each inverter handled different output capacitances ranging from 100 fF to 100 pF. The lab also included creating a proper layout for each inverter, following CMOS design rules and ensuring clean routing for power, ground, input, and output connections. Overall, this experiment gives hands-on experience with how inverter sizing influences delay, switching behavior, and overall circuit performance in real-world design.

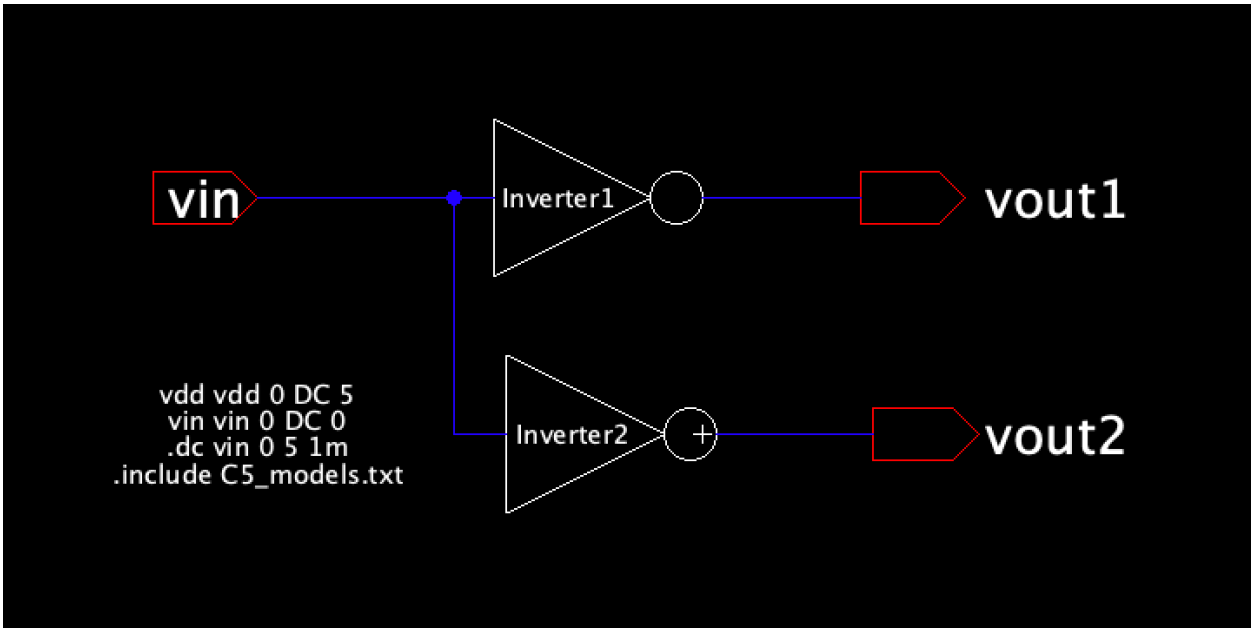
Schematics:

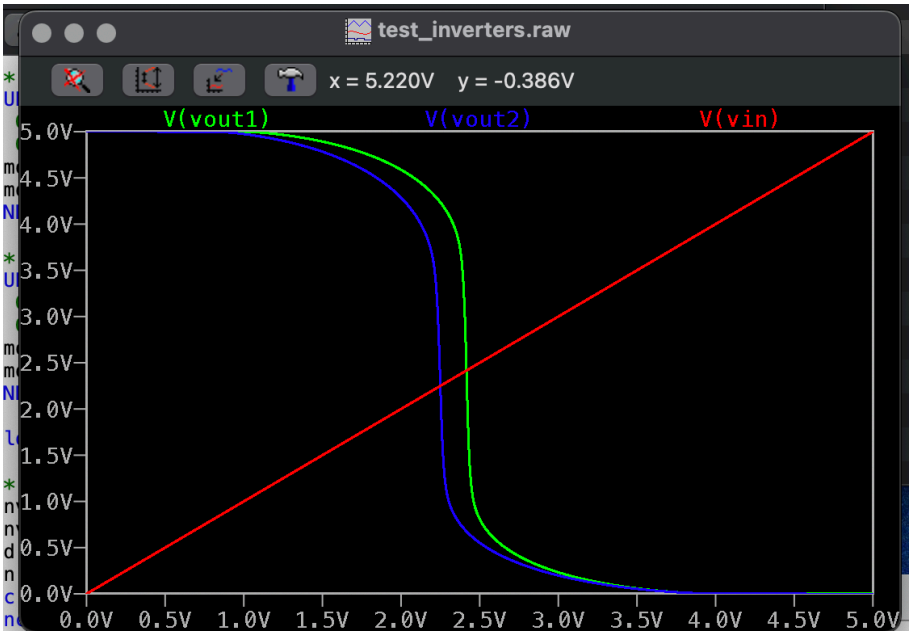
- The schematics for the inverters and respective simulations to show the switching point.

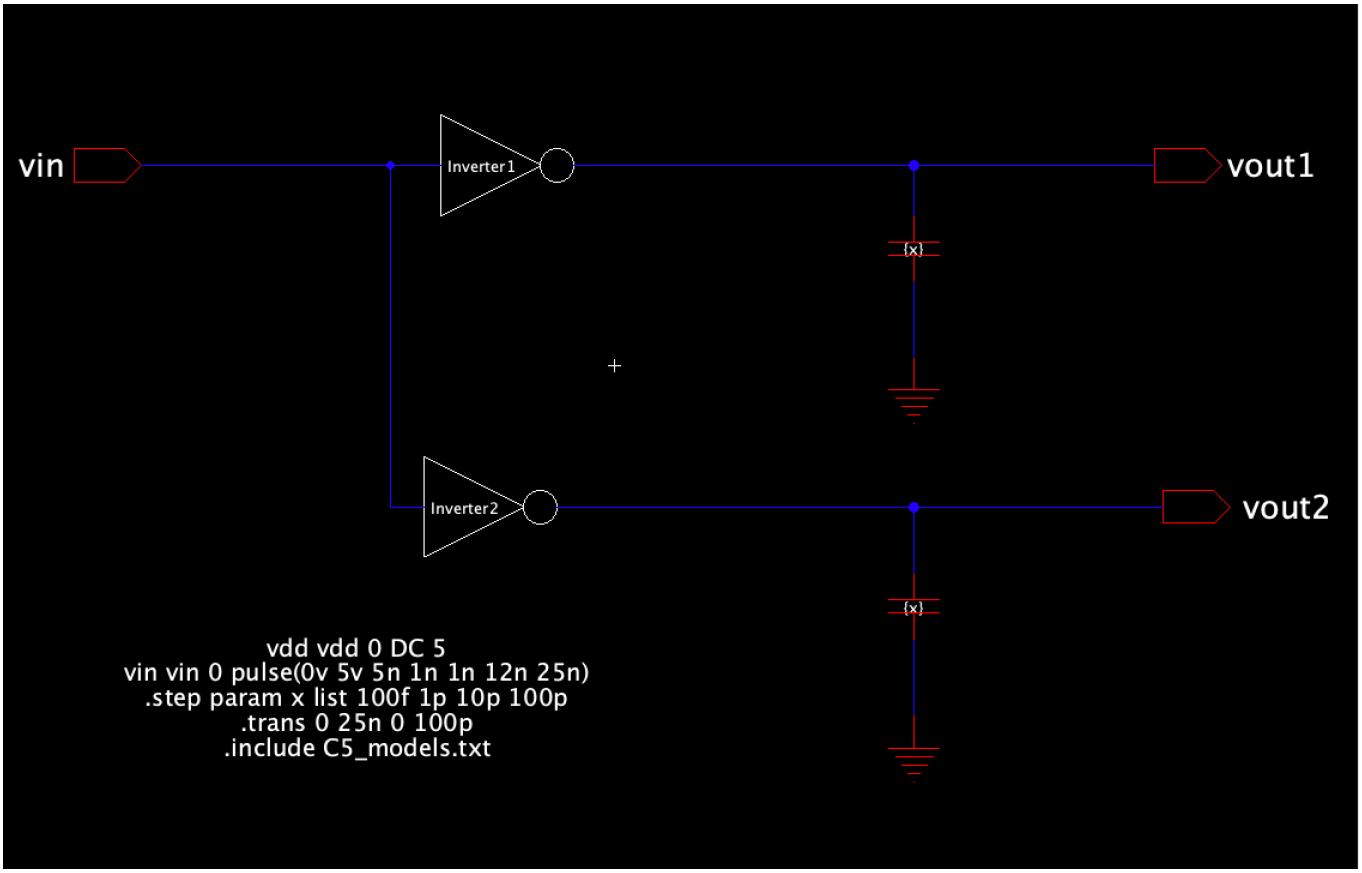




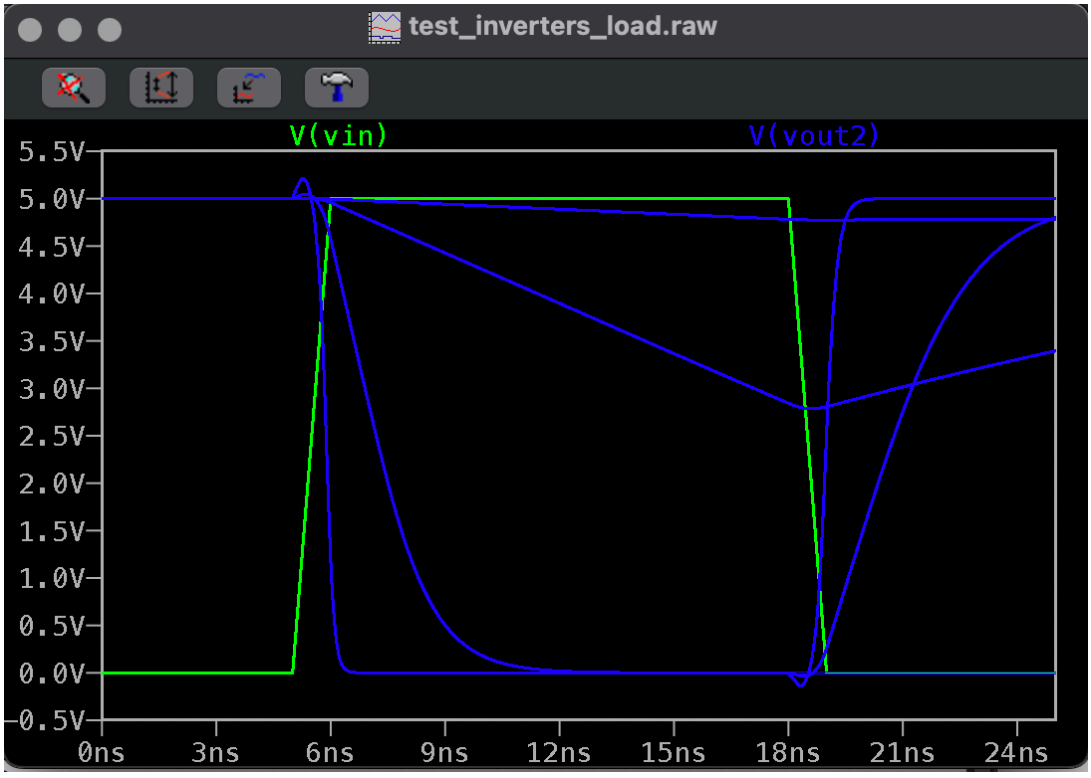
- Apply a pulse waveform to both inverters each driving a 100 fF, 1pF, 10pF, and 100 pF capacitive load. Comment the results on the report.

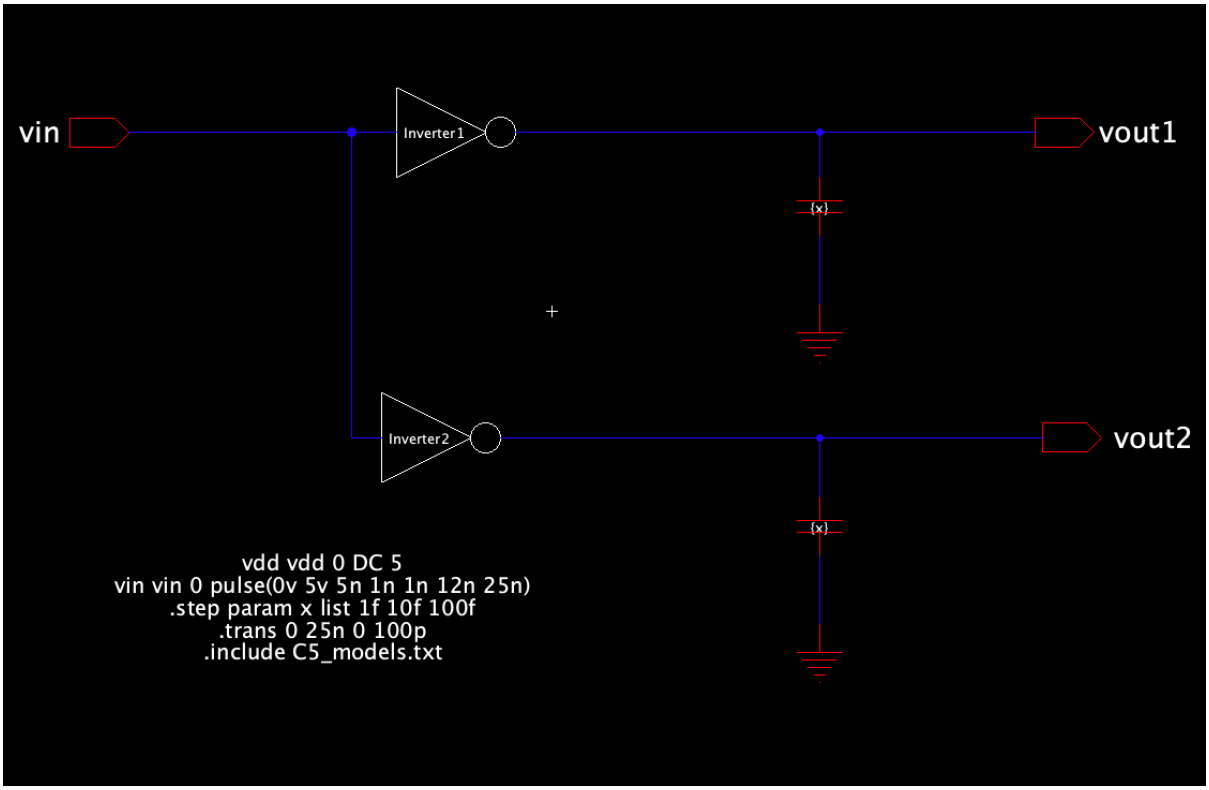


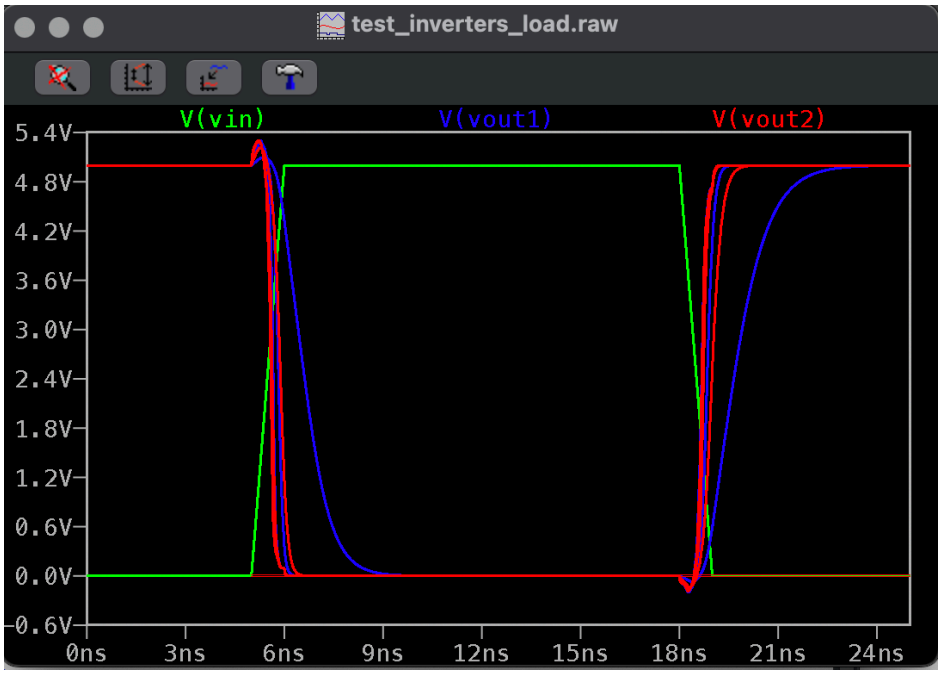

test_inverters.raw
x = 5.220V y = -0.386V
V(vout1)
V(vout2)
V(vin)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V 4.0V 4.5V 5.0V


vin
Inverter1
vout1
{x}
Inverter2
vout2
{x}
vdd vdd 0 DC 5
vin vin 0 pulse(0v 5v 5n 1n 1n 12n 25n)
.step param x list 100f 1p 10p 100p
.trans 0 25n 0 100p
.include C5_models.txt


test_inverters_load.raw
x = 25.67ns y = -0.953V
V(vin)
V(vout1)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0ns
3ns
6ns
9ns
12ns
15ns
18ns
21ns
24ns


test_inverters_load.raw
V(vin)
V(vout2)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0ns
3ns
6ns
9ns
12ns
15ns
18ns
21ns
24ns


vin
Inverter1
vout1
{x}
Inverter2
vout2
{x}
vdd vdd 0 DC 5
vin vin 0 pulse(0v 5v 5n 1n 1n 12n 25n)
.step param x list 1f 10f 100f
.trans 0 25n 0 100p
.include C5_models.txt

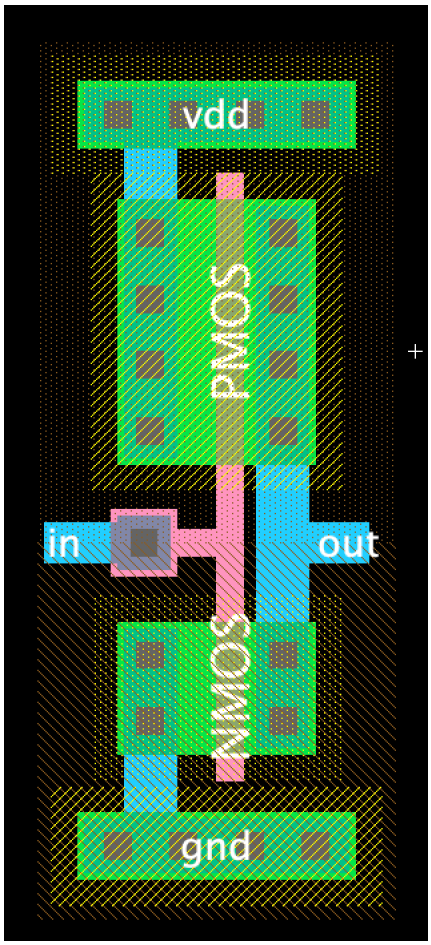

test_inverters_load.raw
V(vin)
V(vout1)
V(vout2)
5.4V
4.8V
4.2V
3.6V
3.0V
2.4V
1.8V
1.2V
0.6V
0.0V
-0.6V
0ns
3ns
6ns
9ns
12ns
15ns
18ns
21ns
24ns

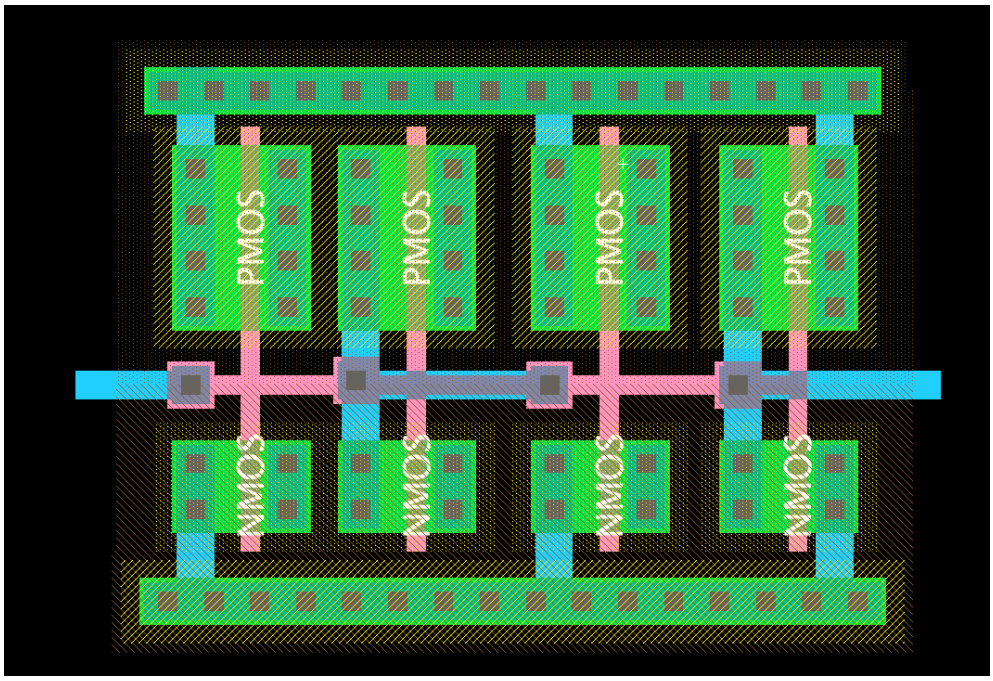
The main goal in designing the inverter schematics was to create two functionally identical circuits with different drive strengths, so we could compare how transistor sizing affects performance. The first inverter used minimum-sized transistors (PMOS 12 μm/6 μm, NMOS 6 μm/6 μm) to establish a baseline. These sizes were chosen to maintain a roughly 2:1 width ratio between the PMOS and NMOS devices, which helps balance the difference in carrier mobility (electrons move faster than holes). This ratio keeps the switching threshold (V_M) close to half of the supply voltage (VDD/2), producing a symmetrical voltage transfer curve and similar rise/fall transition times.

For the second inverter, the transistor widths were increased by a factor of four (PMOS 48 μm/6 μm, NMOS 24 μm/6 μm, using a multiplier M = 4). This was done to reduce the effective on-resistance of each device, allowing the circuit to drive larger capacitive loads more efficiently and switch faster. Using the multiplier instead of a single wide transistor also improves layout compactness and matching, reducing parasitic effects. Both inverters share the same supply voltage, input structure, and output node to make the comparison consistent. The design choices—particularly the width ratio and scaling factor—were made to study how size impacts delay, power consumption, and switching behavior without altering the basic inverter topology.

Layouts:

- The layouts for the inverters, The power should run on the top of the cell via metal1 and ground should run on the bottom of the cell also via metal1.





The layouts were designed to follow standard CMOS layout practices while ensuring clean routing, minimal parasitics, and compliance with DRC and LVS checks. The PMOS transistor was placed at the top inside the N-well, and the NMOS transistor at the bottom in the P-substrate, which follows the conventional inverter structure. The VDD rail was routed across the top in metal1, and the GND rail across the bottom, making it easy to connect multiple cells in a row later on if needed. The input gate was routed vertically using polysilicon to connect both transistor gates, and the output node was formed by sharing the diffusion region between the PMOS and NMOS drains. Sharing this node helps reduce parasitic resistance and capacitance, improving switching performance.

For the larger inverter, a multiplier of M = 4 was used for both transistors. This fingered layout was chosen instead of a single wide device to make routing more compact and to improve current distribution. It also reduces gate resistance and diffusion capacitance, which leads to faster switching and better matching between transistors. Proper well and substrate contacts were added near each device to tie the N-well to VDD and the P-substrate to GND, preventing latch-up and ensuring stable body biasing. Multiple vias were used on high-current paths, especially at the output node and supply rails, to lower contact resistance. Finally, metal layers were organized to keep routing clean and to minimize overlap or spacing violations. These decisions together produced layouts that are efficient, symmetrical, and electrically reliable while maintaining the correct functionality of the schematic.

Conclusion:

In conclusion, This lab was about designing and testing two CMOS inverters with different transistor sizes to see how sizing affects performance. The smaller inverter worked as a baseline, and the larger one, which used a multiplier of four, showed much faster switching and handled bigger loads better. The results made sense — the switching point stayed close to half of VDD, and the wider transistors gave shorter delays and cleaner transitions.

When it came to layout, I focused on keeping everything neat and compact, using shared diffusion areas, proper well and substrate contacts, and multiple vias on the power rails. That helped cut down on parasitics and made the design more reliable overall. I actually found this lab way less challenging than the previous ones, mostly because I've gotten used to using the software and understanding the design steps. It felt good to see everything come together more smoothly this time.