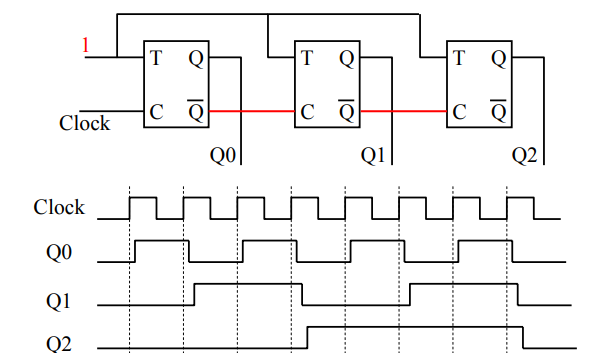
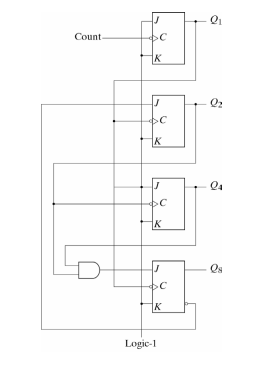
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| **Digital Logic Design** | | |
| Faisal Iradat, PhD | Activity | November 16, 2022 |

1. Given the following Digital Circuit



Derive the values at every rising edge of the clock.

1. Given the following circuit diagram



Draw the timing diagram of the circuit for 10 clock pulses