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Department of Computer Science

Institute of Business Administration, Karachi

Abdullah Iqbal 26904

Lab #11: Shift register and counter design.

Digital Logic Design

# Objective:

The objectives of this experiment are:

1. Use Logisim-evolution to design and analyze a counter.
2. Understanding and designing the shift register with parallel load.
3. Designing a counter using incrementor and parallel load.

**Shift Register with Parallel Load:**

A shift register with parallel load is a digital circuit that combines the features of a shift register with the ability to load data in parallel. In essence, it is a sequential circuit composed of flip-flops where data can be shifted through the register or loaded in parallel. The shift register aspect allows for controlled movement of data in a bit-wise fashion, facilitating tasks like serial-to-parallel or parallel-to-serial data conversion. The distinctive feature of parallel load enhances flexibility by enabling the instantaneous replacement of the entire contents of the register with a new set of bits, making it well-suited for applications requiring both sequential shifting and rapid parallel data loading.

Now, let's move on to an introduction to a counter using an incrementor and parallel load:

**Counter with Increment and Parallel Load:**

A counter with an incrementor and parallel load is a digital circuit designed for counting and storing digital signals. Unlike a simple counter, this type incorporates an incrementer to add a predetermined value to the current count and a parallel load capability for immediate data loading. The incrementer allows for efficient counting operations, while the parallel load feature permits the instantaneous replacement of the counter's content with a new value. This design is particularly useful in applications where precise counting is required, and the ability to quickly load specific count values is essential. The combination of an incrementer and parallel load enhances the versatility and efficiency of the counter in various digital systems and applications.

# Tasks for the Lab

1. Design the following circuit of shift register with parallel load on Logisim evolution.

0

1

0

1

0

1

0

1

2. Design the following counter with parallel load



