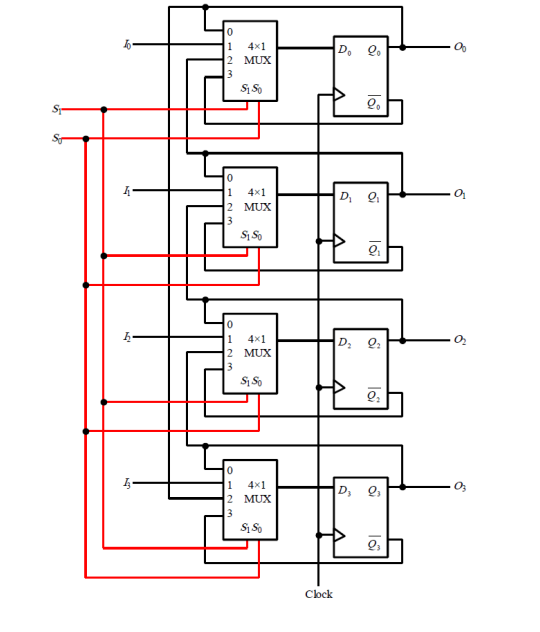
|  |  |  |
| --- | --- | --- |
| **Digital Logic Design** | | |
| Faisal Iradat, PhD | Quiz – 5 | Marks: 20 (Scaled to 2) |

1. Given the synchronous sequential circuit below



1. What circuit is implemented?

[2]

Register with Mode Selection

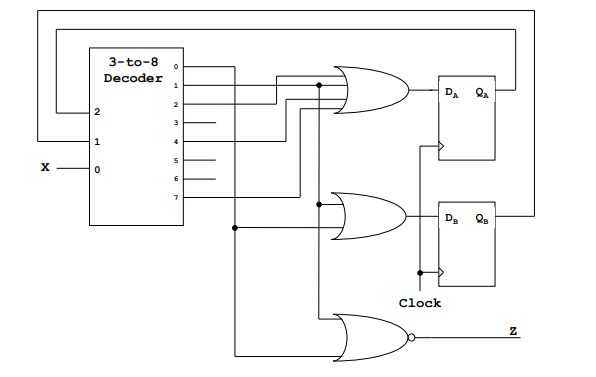
1. The functions of this circuit corresponding to values of S1S0 is incorrectly written below. Reorder the functions for the right values of S1S0

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Functions |
| 0 | 0 | Load with 1’s complement of current value |
| 0 | 1 | Rotate Right |
| 1 | 0 | No change |
| 1 | 1 | Parallel load |

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Functions |
| 0 | 0 | No Change |
| 0 | 1 | Parallel Load |
| 1 | 0 | Rotate Right |
| 1 | 1 | Load with 1’s |

[8]

1. Given the circuit below



1. Draw the stat transition table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Qa | Qb | X | Qa+ | Qb+ | Z |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 |

1. Derive the state transition equations

Da = Sum(1,2,4,7)

Db=Sum(0,1)

Z= Prod(0,1)

1. Draw the state transition diagram
2. Is this a Mealy machine or a Moore Machine?

Moore

[5+3+1+1]

3 x 8 decoder circuit with EN is as follows:

