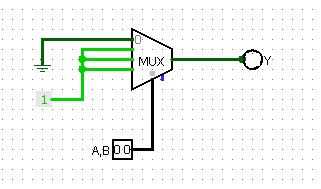
|  |  |  |
| --- | --- | --- |
| **Digital Logic Design** | | |
| Faisal Iradat, PhD | Quiz – 6 | Marks: 20 (Scaled to 2) |

1. For the circuit given below, derive the truth table:

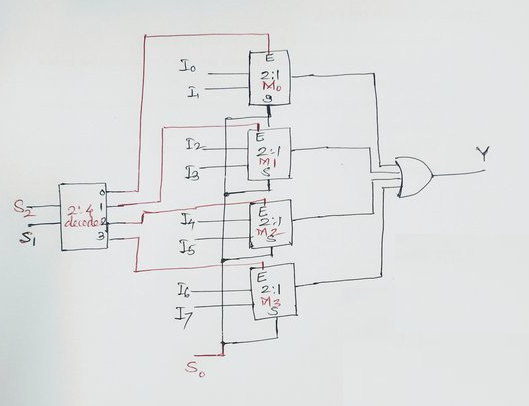


Y = OR Gate

1. Refer to question 1 above, if the first three inputs to the Mux are grounded and the fourth input is made high, derive the truth table.

Y = AND Gate

1. Derive the truth table of the following circuit:



|  |  |  |  |
| --- | --- | --- | --- |
| S2 | S1 | S0 | Y |
| 0 | 0 | 0 | I0 |
| 0 | 0 | 1 | I1 |
| 0 | 1 | 0 | I2 |
| 0 | 1 | 1 | I3 |
| 1 | 0 | 0 | I4 |
| 1 | 0 | 1 | I5 |
| 1 | 1 | 0 | I6 |
| 1 | 1 | 1 | I7 |