Digital Combinational Lock

Introduction

Digital combinational locks are an essential part of security systems in modern electronics. They ensure that only authorized individuals can access specific systems or areas by requiring a predefined sequence of inputs. This project involves designing and implementing a 4-digit digital combinational lock using logic gates and D flip-flops. The circuit ensures security by verifying the correctness of the entered PIN code. If the correct code is entered, a green LED lights up to indicate an unlock signal. Conversely, if an incorrect digit is entered at any position, a red LED and buzzer are activated, signifying a failed attempt.

Requirements

1. Project Objective:

The objective of this project is to design a secure and effective digital combinational lock system that permits access only when the correct 4-digit PIN code is entered. The system incorporates 2-bit and 3-bit shift registers, a magnitude comparator, and combinational logic gates to validate the user input against a pre-saved PIN. If the entered code matches the saved PIN, the system activates an unlock signal (green LED). If any incorrect digit is entered at any stage, the system triggers a red LED and buzzer to indicate failure. This project provides hands-on experience in utilizing D flip-flops, logic gates, magnitude comparators, and sequential circuits to create a practical access control mechanism.

2. Sequential Logic:

The circuit uses D flip-flops as memory elements to sequentially store the input code. Each flip-flop holds one digit of the input sequence, updating the outputs as each digit is entered. The first two D flip-flops with set/reset functionality act as a 2-bit shift register, storing and shifting the input digits. The state of these flip-flops forms the partial "code," which is then compared to the predefined PIN code for the lock to activate.

3. Combinational Logic:

AND and OR gates are used in the combinational logic to compare the flip-flop outputs to the predefined code. The AND gates check if all the correct inputs have been entered, ensuring that the entire sequence is verified. The OR gates are used to aggregate multiple conditions or to reset the error indications. When the correct code is entered, the lock activates, indicated by the green LED. If any digit is incorrect, the error system, consisting of a red LED and buzzer, is triggered to provide immediate feedback.

4. Truth Table & State Diagram:

The behavior of the project is described using a truth table for the combinational circuit and characteristics table for the D flip-flop.

4.1. Characteristic Table For D flip flop:

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

4.2. Truth Table For XOR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

4.3. Truth Table For NOT Gate:

X	Y
0	1
1	0

4.4. Truth Table For 4-input AND Gate:

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

5. Component Selection:

a. 7-segment display
b. 7448/74LS48
c. Magnitude Comparator (74LS85)
d. Priority Encoder (74HC148)
e. D Flip-Flop (74175)
f. D Flip-Flop (CD4013)
g. XOR Gate (74LS86)
h. NOT Gate (74LS04)
i. AND Gate (74LS08)

j. 3-Input AND Gate (74LS11)
k. 4-Input AND Gate (74LS21)
l. OR Gate (74LS32)
m. Resistor 10kΩ, 330Ω
n. Buttons
o. LED Red, Green
p. Buzzer
q. Wires
r. Breadboard
s. Battery

6. Timing Constraints

6.1. Clock Timing: Ensure stable clock pulses from E0 of the priority encoder for synchronous D flip-flops.

6.2. Propagation Delay: Account for delays in synchronous flip-flops and logic gates.

6.3. Response Time: Ensure LEDs and buzzer respond promptly.

6.4. Reset Timing: Reset pulse must quickly clear synchronous flip-flops and logic states.

7. Power Supply & Voltage Levels

Power Supply: The circuit uses a 9V battery to power all components.

Voltage Levels: Operate with the regulated 5V output from the LM7805 voltage regulator to prevent over-voltage issues.

8. Schematic Design:

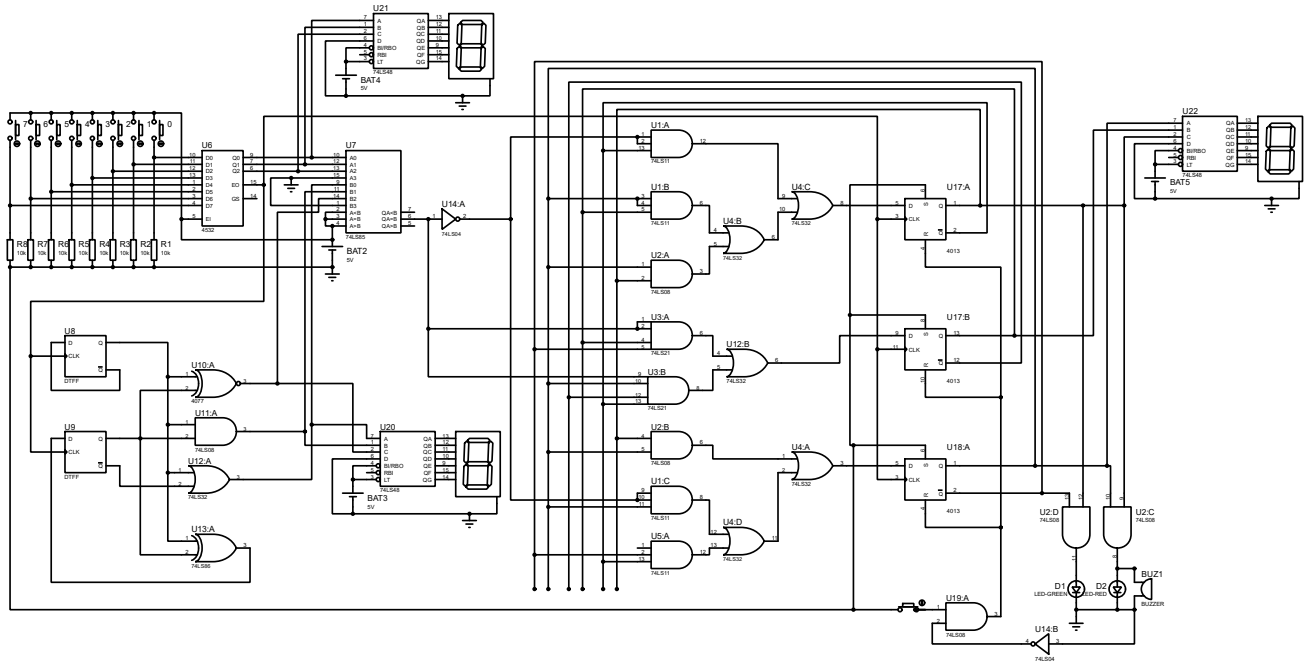

Fig 8.1: Schematic Diagram of Digital Combinational Lock

9. **Simulation:** We simulated the design in Proteus Software based on the schematic diagram and verified its functionality and performance.

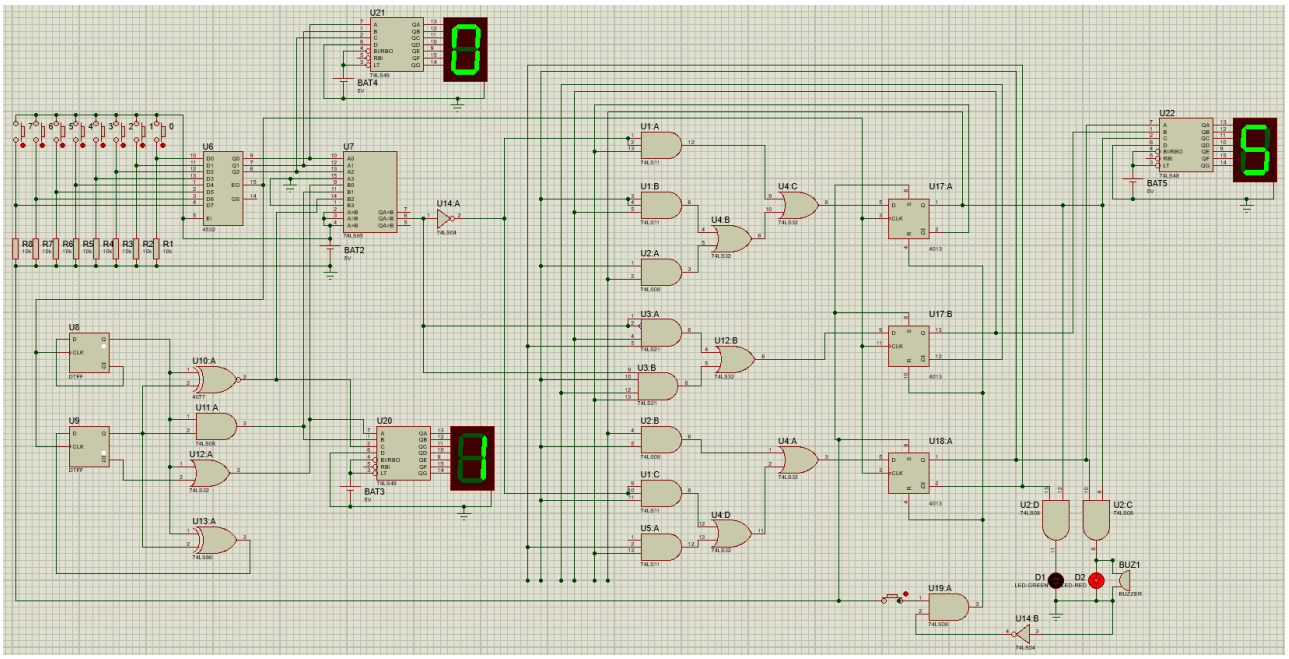

Fig 9.1: Simulation Diagram of Digital Combinational Lock

10. **Prototyping Platform:** We used breadboard as our prototyping platform.

11. **Programming:** Programming is not applicable for this project.

12. **Documentation:** The documentation is completed according to the requirements.

Working Principle

The digital combinational lock operates based on logic circuits and sequential control. The key components include input switches, D flip-flops, AND gates, OR gates, XOR gates, and two 7-segment displays for visual representation of the entered digits. Below is a step-by-step explanation of the working principle:

1. **Input System:**
   - The lock uses a 4-digit PIN code entered using input switches. Each digit is stored and processed in separate D flip-flops to retain the state.
   - The first two D flip-flops (DFFs) with set/reset functionality act as a 2-bit shift register. This 2-bit shift register outputs a signal that is passed into three combination gates to generate a 3-bit combination.
   - The 3-bit combination acts as saved PIN code, which is sent to the magnitude comparator as input B.

2. **Verification Logic:**
   - The user-entered digits from the number pad serve as input A to the magnitude comparator.
   - The magnitude comparator compares inputs A (entered code) and B (saved PIN code). If a match is found, the comparator sends an appropriate signal to another shift register.

3. **Error Indication:**
   - The second shift register consists of **3 D flip-flops (DFFs) with set/reset functionality**, along with numerous **AND gates** and **OR gates**.

- The shift register saves the first three correct digits and monitors the system for the **fourth correct digit**.
- When the fourth correct digit is entered, the shift register sends an **activate signal** to trigger the unlock mechanism, lighting up the green LED.

4. Display System:

- If any digit does not match during verification, the mismatch signal triggers the error system (red LED and buzzer).
- The error system ensures immediate feedback on incorrect inputs.

5. Display System:

- Two 7-segment displays connected to the circuit visually represent the entered digits for user feedback.

6. Reset and Re-entry:

- A reset button is incorporated into the circuit to allow the user to clear the current inputs and re-enter the code if required.

Picture

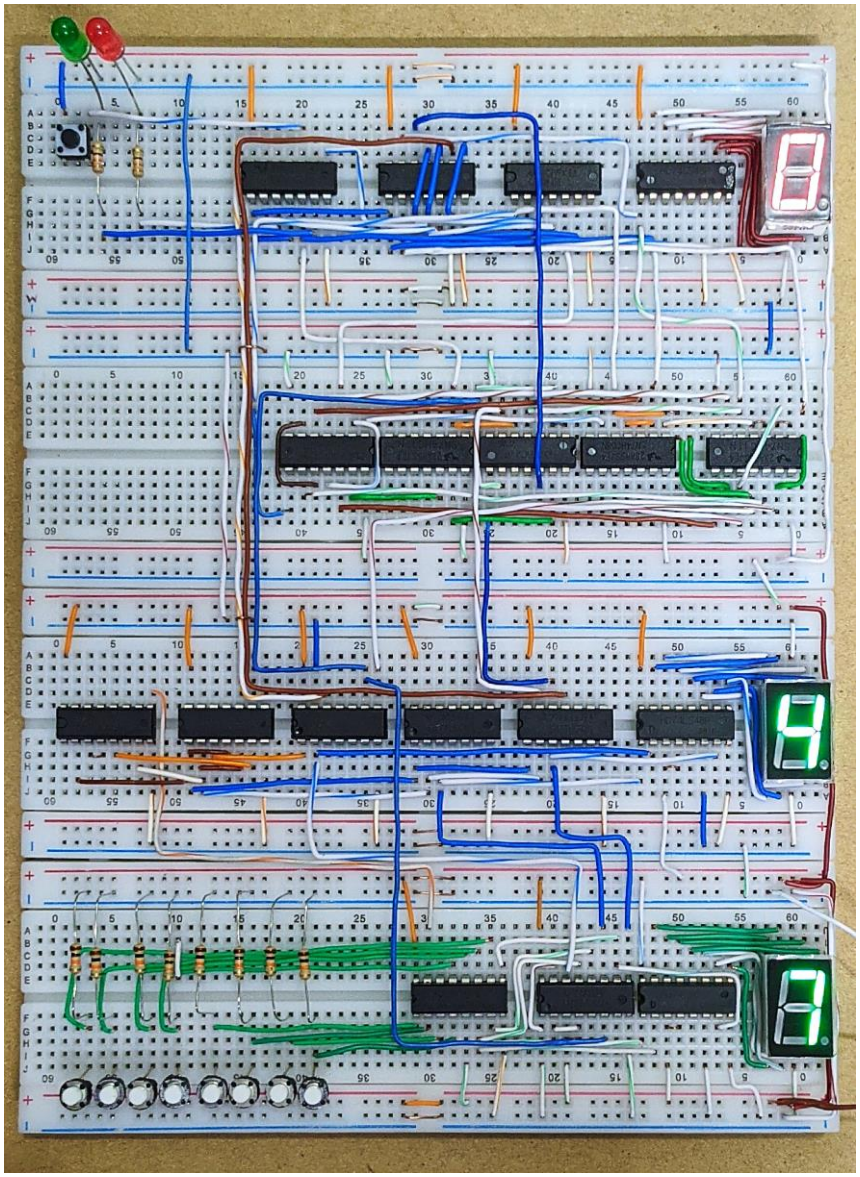

Fig: Digital Combination Lock on a Breadboard

Cost Calculation

Component	Quantity	Unit Price (BDT)	Total Price (BDT)
Combinational & Sequential ICs	13	25	325
7-Seg Decoder	3	35	105
Priority Encoder	1	45	45
Magnitude Comparator	1	45	45
7-Seg Display	3	25	75
Resistors – 10kΩ, 330	12	-	10
Buzzer	1	20	20
9V Battery with Connector	1	70	70
Voltage Regulator LM7805	1	10	10
LED	2	4	4
Bread Board	4	120	480
Buttons	8	3	24
Wires	-	50	50
Total			**1263**

Conclusion

This project demonstrates a practical implementation of a digital combinational lock using fundamental digital electronics concepts. The system uses shift registers, combination gates, and a magnitude comparator to ensure accurate verification of the entered PIN code. By utilizing sequential control and logic gates, the design securely validates user inputs and activates the unlock mechanism only when the correct code is entered. The addition of error indication mechanisms, such as the red LED and buzzer, enhances the security and usability of the system. This design can be extended or integrated into larger systems requiring secure access control.