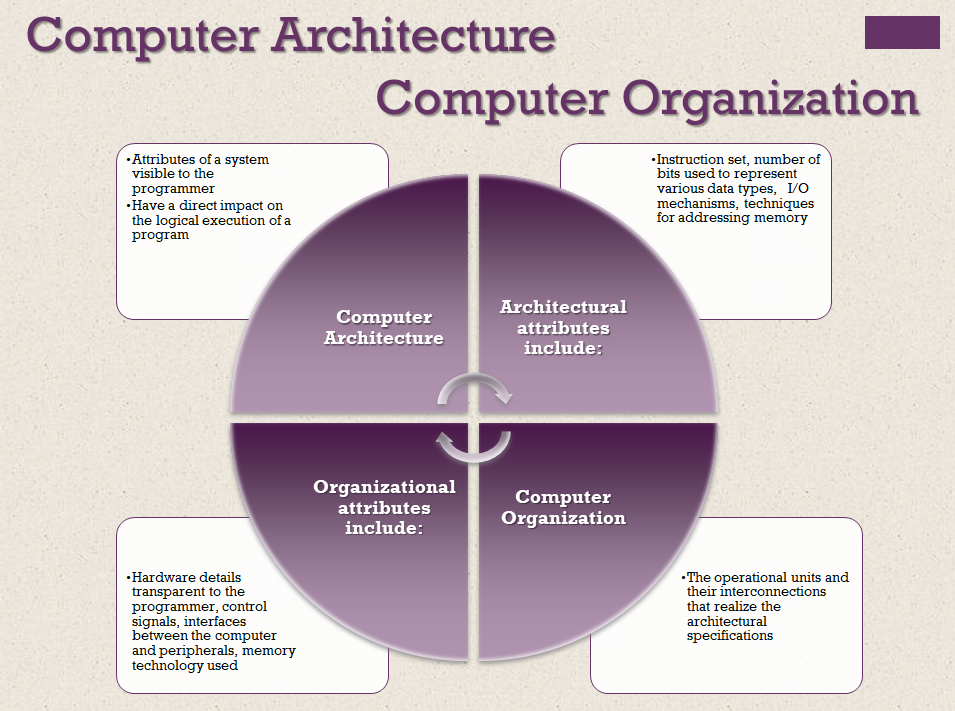
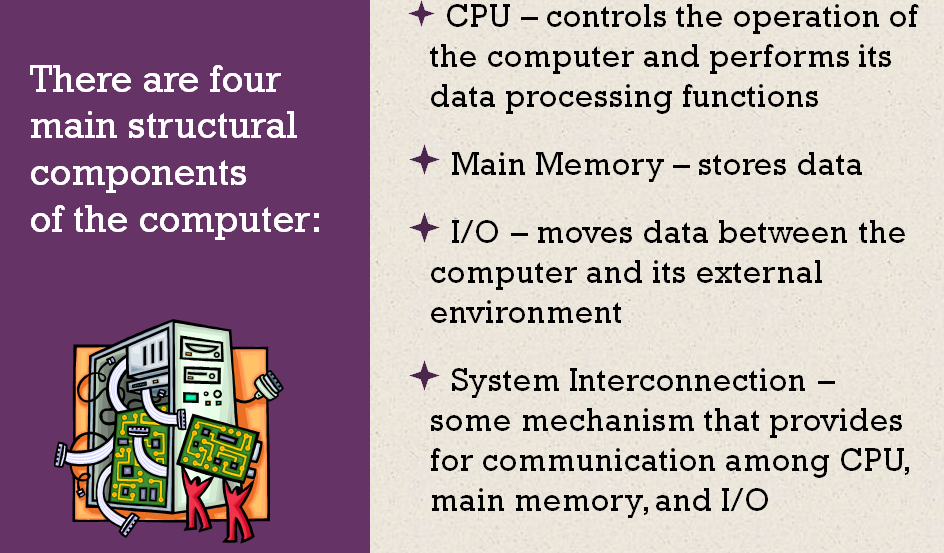
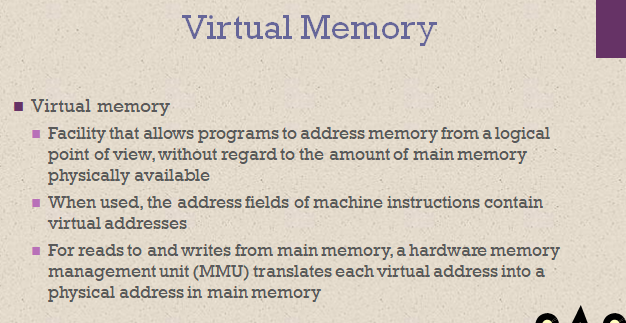
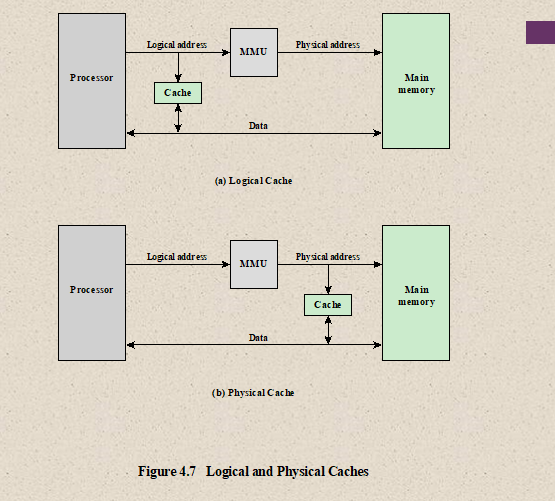
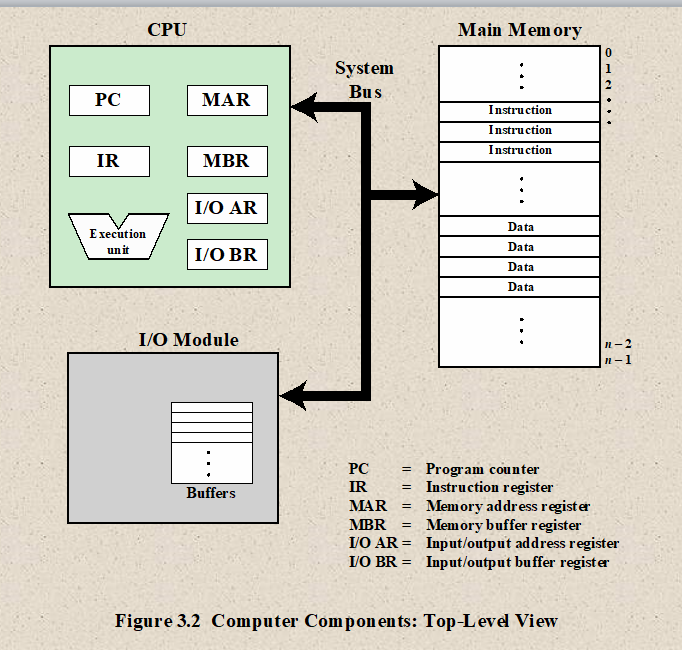
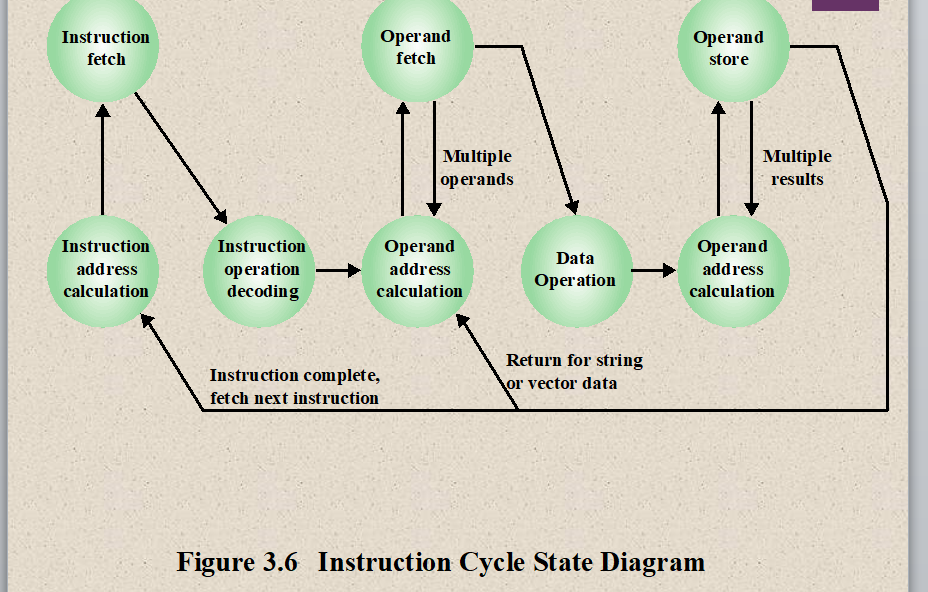
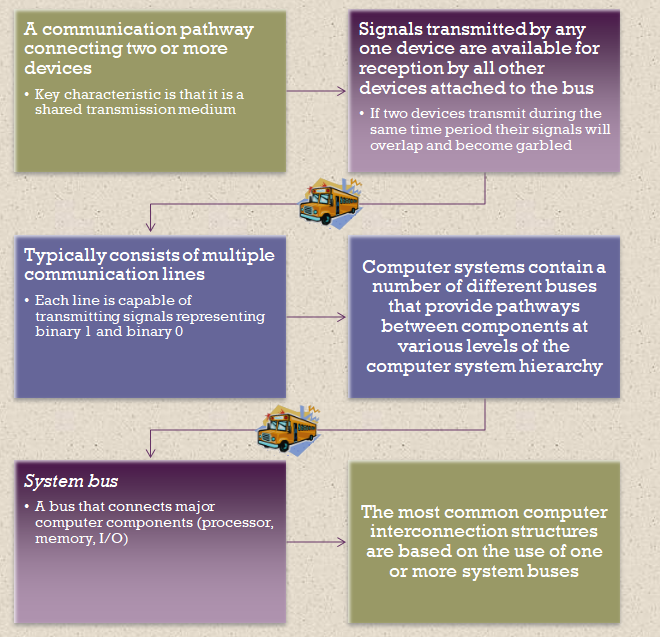
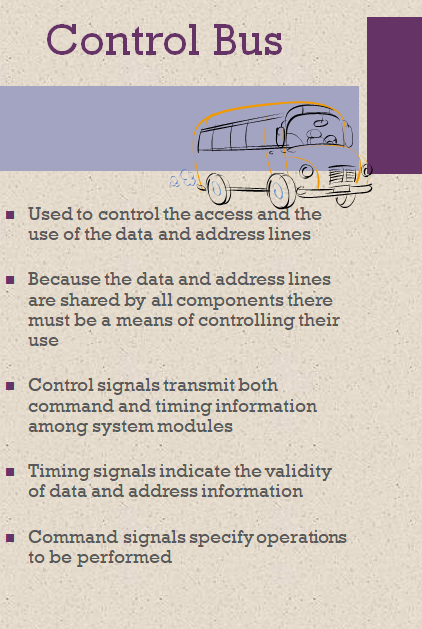
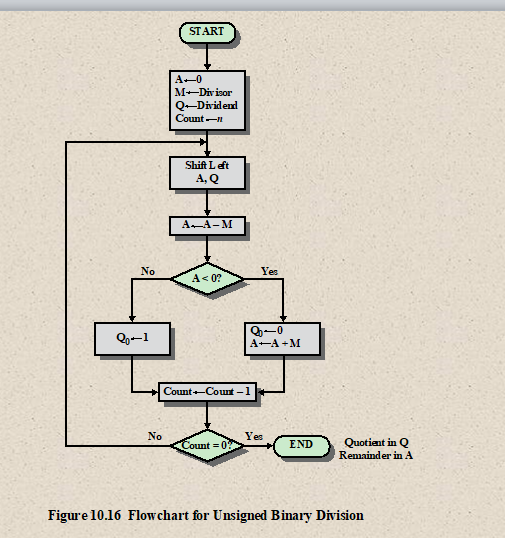
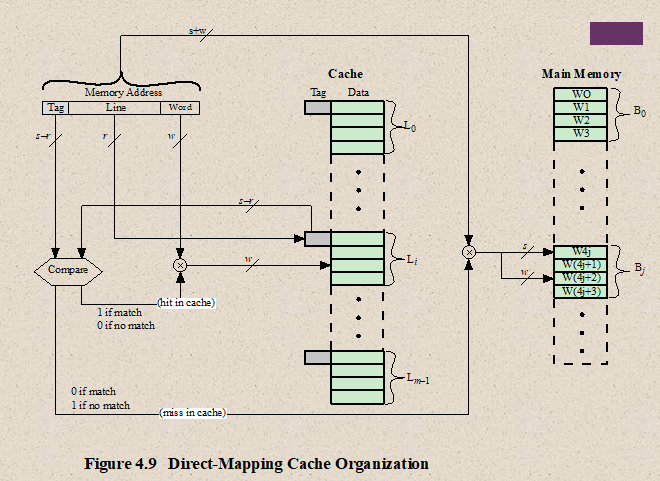
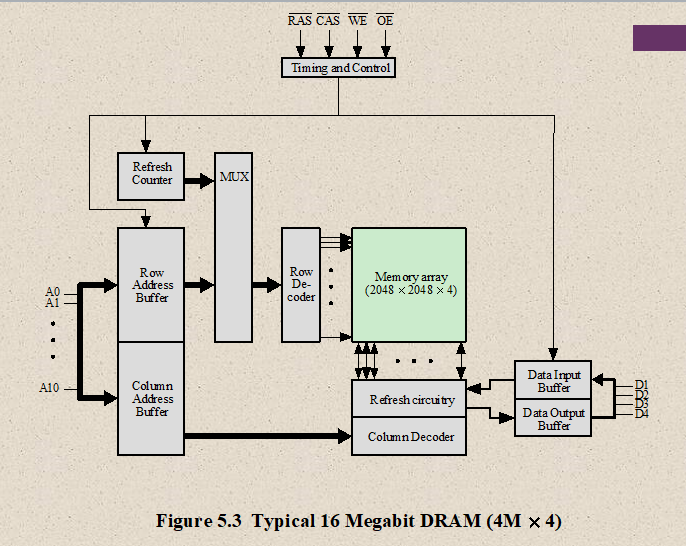
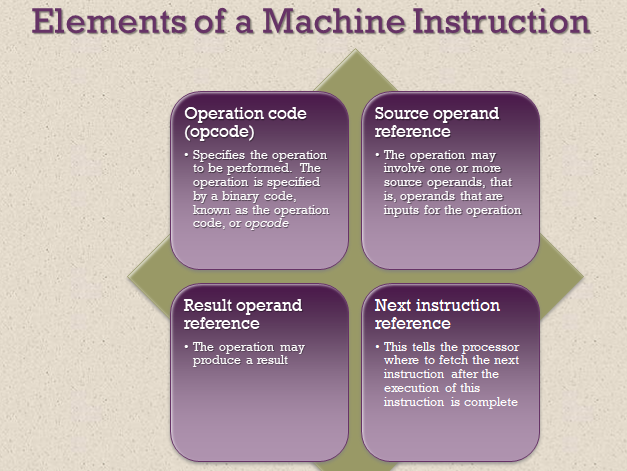
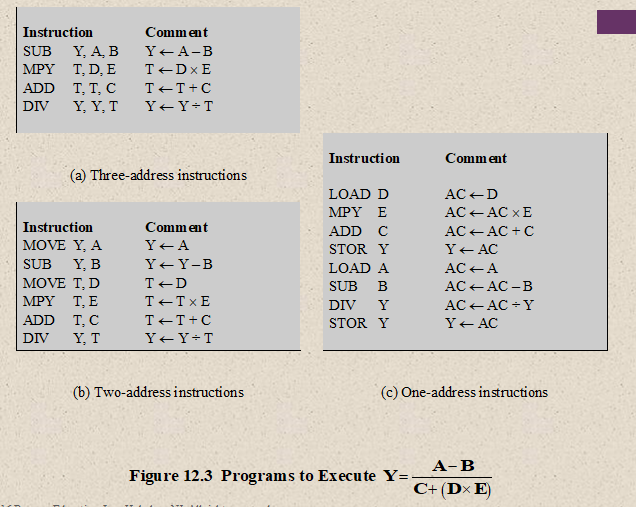
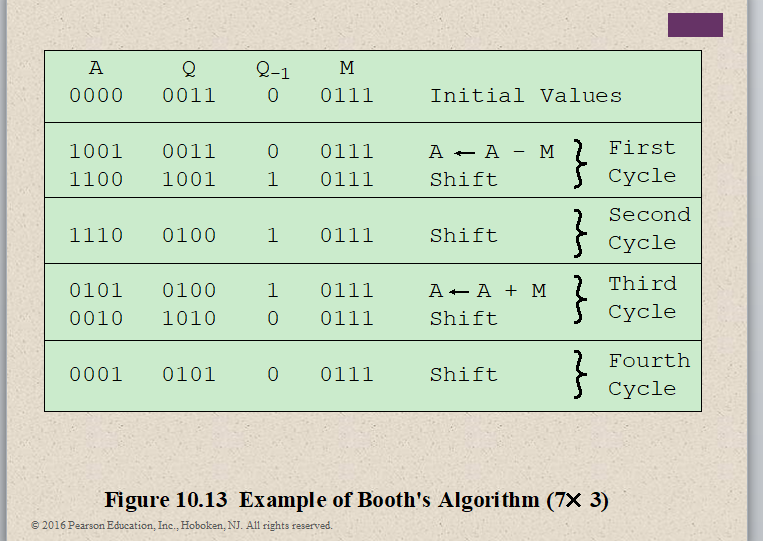
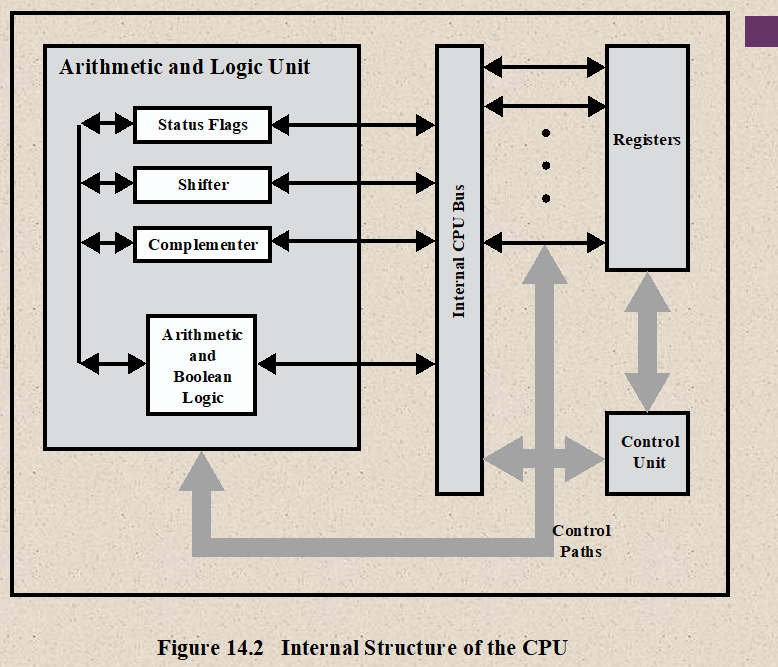
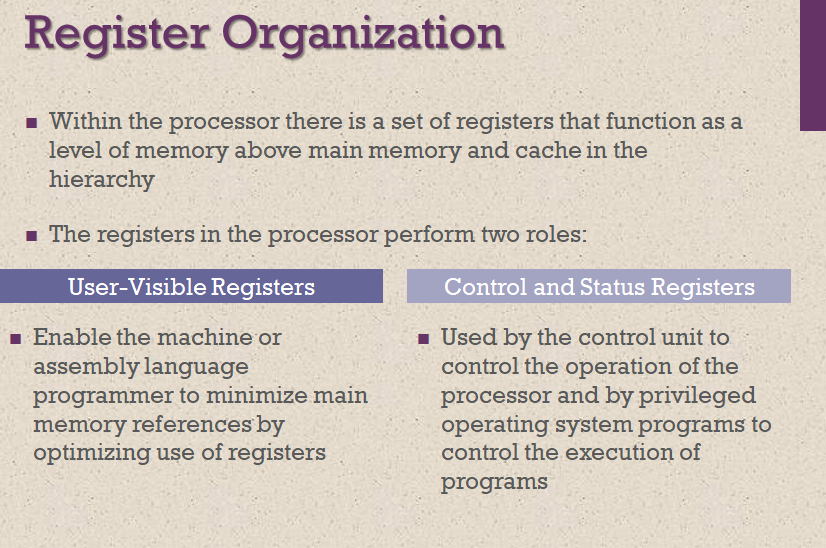
1. Computer Architecture and Organization(Dfine)

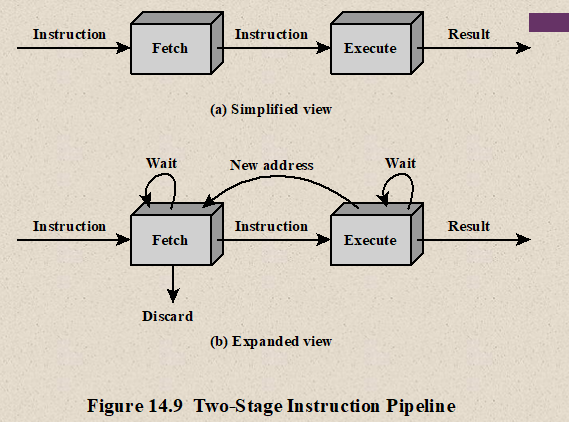
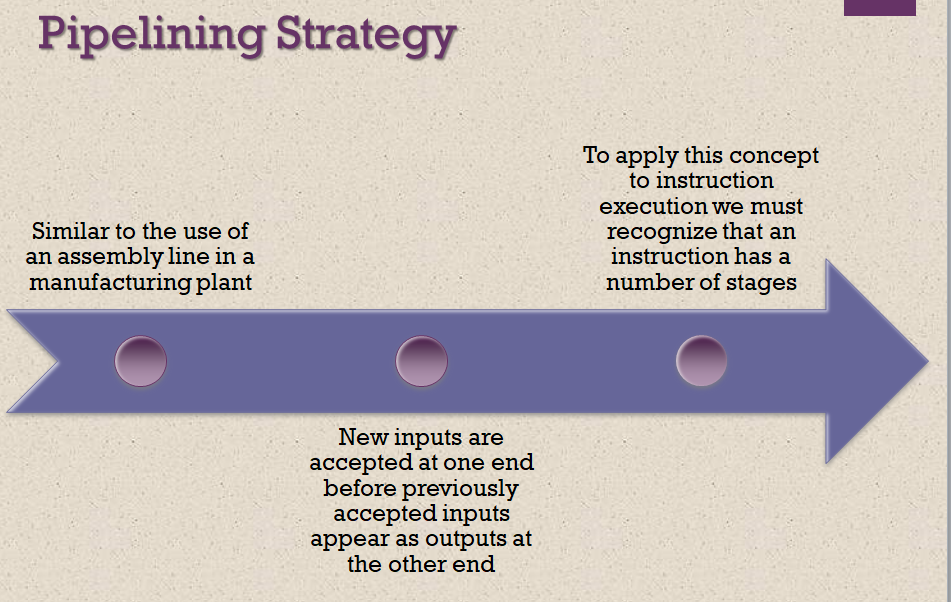
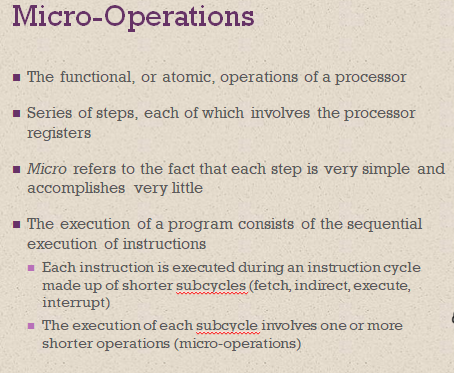
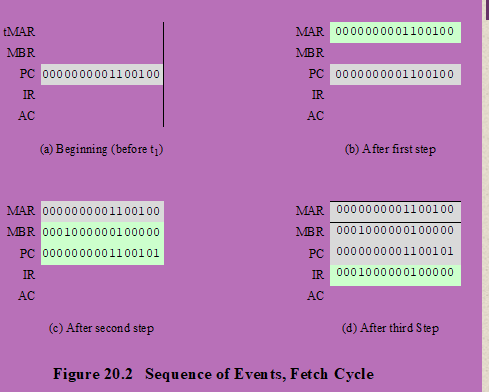


1. System Bus (Define)
2. Main Structural Components of a processor
3. Virtual memory
4. Outline the notion of binary representation of instruction
5. Difference between Logical cache and Physical cache
6. Using top-level view of computer components, explain the basic functions performed by a computer (with necessary diagram). 
7. Describe the possible states of an instruction execution with state diagram. 
8. Illustrate the bus interconnection scheme and explain the control lines of the control bus. 



1. Explain the non-restoring division algorithm showing the flow chart of hardware implementation. 
2. Illustrate direct mapping cache organization. 
3. Demonstrate the internal organization of an 8 Megabit DRAM (2Mx4) with proper explanation. 
4. Construct a memory chip of 1M words by 8 bit per word using memory chips of 256K words.
5. Suppose, the size of the multiple block cache is 64kb and total block size is 32 bit. Now, considering two-way set associative cache and 32-bit physical address, provide the details of division among index, tag and block of set.
6. Analyze the elements of a machine instruction. Categorize different addressing modes with the necessary diagram and description in brief. 
7. Compare one-, two-, and three-address instructions that could be used to compute **Y = (A – B)/[C + (D × E)]**. 
8. Figure out the steps of multiplication process using Booth algorithm of the following binary numbers: **Y = 8 × 10 (Same as)**
9. Differentiate between address space and memory space. An address space is specified by 2 bits and the corresponding memory space by 16 bits. If a page consists of 2K words, calculate the number of pages and blocks in the system.
10. i. Explain the internal structure of the CPU with block diagram. 

ii. Describe the register organization of the CPU and explain the functions of each register. 

1. **i.** Explain the concept of instruction pipeline strategy. Give the simple approach of two-stage instruction pipeline with necessary diagram.   
   **ii.** Write the sequence of events for the fetch cycle from the point of view of its effect on the processor registers. Give an example in context of micro-operations. 
2. **i.** Design a circuit to implement an **AND** and **XOR** logic microoperations.  
   **ii.** Explain different types of interrupt in a microprocessor system.