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Ques Solve

2

Internal structure of MS-DOS and UNIX OS :

MS-DOS :

In MS-DOS on Intel 80x86, there are 4 ~~OP~~ relocation registers.

In basic MMU setup, relocation register is used. The MMU adds the value of relocation register to each logical address, producing the correct Physical address.

In MS-DOS, there are 4 relocation register.

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UNIX :

In Unix, Linux, Windows ; modified version of two Swapping is used :

→ Swapping normally disabled

→ activates when memory usage exceeds a certain threshold

→ disable again if the usage is below threshold.

Difference between internal - external fragmentation :

Fragmentation is a condition in memory management where the available memory space is wasted.

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External	Internal
Total memory space exists to satisfy a request, but it's not contiguous.	occurs when allocated memory is slightly larger than requested memory
occurs outside of allocated memory block.	occurs inside allocated memory block.
caused by dynamic allocation of memory.	caused by fixed size allocation block.

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3

Swapping techniques on mobile System:

Swapping is a memory management technique where the process temporarily swap in and out of the main memory to backing store.

In modern OS system, standard swapping is not used. A modified version is used, that is:

→ swap only when free memory is extremely low. Otherwise swapping is disabled.

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3(a)

holes: 10 kB, 4kB, 25 kB, 18 kB, 7 kB, 8kB.

~~(i) 12kB~~:

(a) first-fit: first hole that is large enough.

(b) best-fit: smallest hole that is large enough
⇒ check ~~all holes~~ entire list.

(c) worst-fit: largest hole.
⇒ check ~~all holes~~ entire list

For (i) 12 kB:

first fit: 25 kB

best-fit: 18 kB

worst fit: 25kB

For (ii) 10kB:

first fit: 10kB

best fit: 10 kB

worst fit: 25 kB

For (iii) 9 kB:

first-fit: 10kB

best-fit: 10 kB

worst fit: P 25kB

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In terms of speed and storage utilization, first-fit and best fit are better than worst fit.

→ Best fit is most efficient if the goal is to maximize memory usage with minimal internal waste.

→ First fit is a good comparison.

4(b) segment-table.

Segment	Base	Length
0	219	600
1	2300	14
2	90	100
3	1352	580

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→ check if offset within the length of "length"

⇒ Physical address = base + offset

~~Diff (1) = 30~~

			Physical address.			
Segment	Base	length	30	110	2400	4900
0	219	600	249	329	Invalid	Invalid
1	2300	14	Invalid.	Invalid	Invalid	"
2	90	100	120	Invalid	Invalid	"
3	1352	580	1382	2734	Invalid.	"

30

Segment 0: Physical address = base + Offset
= 219 + 30 = 249

Segment 1: 30 > Segment length (14)

∴ Invalid.

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Segment 2:

Physical address = 30 + 90

= 120

Segment 3:

Physical address = 30 + 1352

= 1382

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4(e) difference of external- internal fragmentation ✓

Possible solution of external fragmentation : Paging

~~AP~~

Paging is a memory management technique that ~~avoid~~ eliminates the need of contigious allocation of physical memory.

→ Avoid external fragmentation

→ Avoid the Problem of varying size memory chunks.

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(b) Hardware Address Protection technique with base and limit register:

In segmentation, the base and limit register provide hardware based address protection.

base register : hold the starting address of each segment.

limit register : defines the maximum length of each segment.

How it works :

→ The CPU generate the logical address (s, d)

s → segment No.

d → offset.

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→ using the segment Number (s), the system retrieves the base and limit from the segment table.

→ If the offset (d) is within the limit, the physical address is calculated as,

Physical address = base + offset

⇒ If d (offset) exceeds limit, addressing error occurs, and the address is denied.

- This setup ensure that each segment has controlled access, ensuring hardware address protection
- Each entry in the segment may have protection bit including : validation bit, and read/write/execute privileges.

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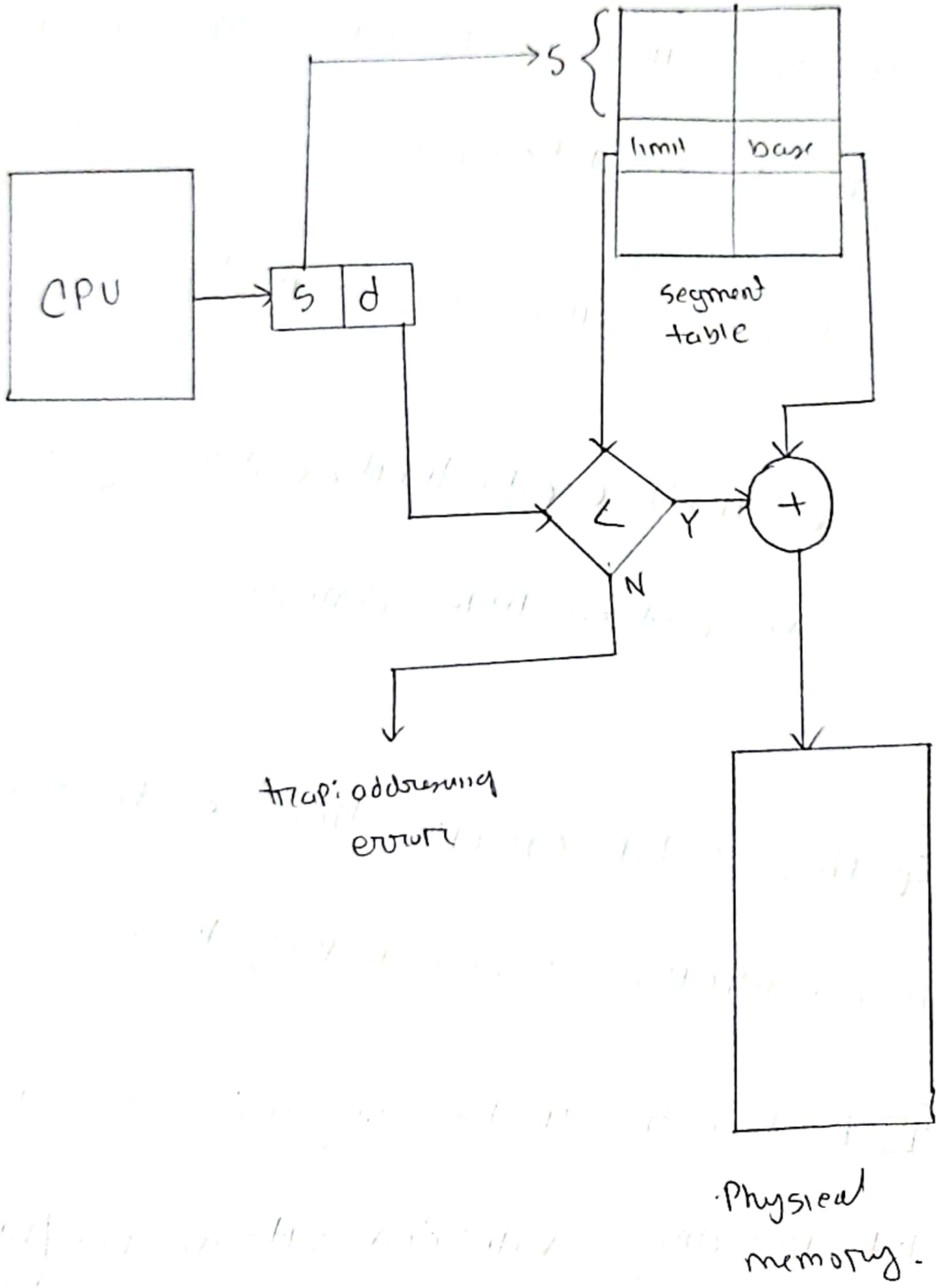
fig Segmentation Hardware



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logical address : logical address is the address that is generated by the CPU. It's the address that Program uses and see.

Physical Address : Physical address is the actual memory location where the data is stored.

Bits in logical Address

64 Pages

1024 words each page

total bits = $\log_2(64) + \log_2(1024)$

$= 6 + 10$

$= 16$

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Bits in Physical Address

32 frames.

1024 words each frame

$\therefore \log_2(32) + \log_2(1024) = 5 + 10$

$= 15$ bits

(1) In Paged memory system without TLB, two memory access is required:

→ access to page table

→ access to actual Physical memory to retrive the data

∴ Page memory reference will take

$(50 + 50)$ ns

$= 100$ ns

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(11) with TLB,

effective memory reference time =

Hit (TLB + Main Memory) + Miss (TLB + PT + Main Memory)

= 75% (2ns + 50ns) + 25% (2 + 50 + 50)

TLB = 2ns

= 0.75 (52) + 0.25 (102)

= 64.5 ns.

Ans)

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7

External Fragmentation in contiguous memory allocation :

Total memory space exists to satisfy a request, but it is not contiguous.

In contiguous memory allocation, a single continuous block of memory is allocated to each process. Over time, processes are loaded and removed from the memory, small gaps form between allocated memory segments. These gaps are external fragments.

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Even through there maybe free memory overall, it maybe fragmented such that a new process can't be loaded because there isn't a single block large enough.

How paging removes external fragmentation :

Paging is a memory management technique that divides both logical and physical memory into fixed sized blocks.

When a process is loaded, it's pages can be placed into any available memory frames in physical memory, not need to be in contigous manner.

So, external frag. removed.

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Appropriate Measure of Memory Protection in memory management Process :

- Memory Protection is implemented by associating Protection bit with each Frame to indicate read-only or read-write access is allowed.

can also add more bits to indicate execution-only and so on.

- valid-invalid bit is attached to every entry in the Page Table.

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⇒ 'valid' indicates that the associated page is in the process' logical address space.

⇒ Invalid indicates that the associated page is ~~in~~ # not in the process' logical address space.

If a process tries to access memory location in a way that violets the protection rule, and will result in a trap to the kernel.

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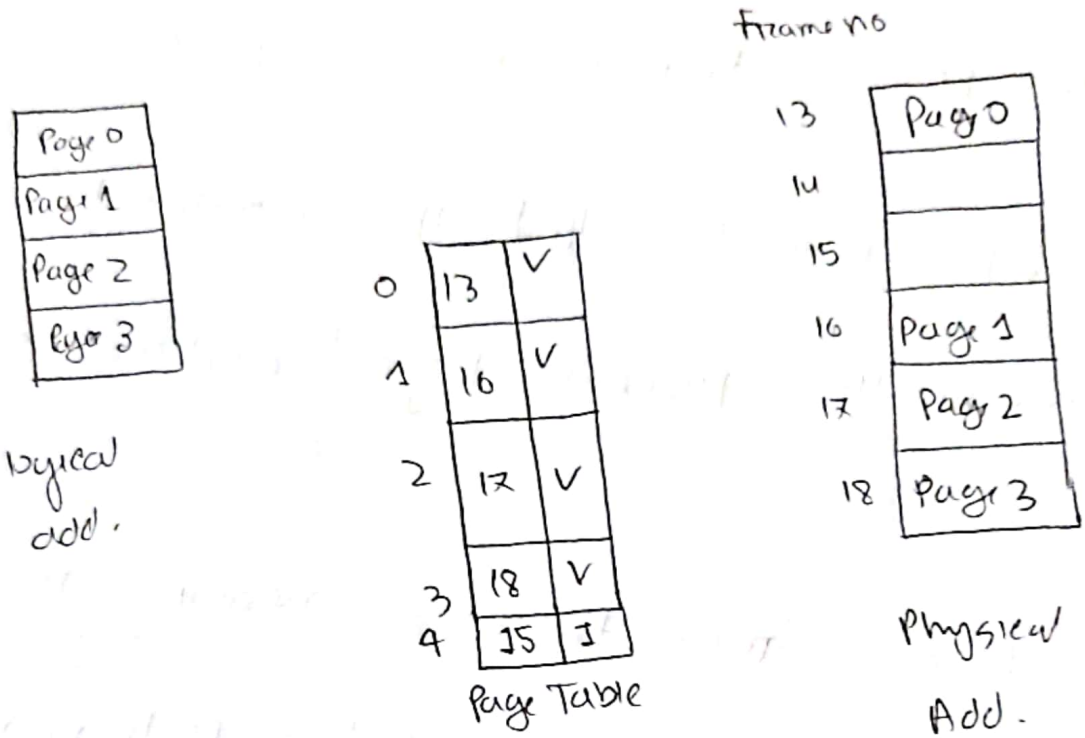

fig. valid-invalid bit in Page Table.

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4(b) Supiruty of Internal fragmentation over external fragmentation :

While both fragmentation waste space, internal frag is more ~~mang~~ managable and predeetable, making it prefairable over external fragmentation.

[external - internal definations + info from difference table.

- In scheme with internal frag (ex. Paging) memory is divided into fixed size blocks, making allocation straightforward.
- Internal frag waste small amount of space.
- External frag. may require compaction
  - ↳ rearranging memory contents to form a large continuous block.

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4(d)

Hit = 75%

Main memory time = 50 ns

TLBs takes 2ns

∴ effective memory reference time =

$$0.75(50+2) + 0.25(50+50+2) \text{ ns}$$

= ✓

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9(e)

logical address space = 8 bit = m

Physical address space = 10 bit

Page size = 32 bytes.

(i) No of virtual page :

$$\text{No of virtual Pg} = \frac{\text{logical Address Space}}{\text{Page size}}$$

$$\text{logical address space} = 2^m = 2^8 = 256 \text{ bytes}$$

$$\therefore \text{Pages} = \frac{256}{32}$$

$$= 8 \text{ Pages.}$$

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(11) No of Physical Pages :

Physical Address space = 2^{10} = 1024 byts.

: No of Py = $\frac{1024}{32}$ = 32 Pags.

(111)

The number of ~~frame~~ in physical Addrss Space is the same as the ~~page size~~ physical Pages (11)

that is = 32

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Function of valid-invalid bits in Page Table : ✓ + pic

11

3)b Address Binding :

Address Binding is the Process of linking a Program address to Physical memory location.

Programs waiting on a disk to be executed ~~must~~ are placed in an input queue.

Addres are represented in different ways in different Stage of Program life.

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Address binding of instruction and data to memory addresses can happend at 3 different stages :

compile time :

If the memory location is known in advaneed, absolute code can be generated.

→ This means the program is bound to specific memory location at compile time

→ If the location changes, Program must recompile.

load time :

If the memory addres is unknow, then relocatable code is generated.

The program can be loaded into any available memory space.

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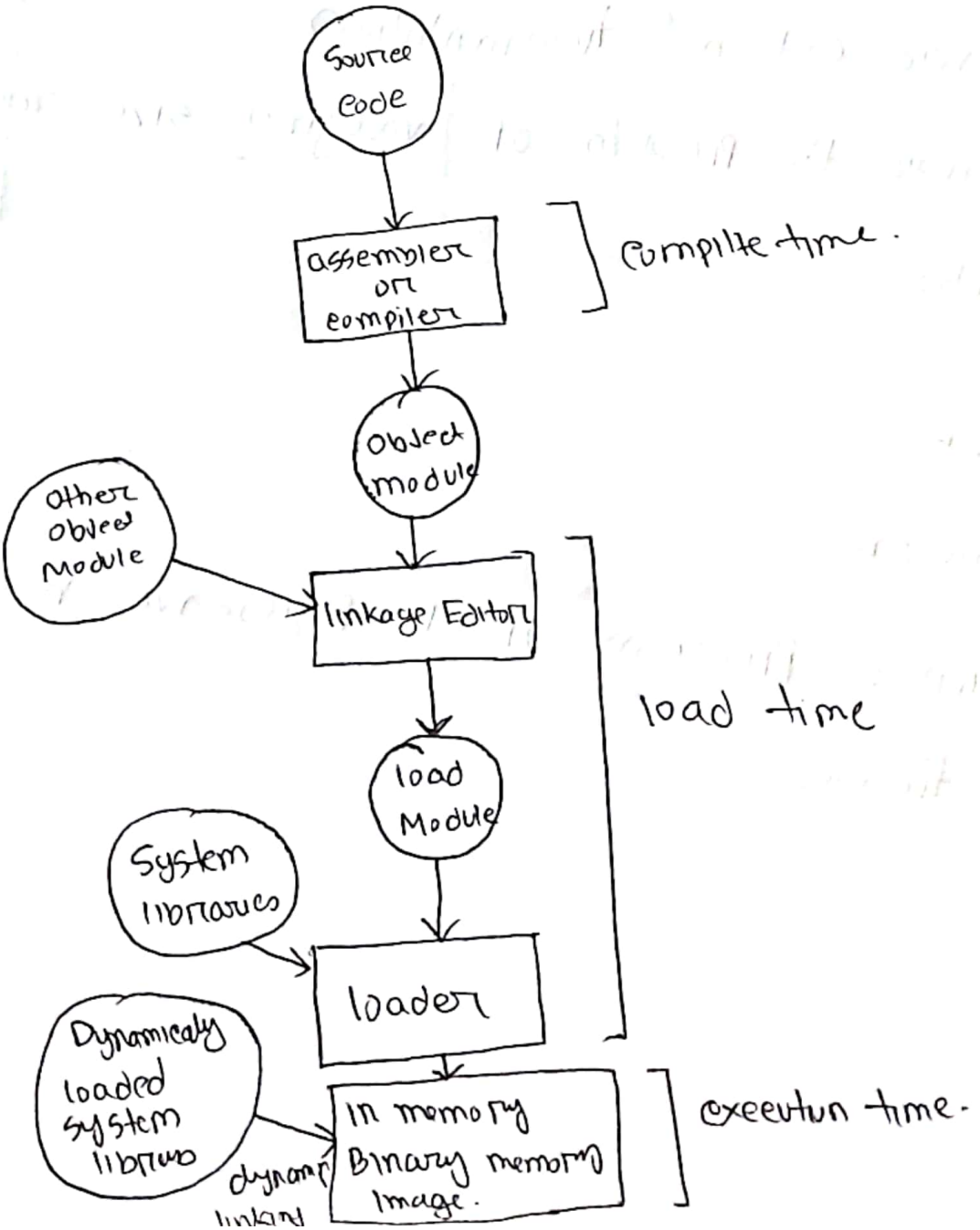
Execution time :

Binding delayed until runtime if the process can be moved during its execution from one memory segment to other.



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Paging Hardware with memory diagram :

Paging is a memory management scheme that eliminates the need of contiguous allocation of Physical ~~on~~ memory

→ avoid external fragmentation

→ avoid the Problem of varying size memory chunks.

Page : ✓

Frame : ✓

To run a Program of N Pages, we need N free frames

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4(d) Paging Hardware with necessary diagram :

Paging is a memory management scheme that eliminates the need of contiguous allocation of physical ~~on~~ memory.

→ avoid external fragmentation

→ avoid the problem of varying size memory chunks.

Page : ✓

Frame : ✓

To run a program of N pages, we need N free frames

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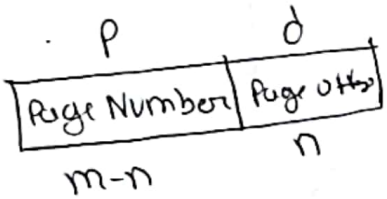
The address generated by CPU can be divided into:

~~two~~

Page Number (P): used as an index into a Page table which contains base address of each Page in Physical memory.

Page offset (d): combined with base address to define the Physical memory address that is sent to the memory unit



Address space = 2^m

Page size = 2^n.

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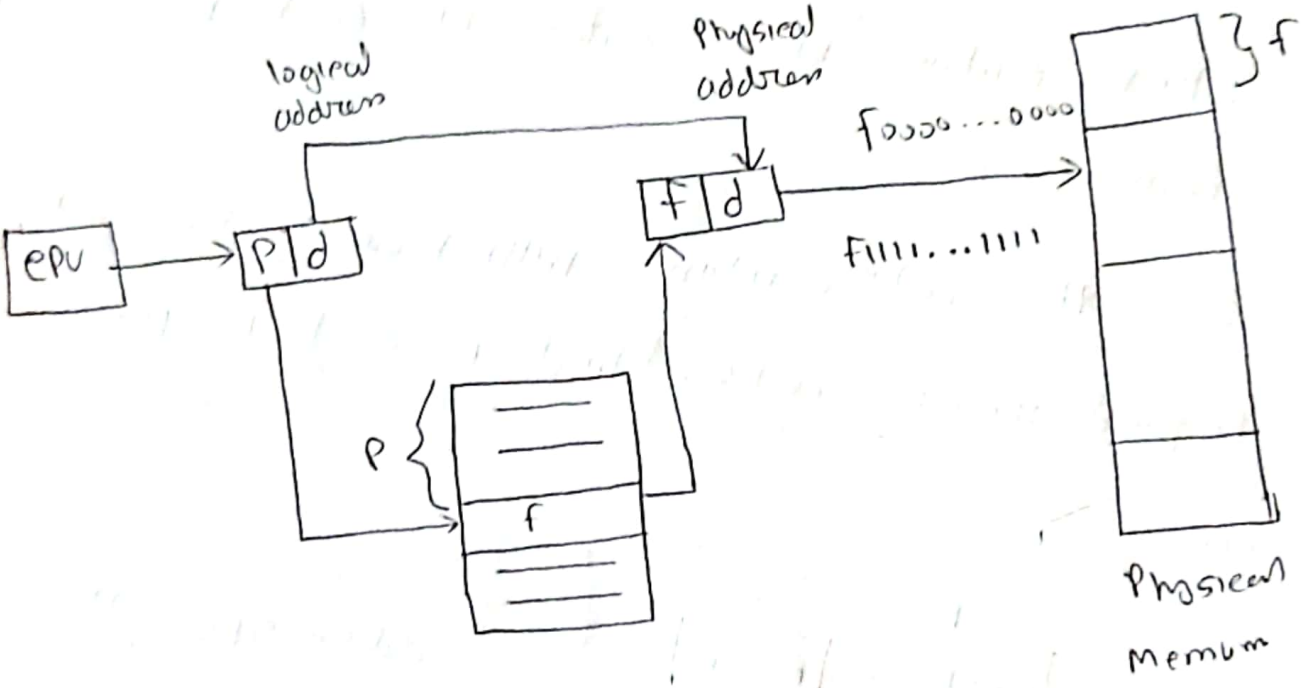
fig. Paging Hardware



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5(e) (i)

memory reference time = 70 ns

Paged memory reference time = (70 + 70) ns

= 140 ns

(ii)

Effective memory reference time

= 0·80 (70+2) + 0·80 (70+70+2)

= ✓

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Showing Paging scheme :

logical memory = 24 byte

Physical memory = 48 byte.

Page size = 6 byte.

word size = 1 byte.

no of Pages in logical memory = $\frac{24}{6} = 4$ Pg

∴ frames, Physical " = $\frac{48}{6} = 8$ frames.

∴

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Showing Paging scheme :

logical memory = 24 byte

Physical memory = 48 byte.

Page size = 6 byte.

word size = 1 byte.

no of Pages in logical memory = $\frac{24}{6} = 4$ Pg

" frames, " Physical " = $\frac{48}{6} = 8$ frames.

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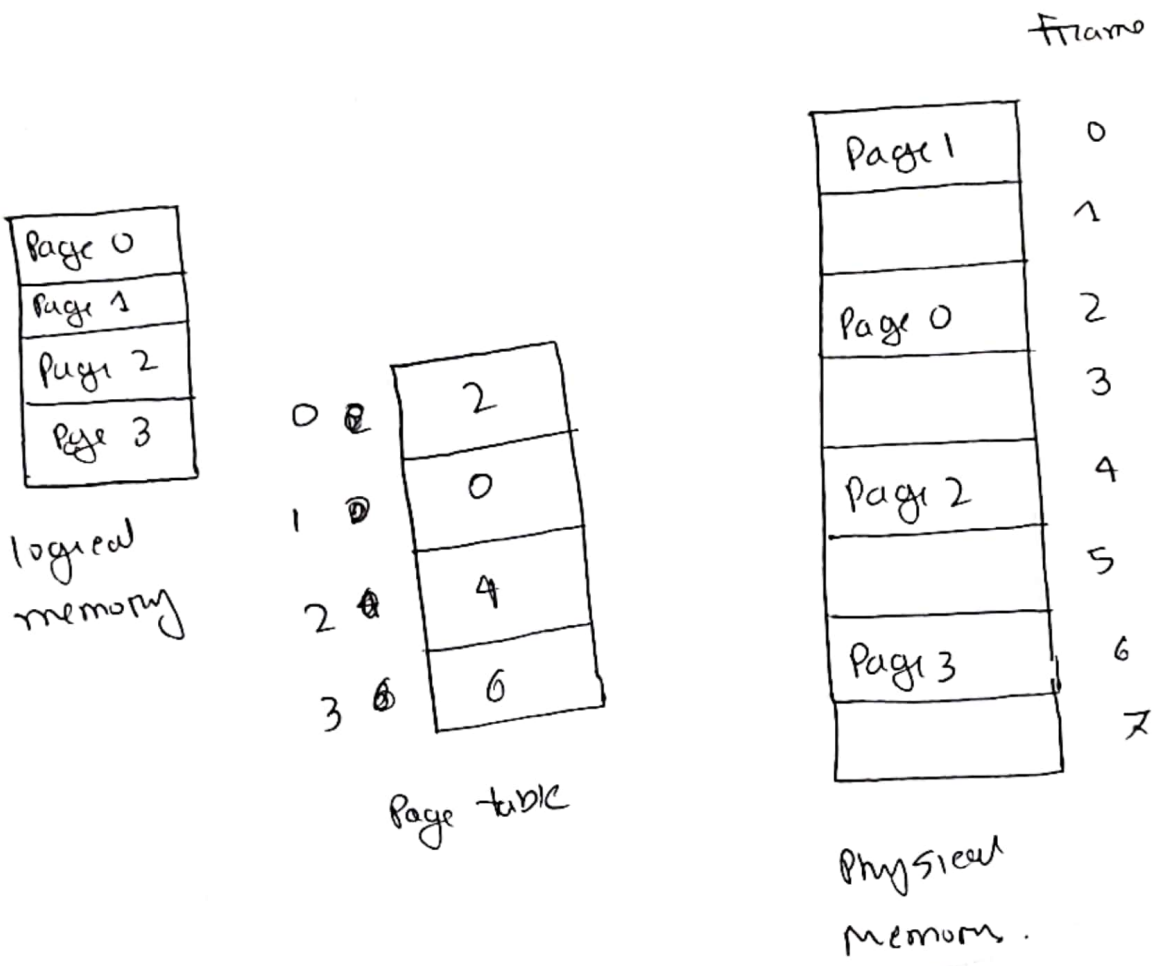

fig. Paging method.

[observe --]