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Question1) Since data bus is 8-bits I am assuming that a word is also 8 bits thus the general structure of the memory is going to be as below:


$4K = 2^{12} = 4096$

So we can use the x4 memories together to store a single word and the x8 can be by itself
$4K + 4K = 8K$ ✓

| | $A_{15}A_{14}A_{13}A_{12}$ | $A_{11}A_{10}A_9A_8$ | $A_7A_6A_5A_4$ | $A_3A_2A_1A_0$ | |
|---|---|---|---|---|---|
| \$6000 = | 0110 | 0000 | 0000 | 0000 | MeMx |
| \$6FFF = | 0110 | 1111 | 1111 | 1111 | MeMY |
| \$7000 = | 0111 | 0000 | 0000 | 0000 | MeM Z |
| \$7FFF = | 0111 | 1111 | 1111 | 1111 | |

So the address range is from \$6000 – \$7FFF

b) From part @ we see that up until $A_{11}$ the bits change within the same memory module and if $A_{12}$ changes we change the memory module itself. First Module being MeMx and MeMY, second module being MeM Z.

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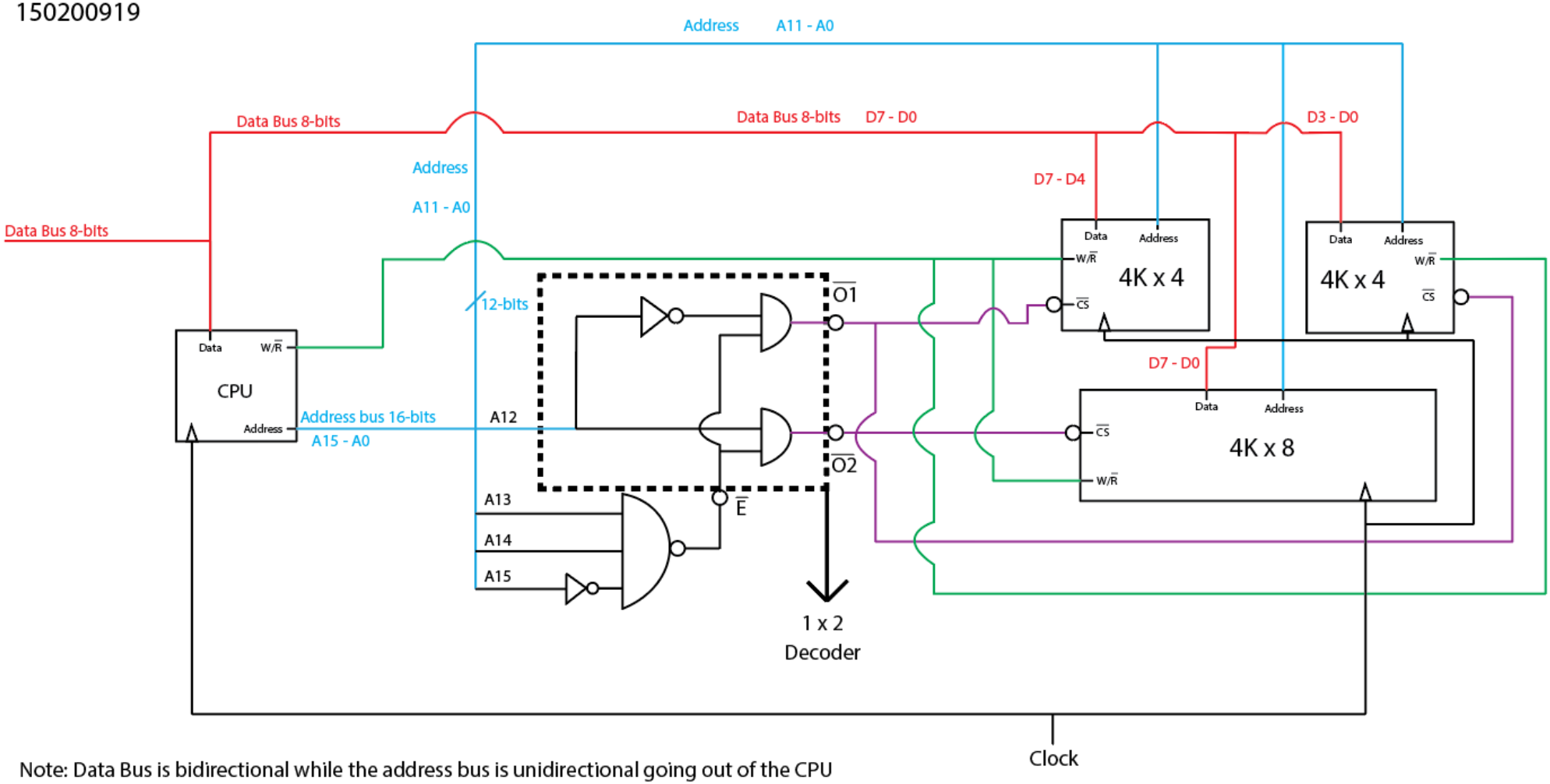


Note: Data Bus is bidirectional while the address bus is unidirectional going out of the CPU
Note: The enable for the decoder is set as active low, and the CS for the memories are also active low
Note: The circle at the decoder outline can be replaced with a NOT gate.
But they are only there because we were requested to make the enable as active low and having a NOT gate makes it look weird.
Also the circles are meant to be the negating part, the labels that I put are just for explanation. so having as negating circle and an inverted label like $\overline{CS}$ doesnt mean -ve and -ve so its +ve. It means to emphasise that due to that circle it is active low