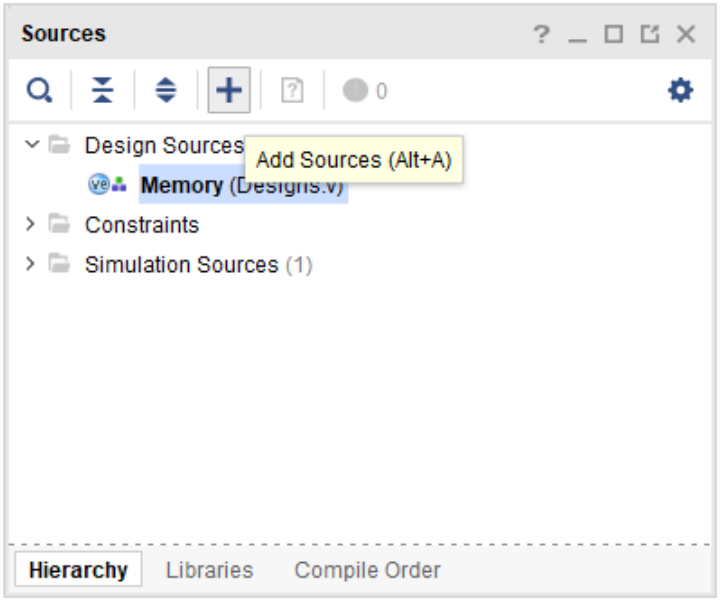
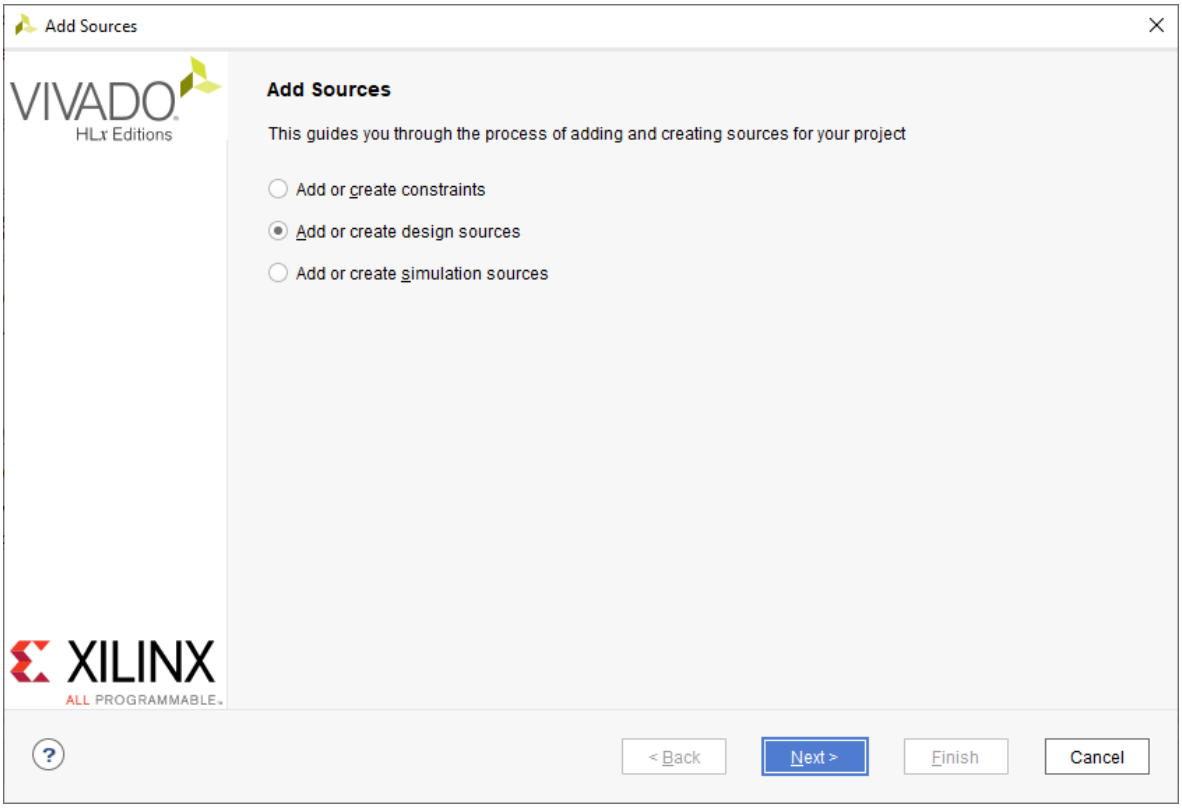
Add Ram Sources to Project

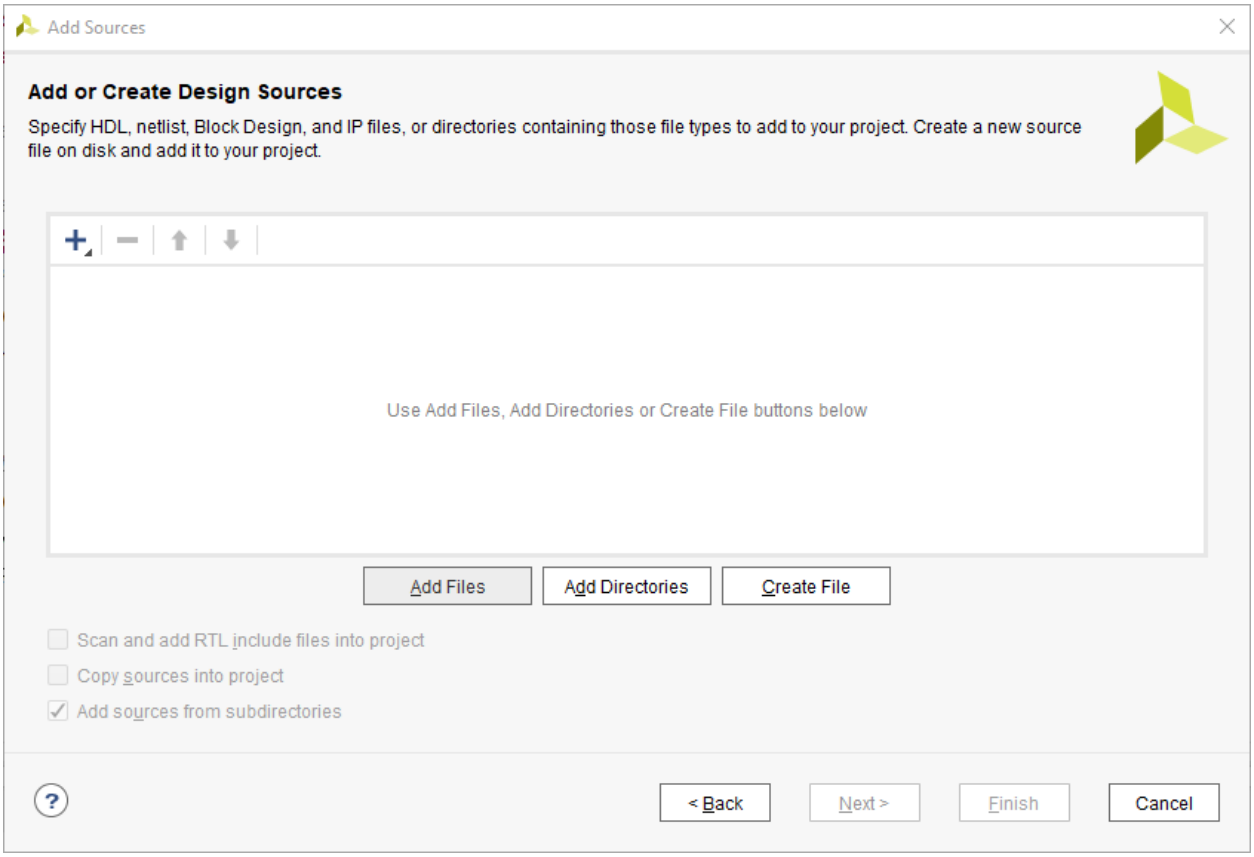
Click the Add Sources under Sources Tab.



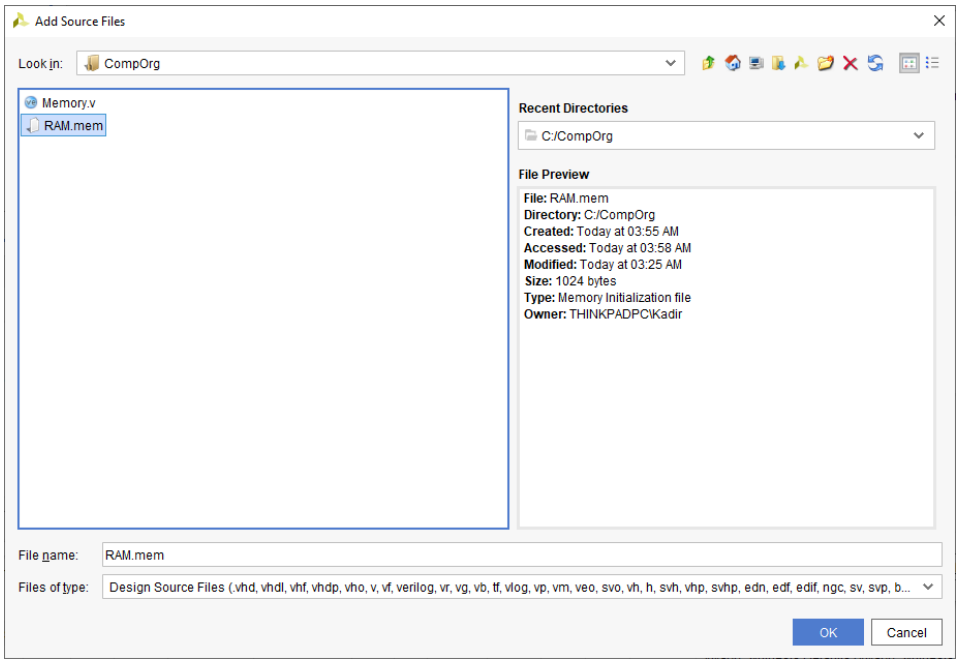
Select “Add or create design sources”, then click the next button.



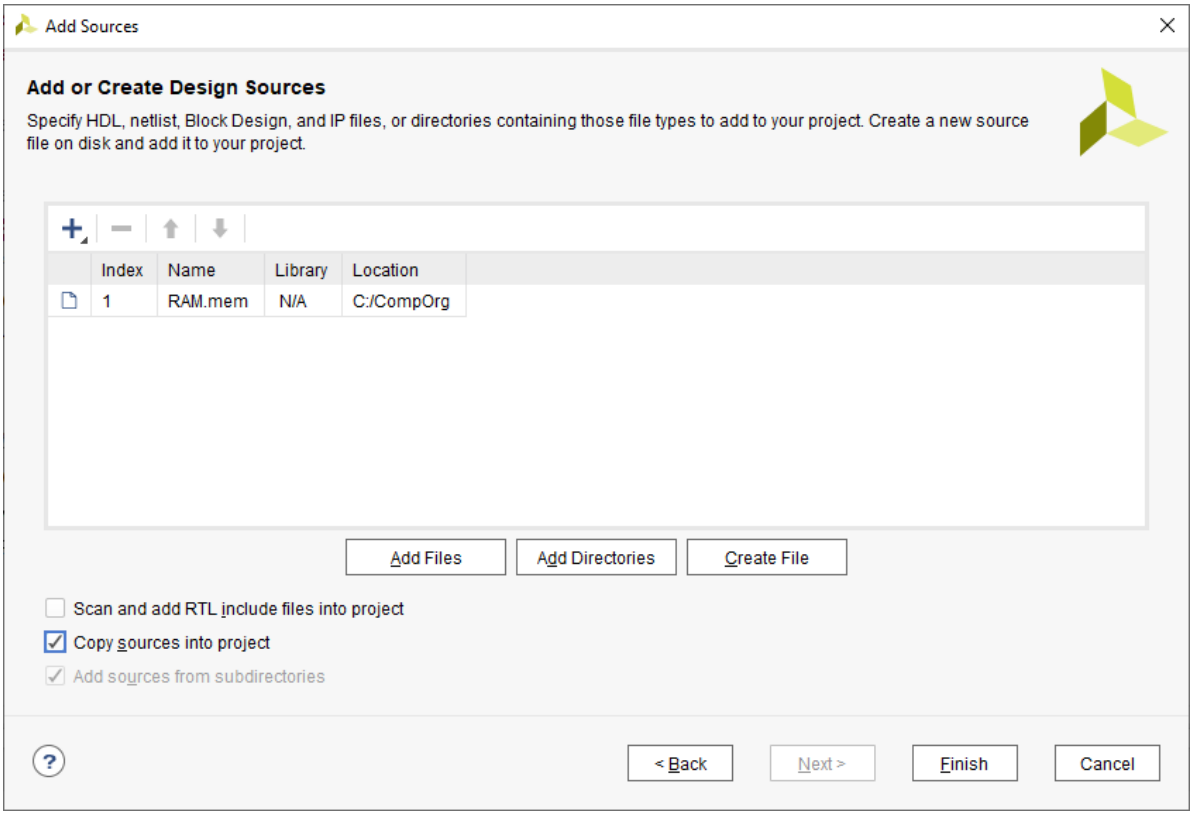
Click “Add Files” button.



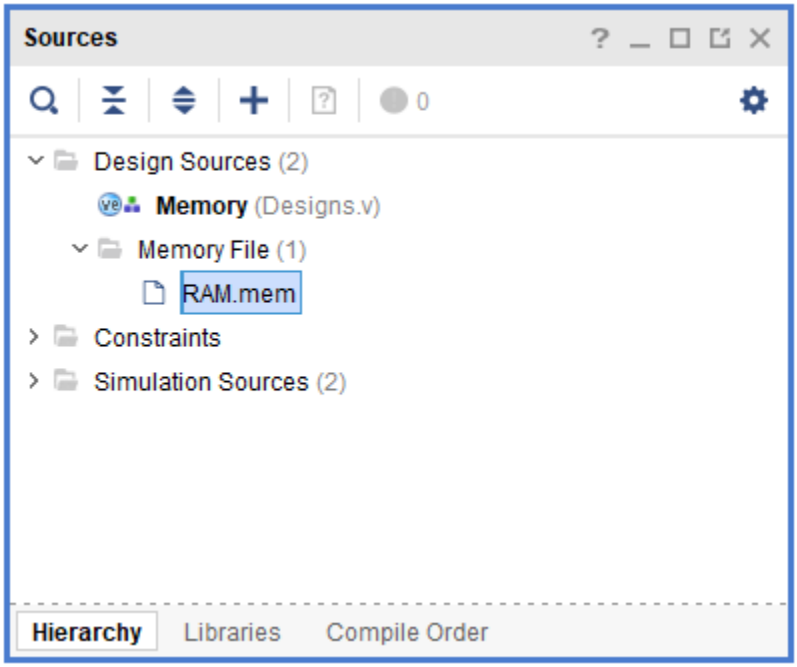
Select the RAM.mem file from File Explorer. Then click OK button.



Select the “Copy sources into project” option and click Finish button to add file.



RAM file can be accessed under sources section.

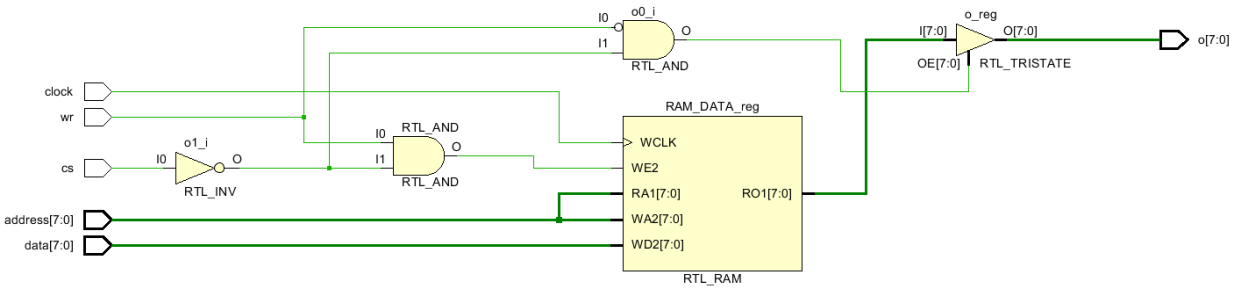


After that, you must include Memory module.

```
module Memory(
    input wire[7:0] address,
    input wire[7:0] data,
    input wire wr, //Read = 0, Write = 1
    input wire cs, //Chip is enable when cs = 0
    input wire clock,
    output reg[7:0] o // Output
);
    //Declaration oıf the RAM Area
    reg[7:0] RAM_DATA[0:255];
    //Read Ram data from the file
    initial $readmemh("RAM.mem", RAM_DATA);
    //Read the selected data from RAM
    always @(*) begin
        o = ~wr && ~cs ? RAM_DATA[address] : 8'hZ;
    end

    //Write the data to RAM
    always @(posedge clock) begin
        if (wr && ~cs) begin
            RAM_DATA[address] <= data;
        end
    end
endmodule
```

You can access your RAM using this module.

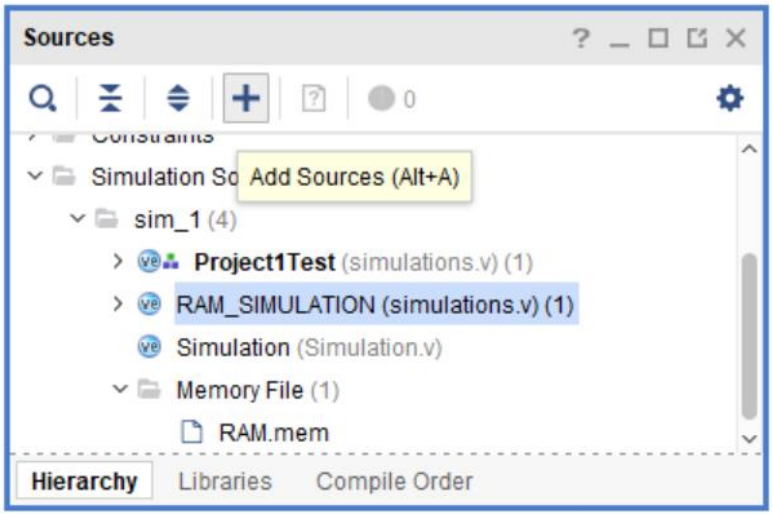


Content of the RAM.mem file: Each line shows the initial content of the memory cell. For Project 1, all values will be zero. These values represent instructions for Project 2.

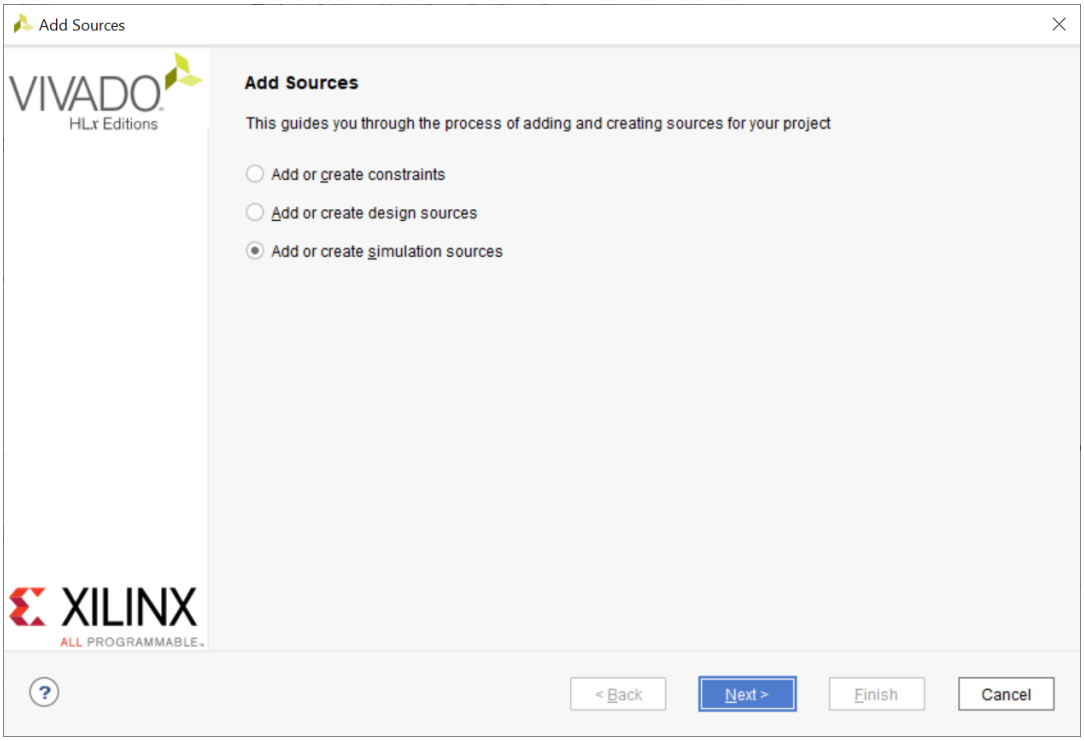
```
1  00
2  00
3  00
4  00
5  00
6  00
7  00
8  00
9  00
10 00
11 00
12 00
13 00
14 00
15 00
16 00
```

Add Test Bench Sources to Project

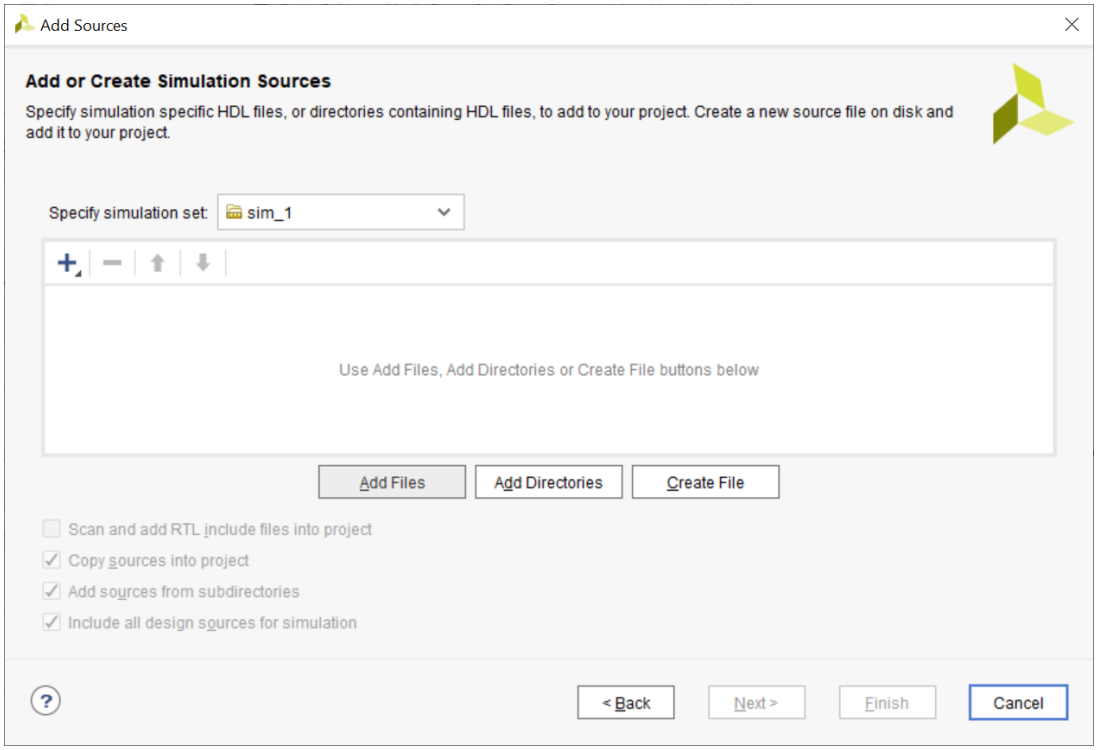
Click the Add Sources under Sources Tab.



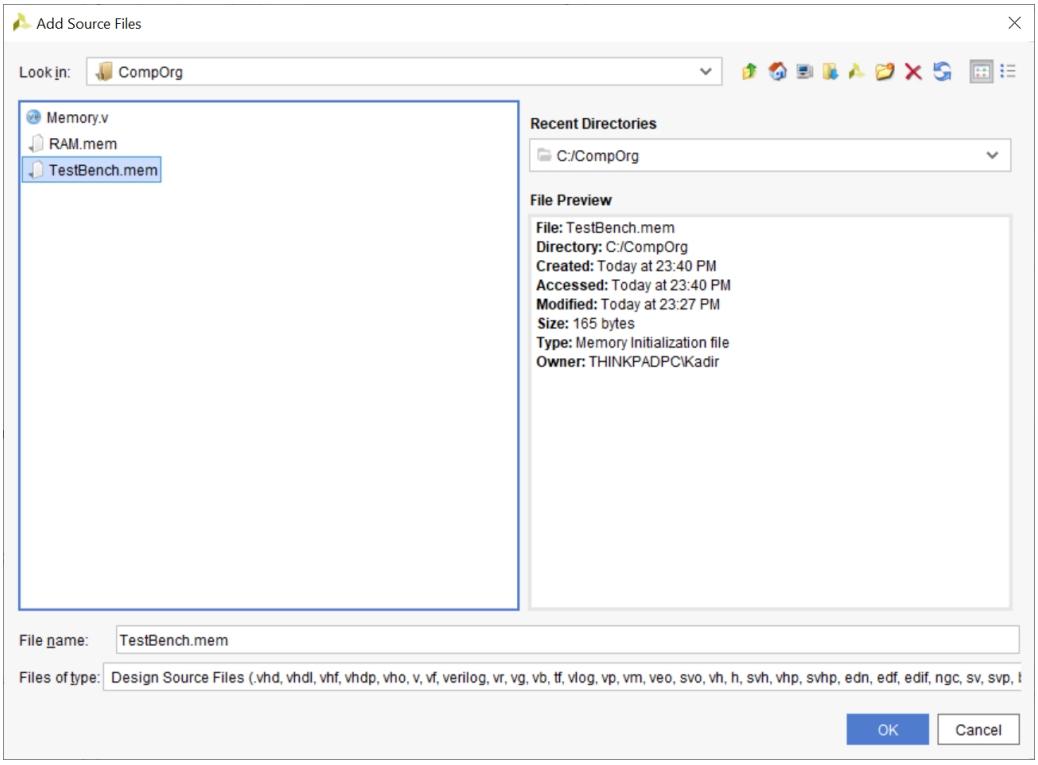
Select “Add or create simulation sources”, then click the next button.



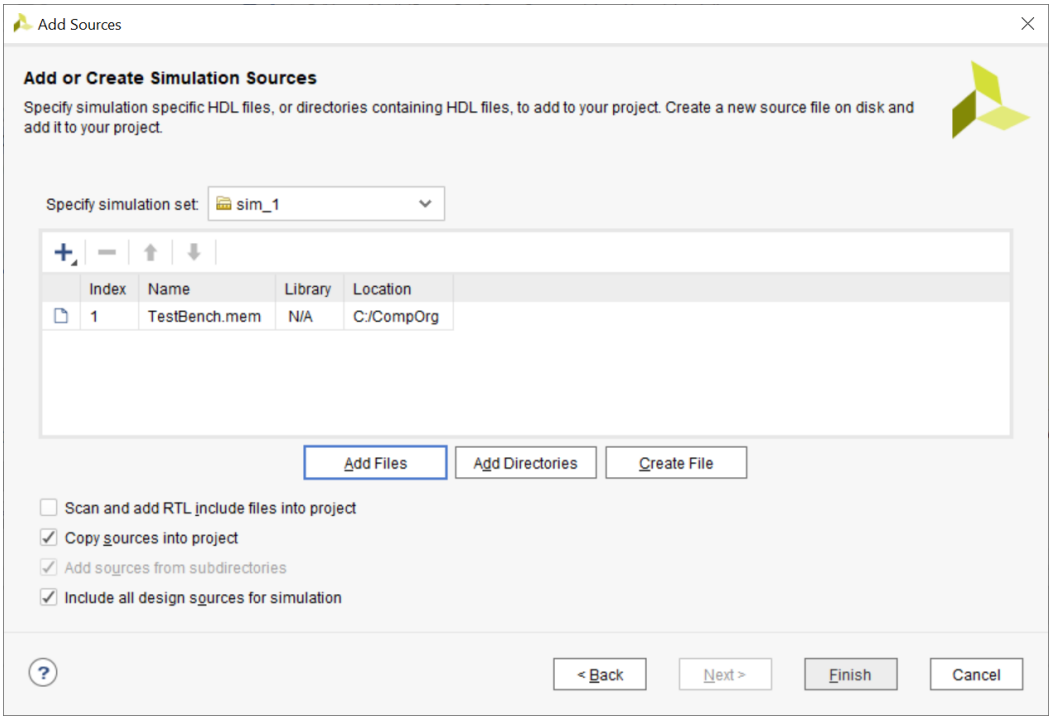
Click “Add Files” button.



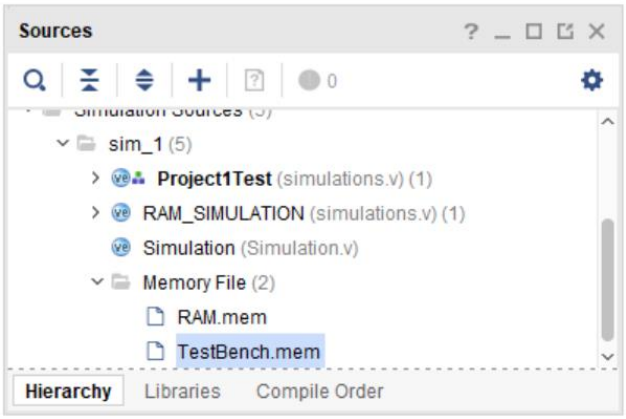
Select the TestBench.mem file from File Explorer. Then click OK button.



Select the “Copy sources into project” option and click Finish button to add file.



TestBench.mem file can be accessed under sources section.



After that, you must include Project1Test module into your project.

```
module Project1Test();
    //Input Registers of ALUSystem
    reg[1:0] RF_OutASel;
    reg[1:0] RF_OutBSel;
    reg[1:0] RF_FunSel;
    reg[3:0] RF_RegSel;
    reg[3:0] ALU_FunSel;
    reg[1:0] ARF_OutCSel;
    reg[1:0] ARF_OutDSel;
    reg[1:0] ARF_FunSel;
    reg[2:0] ARF_RegSel;
    reg      IR_LH;
    reg      IR_Enable;
    reg[1:0]      IR_Funsel;
```

Content of the TestBench.mem file: Each line shows test cases for ALU System.

```
1_10_11_11_0000_0011_11_01_11_000_1_1_11_1_1_10_01_10
0_01_10_01_0010_0101_10_10_00_010_0_0_01_0_0_01_00_00
0_01_10_01_0010_0101_10_10_01_010_0_0_01_0_0_01_00_00

```