4

Latches and Flip-flops

4.1 Introduction

In this experiment, you will implement and examine data storage elements: latches and flip-flops.

4.2 Preliminary

- Refresh your knowledge on how latches and flip-flops work.
- Design and draw the circuit to implement in each experiment part.
- Decide which input data must be loaded to the shift register for each case in 4.4.4.

4.3 Equipments and Integrated Circuits (ICs)

Following equipment and ICs are going to be used in the experiment.

- C.A.D.E.T. (**C**omplete **A**nalogue **D**igital **E**lectronic **T**rainer)
- 74000 series ICs
  - 74xx00 - Quadruple 2-input Positive NAND Gates
  - 74xx02 - Quadruple 2-input Positive NOR Gates
  - 74xx04 - Hex Inverters
  - 74xx75 - Quadruple Bistable D Type Latches
  - 74xx165 - 8-Bit Parallel Input/Serial Output Shift Register
- Oscilloscope

Fundamental information (function tables and pin configurations) of the ICs listed above are given in the Appendix **??**. You should also examine the data-sheets in order to acquire further information about these ICs.

4.4 Experiment

4.4.1 Experiment - Part 1

Implement a SR type latch without an enable input. Use only NOR gates. Use switches for S and R inputs and LEDs for Q and Q_N outputs. Create a truth table for the latch by testing all possible input combinations. Using this truth table, write the characteristic function of the latch as $Q(t+1) = f(S, R, Q(t))$. Note how the latch behaves for disallowed inputs.

4.4.2 Experiment - Part 2

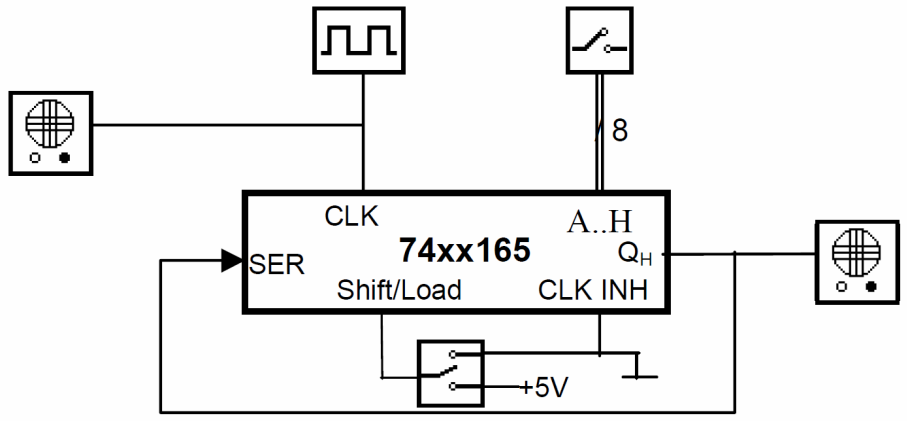
Implement a SR type latch with an enable input, C. Use only NAND gates. Use switches for S, R and C inputs and LEDs for Q and Q_N outputs. Create a truth table for the latch by testing all possible input combinations. Note how the latch behaves for disallowed inputs and how enable input effects the output.

4.4.3 Experiment - Part 3

Implement a negative edge triggered D type flip-flop using two D type latches and one inverter. Use a debounced pushbutton for the clock input, a switch for D and LEDs for Q and Q_N outputs. Show that the clock is only effective at falling edge.

4.4.4 Experiment - Part 4

Implement a pulse generator using a shift register. It should support variable pulse frequencies and durations. Build the circuit below and generate given signals. For each signal, observe both input and output using the oscilloscope and draw.



- with the 1/2 frequency of input
- with the 1/4 frequency of input
- with the 1/8 frequency of input
- with 1/3 pulse–gap duration rate
- with 1/7 pulse–gap duration rate

4.4.5 Experiment - Part 5

Using the $74xx161$ integrated circuit and other necessary gates, implement a counter that counts 0 to 5 in a circular way. Demonstrate the output in the seven segment display.

4.5 Report

Prepare your report by using the guidelines and the report template which are posted on Ninova e-Learning System. Your report should also include the following materials:

- Circuits diagrams of the circuits which were implemented during this experiment.
- Your results as truth tables and discussions for the first 3 parts of the experiment.
- Draw the circuit you implemented in 4.4.5 and explain how it works.
- Your signal drawings and input values for the last part of the experiment.