Istanbul Technical University

Department of Computer Engineering

BLG 242E – Logic Circuits Laboratory

Experiments Booklet

Spring 2023*

Version 2.0

* Version 1.8.0 was prepared by Gökhan Seçinti and Atakan Aral in Spring 2016
Version 1.8.1 was revised by Müge Erel-Özcevik in Spring 2017
Version 1.9 was prepared by Müge Erel-Özcevik and Kadir Özlem in Spring 2019
Version 1.9.1 was revised by Kadir Özlem in Spring 2020
Version 2.0 was revised by Çağatay Koç in Spring 2022

1

Learning CADET & Boolean Algebra

1.1 Introduction

The aim of this experiment is

- to learn about each of the CADET components and how to use them
- to recall the axioms and theorems of Boolean algebra
- to observe these axioms and theorems by applying them in an experimental environment
- to have a basic knowledge of the use of the function generator and the oscilloscope

1.2 Preliminary

- Revise CADET components, the function generator, and the oscilloscope given in the Introduction section of booklet.
- Review your electronic knowledge such as amplitude, frequency, period, peak to peak voltage, root mean square value.
- Revise the axioms and theorems of Boolean algebra.
- Prove the given equalities below by using the axioms of Boolean algebra.
  - $a + a \cdot b = a$
  - $(a + b) \cdot (a + b') = a$
- Determine and prove the duals of the equalities defined above.
- Calculate the complementary expression (F') for the function F which is defined as follows ($F = a \cdot b + a' \cdot c$) by using De Morgan theorem and draw the logic circuit for both expressions (F and F').
- Simplify given logical function and draw the logic circuit.
  - $F(a, b, c, d) = \cup_1(1, 2, 5, 6, 9, 10, 13, 14)$

1.3 Equipments and Integrated Circuits (ICs)

Following equipment and ICs are going to be used in the experiment.

- C.A.D.E.T. (**C**omplete **A**nalogue **D**igital **E**lectronic **T**rainer)
- 74000 series ICs
  - $74xx$[1]04 - Hex Inverter

[1] "xx" has been used as a wildcard in this document. Instead of "xx"; S, LS, C, HC or HCT could be written on the ICs . These letters specify the inner structure of the logic gates. Although their inner structures may differ, their logic functionalities are the same.

  - $74xx08$ - Quadruple 2-input Positive AND Gates
  - $74xx32$ - Quadruple 2-input Positive OR Gates
- Function generator
- Oscilloscope

Fundamental information (function tables and pin configurations) of the ICs listed above are given in the Appendix A. You should also examine the data-sheets in order to acquire further information about these ICs.

1.4 Experiment

1.4.1 Experiment - Part 1

Design and implement the logic circuits for the given expressions below by using the necessary gates.

- $F_1(a, b) = a + a \cdot b$
- $F_2(a, b) = (a + b) \cdot (a + b')$

Design general structure of CADET using power supply (0 V - 5 V). You should use power-strips to distribute V_{cc}(5 V) and Gnd(0 V) through the CADET by using tie points. You should use the switches on the CADET as the inputs for the expressions and you should also use the LEDs to observe the output of the circuit you have implemented.

After the implementation phase:

- Validate correctness of your design.

- Repeat the same implementation by using SPDT switch.

1.4.2 Experiment - Part 2

A theorem is given as: $(a + a \cdot b = a)$. First, determine the dual of the given theorem and then, implement the functions for both sides of the dual theorem by using logic gates. Validate the truth of the theorem by comparing the changes in the outputs.

1.4.3 Experiment - Part 3

$F_3(a, b, c) = a \cdot b + a' \cdot c$ is given. First, determine the complement of the given function (F_3). Then, implement the circuit which realizes the complementary function (F_3') . Validate your implementation by using the truth table.

1.4.4 Experiment - Part 4

A basic logical function (F_4) is defined as follows.

$$F_4(a, b, c, d) = \cup_1(1, 2, 5, 6, 9, 10, 13, 14)$$

First, simplify given logical function and implement the simplified expression using logic gates. Validate your circuit by observing the outputs for each possible input.

1.4.5 Experiment - Part 5

- By using voltmeter, observe V_{cc} and Gnd voltages.
- By using potentiometer, build a resistance in 8 Kohm.
- Show "27" in two seven segment display by giving an input using 8 switches.

1.4.6 Experiment - Part 6

- By giving TTL input from function generator, show the output into logic monitor. Observe the changes on output with different frequencies.
- Use oscilloscope to observe input on different following frequencies.
  - 27 kHz TTL
  - 5 V (Vpp), 1992 Hz CMOS
  - 1 V (Vmax), 500 Hz CMOS
  - 3.14 V (Vpp), 0.6 MHz triangular wave
  - 1.2 V (Vmax), sine wave with 2.5 ms period
  - 0.7 V (Vpp), 0.001 GHz square wave
  - 1250 mV (Vpp), 45 Hz square wave

1.5 Report

Prepare your report by using the guidelines and the report template which are posted on Ninova e-Learning System. Your report should also include the following materials:

- Theoretical information used in the experiment
- Circuits diagrams of the expressions which were implemented during this experiment.
- Function tables (or truth tables) of the implemented expressions.
- For the enrichment of the report, materials such as tables, photos, scheme and diagram.

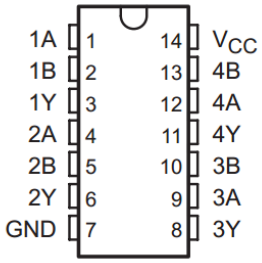
During the experiment, please do not forget to take notes about the critical points of the implementations in order to write a proper report for the experiment. Additionally, if there were any complications which affect your performance during the experiment, please also indicate these difficulties in your report.

A

Appendix - Data Sheets

A.1 7400 - Quadruple 2-input Positive-NAND Gates

Pin Configuration

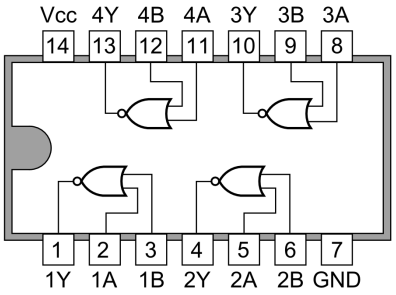


Function Table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

A.2 7402 - Quad 2-input Positive-NOR Gates

Pin Configuration



Function Table

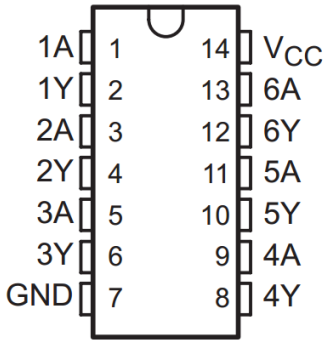
$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

A.3 7404 - Hex Inverters

Pin Configuration

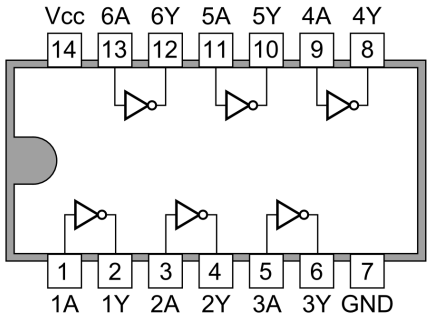


Function Table

INPUT A	OUTPUT Y
H	L
L	H

A.4 7405 - Hex Inverters with Open-Collector Outputs

Pin Configuration



Function Table

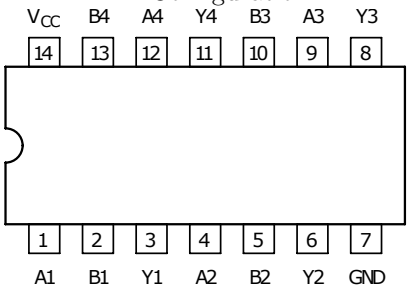
$Y = \overline{A}$

Input A	Output Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

A.5 7408 - Quadruple 2-input Positive-AND Gates

Pin Configuration

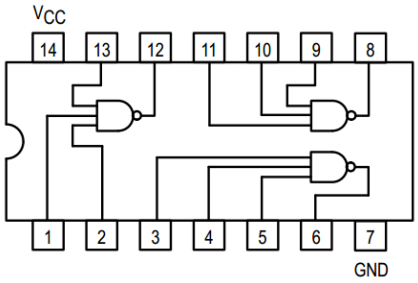


Function Table

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

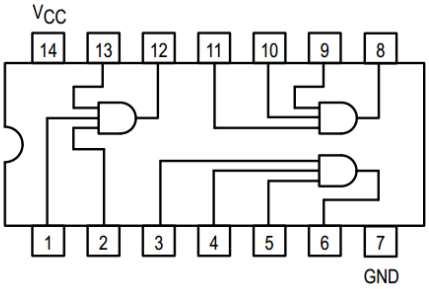
A.6 7410 - Triple 3-input NAND Gates

Pin Configuration



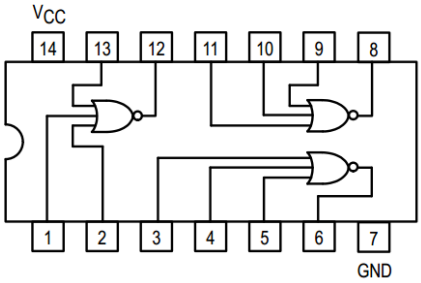
A.7 7411 - Triple 3-input AND Gates

Pin Configuration



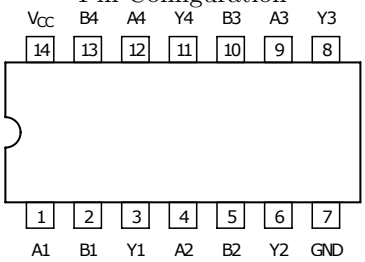
A.8 7427 - Triple 3-input NOR Gates

Pin Configuration



A.9 7432 - Quadruple 2-input Positive-OR Gates

Pin Configuration

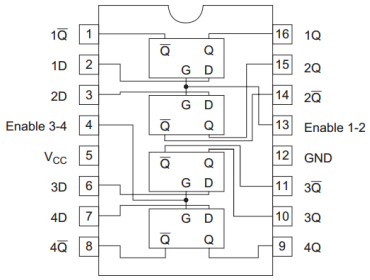


Function Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

A.10 7475 - Quadruple Bistable Latches

Pin Configuration



Function Table

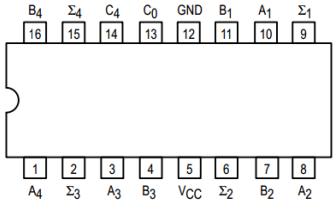
Inputs		Outputs	
D	**G**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H; high level, L; low level, X; irrelevant
Q_0; level of Q before the indicated steady-state input conditions were established.

$\overline{Q}_0$; complement of Q_0 or level of $\overline{Q}_0$ before the indicated steady-state input conditions were established.

A.11 7483 - 4-Bit Binary Full Adder with Fast Carry

Pin Configuration



Function Table

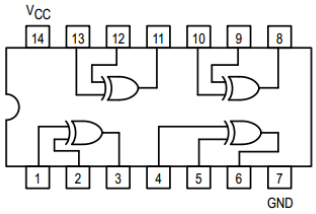
FUNCTIONAL TRUTH TABLE

C (n–1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

A.12 7486 - Quad 2-Input Exclusive Or Gate

Pin Configuration



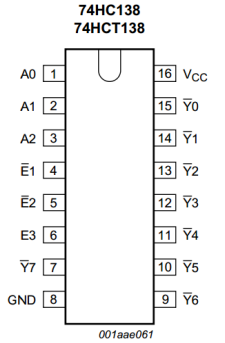
Function Table

TRUTH TABLE

IN		OUT
A	**B**	**Z**
L	L	L
L	H	H
H	L	H
H	H	L

A.13 74138 - 3-to-8 decoder/demultiplexer

Pin Configuration



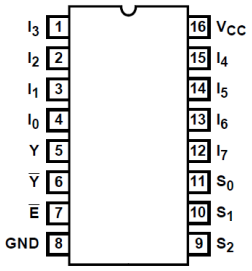
Function Table

Control			Input			Output							
$\overline{E}1$	$\overline{E}2$	E3	A2	A1	A0	$\overline{Y}7$	$\overline{Y}6$	$\overline{Y}5$	$\overline{Y}4$	$\overline{Y}3$	$\overline{Y}2$	$\overline{Y}1$	$\overline{Y}0$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X											
X	X	L											
L	L	H	L	L	L	H	H	H	H	H	H	H	L
			L	L	H	H	H	H	H	H	H	L	H
			L	H	L	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	L	H	H	H
			H	L	L	H	H	H	L	H	H	H	H
			H	L	H	H	H	L	H	H	H	H	H
			H	H	L	H	L	H	H	H	H	H	H
			H	H	H	L	H	H	H	H	H	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

A.14 74151 - 8-Input Multiplexer

Pin Configuration

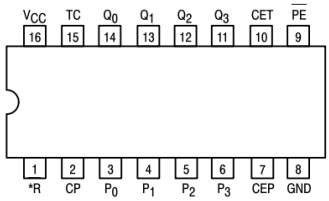


Function Table

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

A.15 74161 - BCD Decade Counter / 4-Bit Binary Counter

Pin Configuration

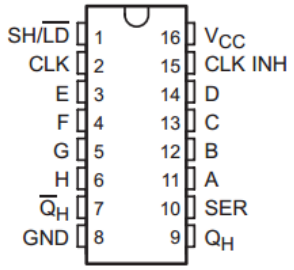


Function Table

*SR	PE	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD (P_n Q_n)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

A.16 74165 - 8-Bit Parallel-Load Shift Register

Pin Configuration



Function Table

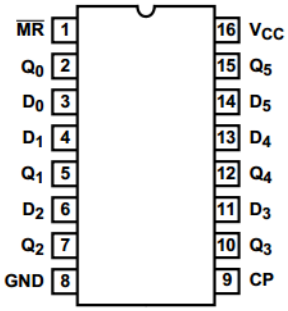
FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

† Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

A.17 74174 - Hex D-Type Flip-Flop with Reset

Pin Configuration



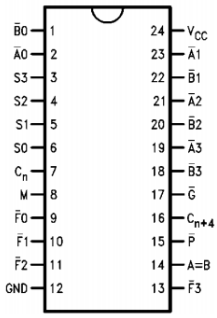
Function Table

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA D_n	Q_n
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant, ↑ = Transition from Low to High Level, Q_0 = Level Before the Indicated Steady-State Input Conditions Were Established

A.18 74181 - 4-Bit Arithmetic Logic Unit

Pin Configuration & Function Table



Pin Names	Description
$\overline{A}0$–$\overline{A}3$	Operand Inputs (Active LOW)
$\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

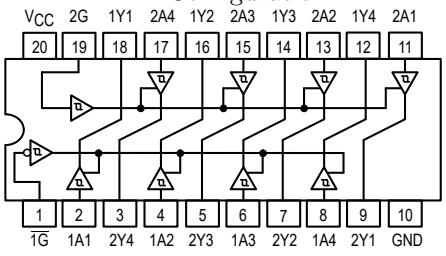
Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 2)	Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A}+B$	A + B
L	L	H	L	$\overline{A}+\overline{B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A}+\overline{B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A}\oplus\overline{B}$	A minus B minus 1	$A\oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A}+B$	A plus AB
H	L	L	H	$A\oplus B$	A plus B	$\overline{A}\oplus\overline{B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A+\overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\overline{B}$ minus A	$A+\overline{B}$	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

Note 1: Each bit is shifted to the next most significant position.

Note 2: Arithmetic operations expressed in 2s complement notation.

A.19 74241 - Octal 3-State Buffer/ Line Driver/ Line Receiver

Pin Configuration



Function Table

Inputs				Outputs	
G	$\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

A.20 4011 - Quad 2-Input NAND Gate

Pin Configuration