ITC Boss level v1.

Addendum, updates and clarifications to 16 bit CPU specifications shared earlier.

As per the original scope and design document.

Version date: 29/11/24

Minimum requirements

Data Transfers

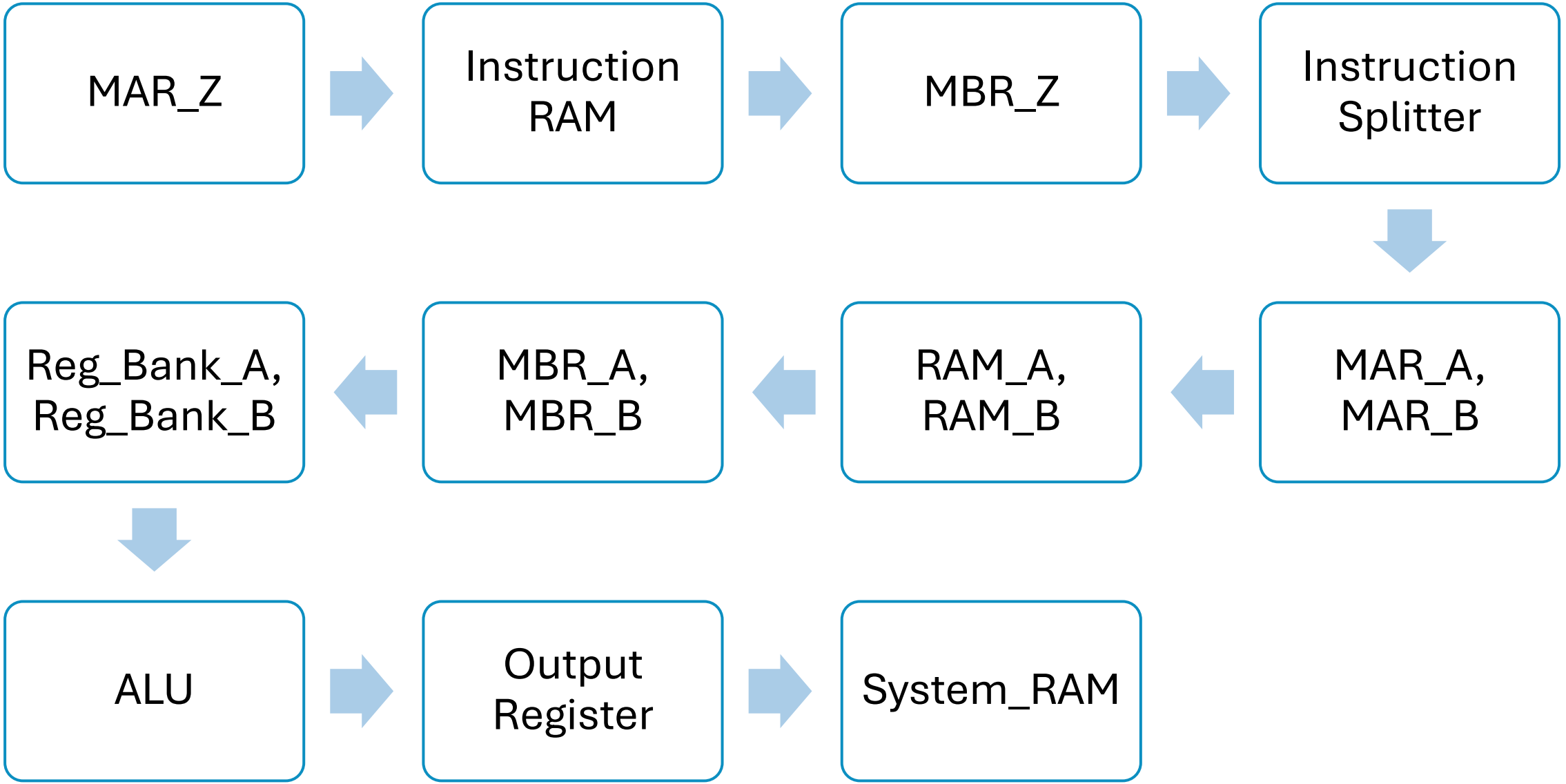
- Addresses to A and B can only be transferred via MAR A and MAR B. Addresses for INST and SYS can only transfer via MARZ.
- Data to ALU can only come through registers. Data to registers can only come through MBR. Data to RAM can only flow through MBRS.
- If you are using a bus terminal, the terminal can only talk to and via MBRS

Hard coding

- Of execution cycles is strictly prohibited in any shape and form.
- Must use program counters for flow of control
- Architectural flow must follow shared data flow and design requirements

Data Flow

Flow summary

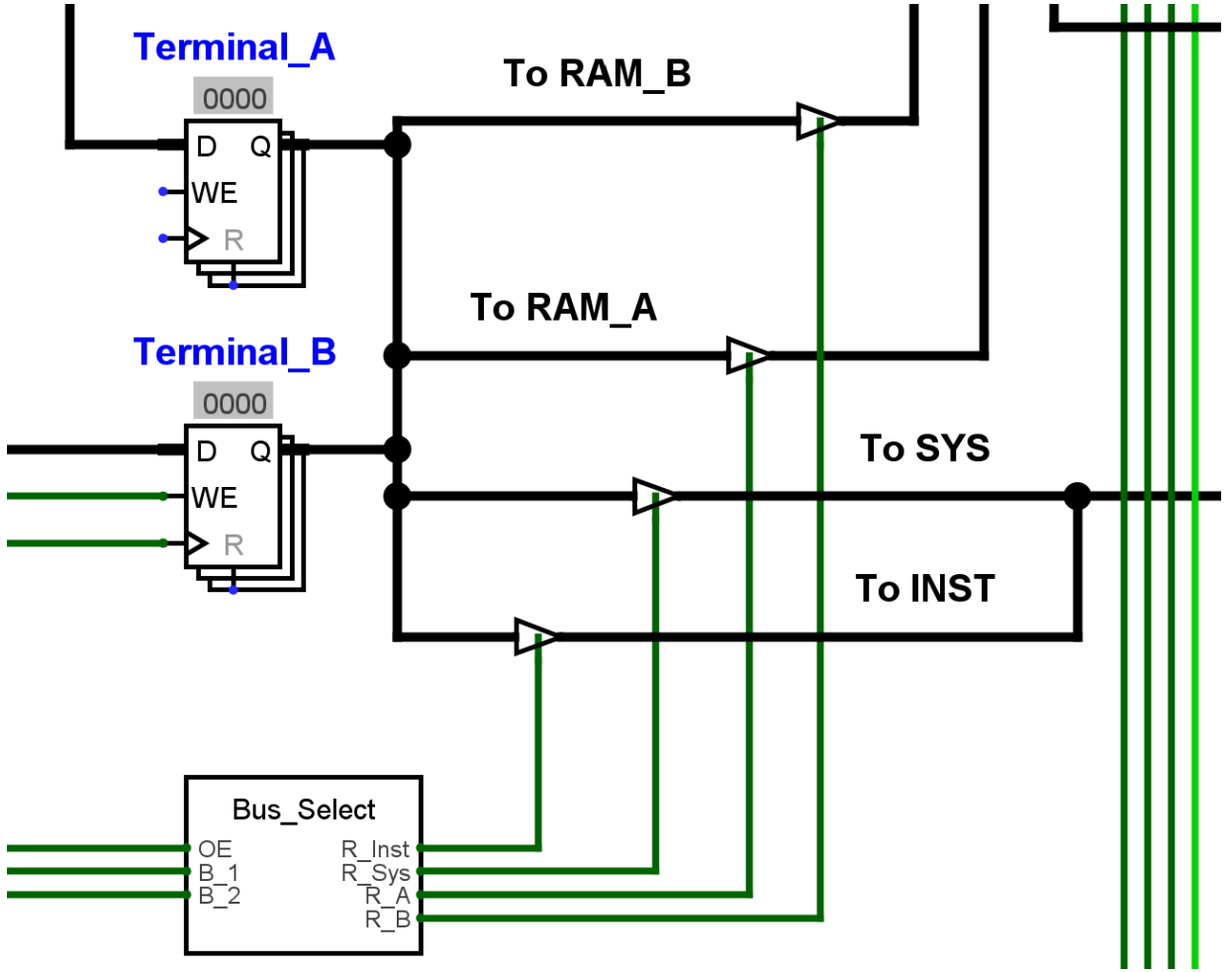


Bus Terminal

One possible visual interpretation of the bus terminal. The bus terminal moves and transfers data across block of RAM using the MOVE instructions. See instructions below

OE = Output Enable
B_1 = Control Line
B_2 = Control Line

R_Inst = Instruction RAM
R_Sys = System RAM
R_A = RAM A
R_B = RAM B



Terminology

Memory Address Register. MAR.

- 5 bits. 3 count

Memory Buffer Register. MBR.

- 16 bits. 3 count

Register Bank. Reg 1 – 8.

- 16 bits. 8 count

Random Access Memory. RAM. Read and Write.

- 16 bits. 4 count

Read Only Memory. ROM. Read only.

- 32 bits. 1 count

Program Counter. PC.

- 2 count

Program Control Unit. PCU.

- 1 count

Architecture

Check List

Core Architecture. Checklist

4 x RAM Blocks.

- 5 bit addresses. 16 bit words

3 x MAR Registers

- 5 bit

3 X MBR Registers

- 16 bit

1 X Bus Terminus

- Bus Interchange

8 x CPU Input Registers

- 16 bit

1 x CPU Output Register

- 16 bit

1 X ALU

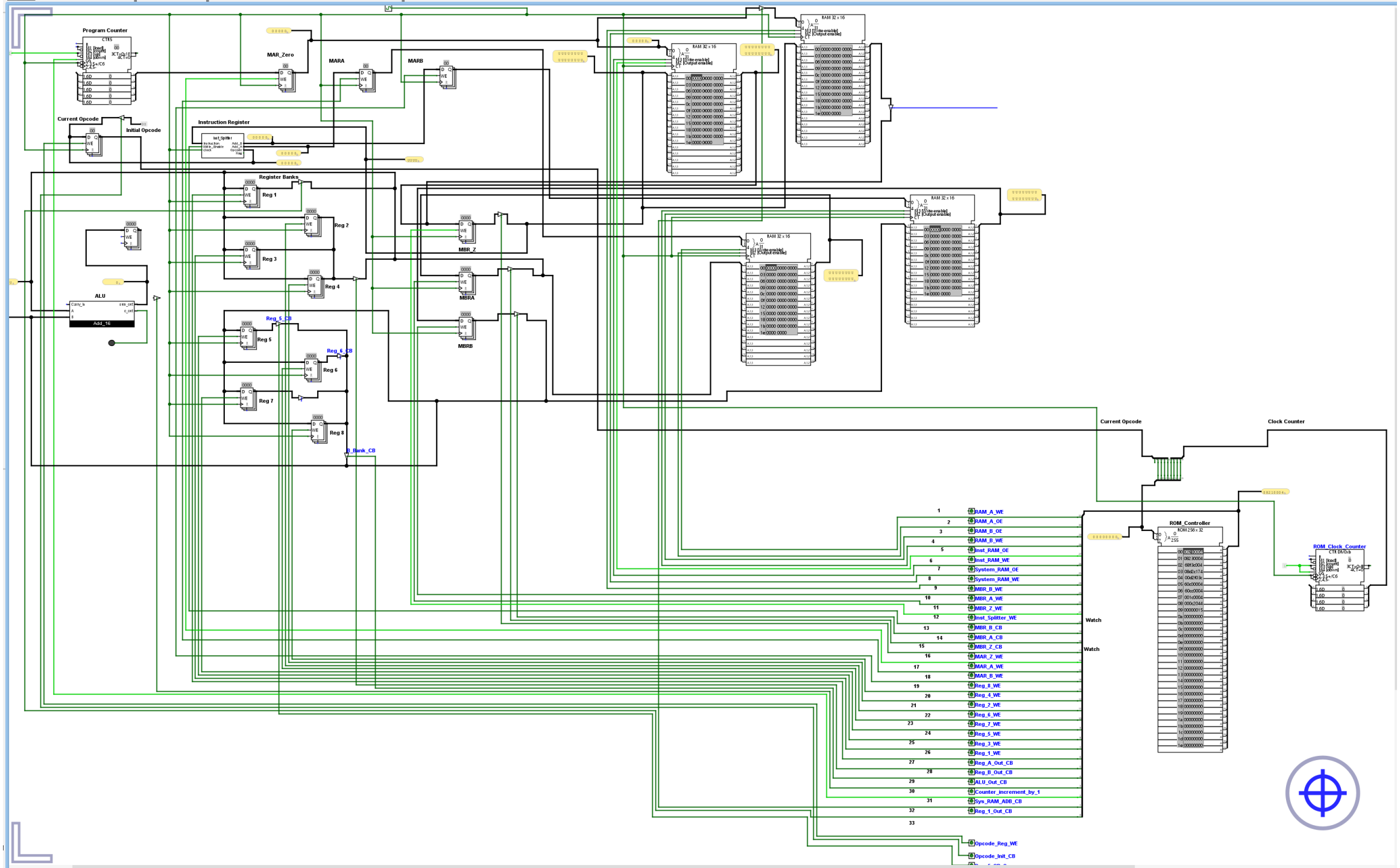
- 12 – 16 Operations

1 x ROM based Program control Unit (PCU)

- Instead of digital circuit based PCU

3 x 16 Bit buses

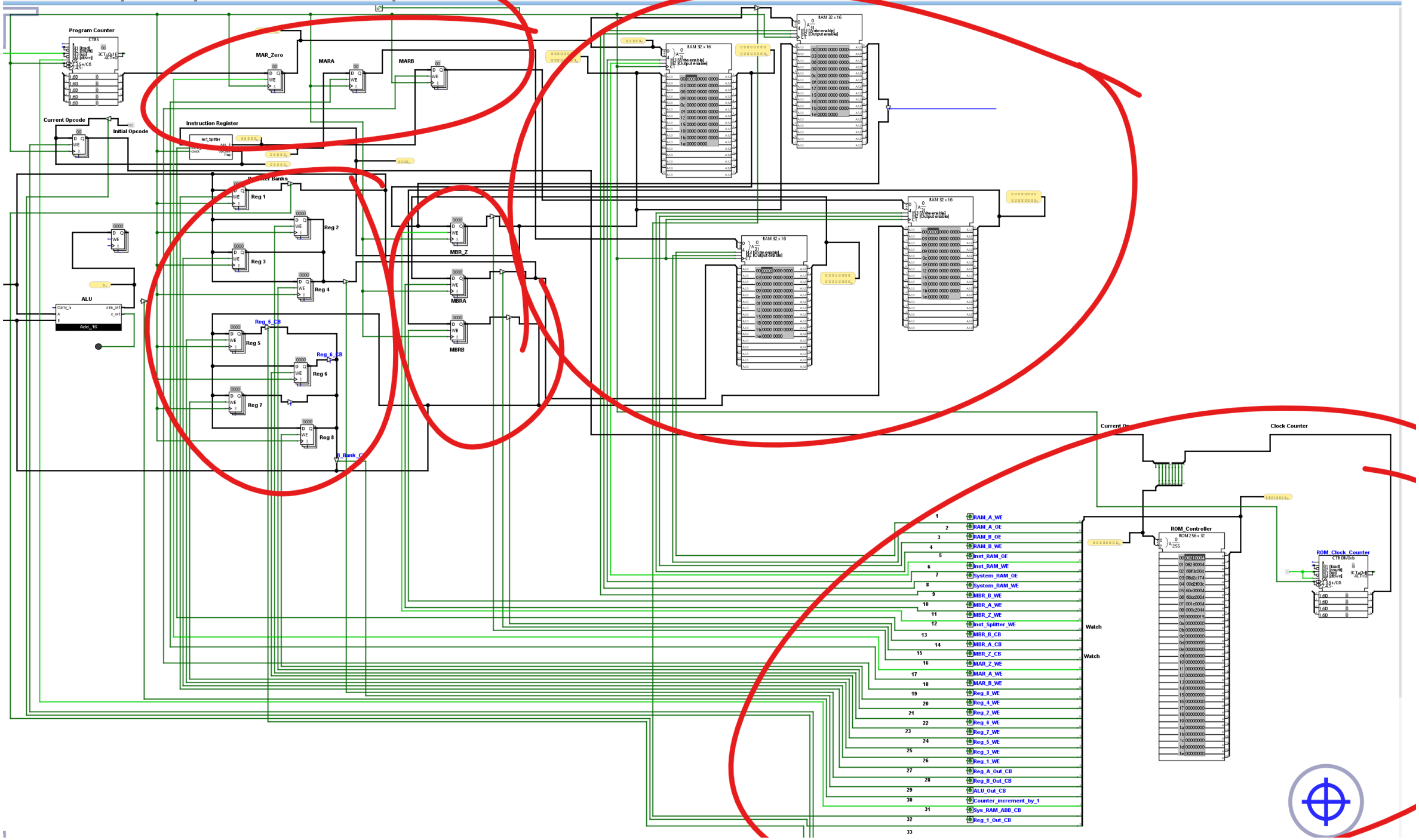
- Separate buses for RAM Blocks


Program Counter
MAR_Zero
MARA
MARB
Current Opcode
Initial Opcode
Instruction Register
Register Banks
Reg 1
Reg 2
Reg 3
Reg 4
Reg 5
Reg 6
Reg 7
Reg 8
Reg_5_CB
Reg_6_CB
B_Bank_CB
MBR_Z
MBRA
MBRB
ALU
Add_16
RAM 32 x 16
Current Opcode
Clock Counter
ROM_Controller
ROM 256 x 32
ROM_Clock_Counter
Watch
Watch
1 RAM_A_WE
2 RAM_A_OE
3 RAM_B_OE
4 RAM_B_WE
5 Inst_RAM_OE
6 Inst_RAM_WE
7 System_RAM_OE
8 System_RAM_WE
9 MBR_B_WE
10 MBR_A_WE
11 MBR_Z_WE
12 Inst_Splitter_WE
13 MBR_B_CB
14 MBR_A_CB
15 MBR_Z_CB
16 MAR_Z_WE
17 MAR_A_WE
18 MAR_B_WE
19 Reg_8_WE
20 Reg_4_WE
21 Reg_2_WE
22 Reg_6_WE
23 Reg_7_WE
24 Reg_5_WE
25 Reg_3_WE
26 Reg_1_WE
27 Reg_A_Out_CB
28 Reg_B_Out_CB
29 ALU_Out_CB
30 Counter_increment_by_1
31 Sys_RAM_ADR_CB
32 Reg_1_Out_CB
33
Opcode_Reg_WE
Opcode_Init_CB

Minimum requirements for viva

ROM based PCU	4 RAM Blocks	8 Register across 2 Banks	3 MAR / 3 MBR
12 – 16 Operations	3 Buses	1 Bus Terminus	Automated Execution of 12 operations

4 x Assembly Test Script execution


Program Counter
MAR_Zero
MARA
MARB
Current Opcode
Initial Opcode
Instruction Register
Inst_Splitter
Register Banks
Reg 1
Reg 2
Reg 3
Reg 4
Reg 5
Reg 6
Reg 7
Reg 8
Reg_5_CB
Reg_6_CB
MBR_Z
MBRA
MBRB
ALU
Add_16
RAM 32 x 16
Current Opcode
Clock Counter
ROM_Controller
ROM 256 x 32
ROM_Clock_Counter
RAM_A_WE
RAM_A_OE
RAM_B_OE
RAM_B_WE
Inst_RAM_OE
Inst_RAM_WE
System_RAM_OE
System_RAM_WE
MBR_B_WE
MBR_A_WE
MBR_Z_WE
Inst_Splitter_WE
MBR_B_CB
MBR_A_CB
MBR_Z_CB
MAR_Z_WE
MAR_A_WE
MAR_B_WE
Reg_8_WE
Reg_4_WE
Reg_2_WE
Reg_6_WE
Reg_7_WE
Reg_5_WE
Reg_3_WE
Reg_1_WE
Reg_A_Out_CB
Reg_B_Out_CB
ALU_Out_CB
Counter_increment_by_1
Sys_RAM_ADB_CB
Reg_1_Out_CB
Watch
Watch

Final viva checklist

- Your circuit must work using the ROM based PCU. No other PCU's are allowed.
- Your circuit must implement at least 12 of the specified instruction. MAT MULT / Block Load / Block Store are mandatory instructions.
- Your circuit must execute 3 of the 4 shared test scripts as they are written without any changes or modification to the script or your circuit.
- Your circuit must meet the minimum architecture requirements specified earlier in this note.
- Mat Mult is not mandatory for the TA viva but is mandatory for the final viva

OpCodes

OPCodes

0000	• Reserved
0001	• Add
0001. With Flag = 1	• Subtract
0010	• Debug
0011	• Mult
0100	• Store
0100. With Flag = 1	• Store Over Flow
0101. Mem Swap	• From A to B
0110. Reg Swap	• Swap source with destination

OPCodes

0111	• Block Load
1000	• Block Store
1001	• Mat Mult
1010	• Compare
1011	• And
1100	• XOR
1101	• NOT (A)
1110	• NOP
1110. With Flag = 1	• HALT

OPCodes

1111	• MOVE A,B (A=Ram A | B=System Ram)
1111. With Flag=1	• MOVE A,B (A=Ram B | B=System Ram)

Instructions

19 Instructions in total

Instructions. A

Reserved. No operation has been assigned to this code

Add, A, B. Add B to A

Sub, A, B. Sub B from A

Mult, A, B. Multiply A and B

Store, C. Store the value in the output register in location C in System RAM

Store OverFlow, C. Store the overflow value in location C in System RAM

Mem Swap, A, B. Swap the value at location A in RAM_A, with value in location B in RAM_B

Instructions. B

Compare A, B. Compare A and B. Store 1 if A is less than B. Store 2 if A = B. Store 4 if A is greater than B. Store results in a specific location in System memory.

AND A, B. Logical Operation AND on A, B

XOR A, B. Logical Operation XOR on A, B

NOT A. Logical Not of Value A

NOP. No Operation.

HALT. Stop Execution

Instructions. C

Reg Swap, A, B. Swap value in register A, with value in register B

Block Load, A, B. Block load 4 values from Address A in RAM_A in Registers 1, 2, 3, 4. Block load 4 values from Address B in RAM_B in Registers 5, 6, 7, 8.

Block Store C. Block store 4 values from output registers in System RAM starting from memory location C.

Mat Mult. Multiply a 2 x 2 Matrix. 4 values x 4 values.

MOVE A,B. Move value in System Ram, at Address B to value in **Ram A address A**.

MOVE A,B (with flag). Move value in System Ram, Address B to value in **Ram B address A**.

Debug A. Delay every data cycle by the clock cycle specified in A. So Debug 3, will add a delay of 3 clock cycles to each data transfer between RAM and MBR, MBR and Registers, Registers and ALU, ALU and Output, Output and MBR, MBR and RAM

Boss Level
Viva Extensions

To be released on 1st December 2024