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Exam Type:	Quiz 4b	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1 [6]

What is the difference between following memories: Mask-programmed, EPROM and DRAM in terms of write ability and storage permanence?

Question 2 [14]

1. **L1: ld R1, 50 (R4)**
2. **Div R2, R1, 8**
3. **ld R3, 100 (R4)**
4. **sub R5, R3, R2**
5. **st R5, 50 (R4)**
6. **sub R4, R4, 4**
7. **bne R4, R6, L1**

Consider the following specification for our pipelined processor:
Five stages MIPS pipeline where division consumes 4 cycles in execution. All other instructions consumes 1 cycle in each stage. Branch calculation is done in decode stage.
Forwarding has been implemented.

a) Add stalls in the above code to avoid data and control hazards	**b) Rearrange the code to remove stalls**

c) Perform 2-level un-roll and reschedule the code to remove as many stalls as possible

Unrolled code	**Rescheduled unrolled code**