	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2018
			Total Marks:	65
	Due Date:	25-09-2018	Weight	~3.3
	Exam Type:	Assignment 1	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1 [15]

Given the following values in hexadecimal notation

1. 0x AE2A0028
2. 0x 01288020
3. 0x 1573FFFC

What does these represent, assuming that they are

a. A two's complement integer
b. An unsigned integer
c. A MIPS instruction
d. A single precision floating-point number in IEEE 754 format

Question 2 [10]

Convert the following values to 32-bit IEEE 754 floating point representations.

i. 30.125
ii. -35.0
iii. +inf
iv. –inf
v. NAN

Question 3 [10]

Using Optimized divider circuit, perform the division operation. Value of each register is initialized in the table below. List different steps that will be performed in each iteration and the resulting value of each register. Dividend register will contain Remainder and Quotient at the end of all iterations.

Iteration	Step	Dividend (Remainder + Quotient)	Divisor
0	Initial values	10111010	0111
1			
2			
3			
4			
5			

Question 4 [10]

Design a 4-bit ALU that supports the following operations:

1) A + B
2) A – B (2's complement subtraction)
3) 1-bit right shift (apply to input A)
4) 2-bit right shift (apply to input B)
5) 1-bit rotate left (apply to input A)
6) 1-bit rotate right (apply to input B)
7) A & B (bitwise AND)
8) A xor B (bitwise XOR)

Question 5[15]

Draw a sequential circuit that has two D flip-flops, A and B, maintaining state, two inputs X and Y and one output Z. The output and next flip-flop states are given by the equations.

$$A_{i+1} = A_i(\bar{X}B_i + Y)$$
$$B_{i+1} = \bar{X}Y + XA_i$$
$$Z = X\bar{B_i} + X\bar{A_i}$$

a) Draw the logic diagram of the circuit.
b) Tabulate the state table
c) Draw state diagram

Question 6[5]

Construct a 16-to-1 multiplexer with 8-to-1 and 2-to-1 multiplexers. Use block diagrams for each multiplexer instead to designing the internal functionality.