	Course Name:	Computer Architecture	Course Code:	EE204
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			Total Marks:	60
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	Evaluation Type:	Assignment 3	Page(s):	4

Student : Name:_____ **Roll No.**_____ **Section:**_____

Question1: **(20 marks)**

Suppose we want to execute the following program on a 2-way superscalar processor with following execution units with mentioned latencies.

Adder **2 cycles**
Divider **3 cycles**

```
Loop: LD R3, 40(R5)
      DIV  R2, R2, R5
      ADD R2, R2, R3
      ST R2, 20(R5)
      SUB R5, R5, 2
      BEQ R5, R0, Loop
```

You have to show the execution of two iterations of this loop on a 2-way superscalar processor. You can move an instruction from one stage to the other as soon as a slot is available in the next stage. Instruction wait in the decode stage in case there is any dependency. Buffers are available after execution and memory stages to hold completed operations. Forwarding is implemented.

a. **You have to show all steps for In-order issue and out-of-order execution and completion.**

Cycle No.	IF	ID	EX	MEM	WB
1					
2					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					

b. Now unroll the loop for level-2 (2 iterations only) and reschedule the instructions to get best execution time.

Instructions after 2 level loop-unrolling (without false dependencies)	Optimized schedule of Instructions

c. Execution on 2-way superscalar:

Now take instructions after 2 level loop-unrolling (without optimization) and show the execution of this sequence of instructions on 2-way superscalar processor for In-order issue and out-of-order execution and completion.

Cycle No.	IF	ID	EX	MEM	WB
1					
2					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					

Question 2: **(15 marks)**

You need to design a memory system that has 36 bit address bus and 32 bit data bus. The memory system will have 2 cache levels.

- L1 cache is a direct-mapped cache containing 128 KB data and has a line/block size of 128 bits (16 bytes).
- L2 cache is a 4-way set associative cache containing 4 MB data and has a line/block size of 128 bits (16 bytes).

Design the memory system clearly showing the inter connection between the 2 caches. You should label the tag, index and offset bits clearly with their relevant sizes. Also calculate the size of tag array for each cache.

Question 3: **(10 marks)**

Each instruction fetch means a reference to the instruction cache and 25% of all instructions reference data memory (Load/Store instructions).

With the first implementation (separate instruction and data cache):
- The average miss rate in the L1 instruction cache was 3%
- The average miss rate in the L1 data cache was 8%
- In both cases, the miss penalty (time to access main memory) is 200 CCs

For the new design, with unified memory (same cache for instruction and data), the average miss rate is 5% for the cache as a whole, and the miss penalty is again 200 CCs.

a) Which design is better and by how much?
b) If we add L2 cache in the new design with access time equal to 20cc, it reduces the miss rate to 2.5 % from 5 %. What will be the new average memory access time?

Question 4: **(15 marks)**

Consider a program having the following instruction mix:

Instruction Type	%age in Program
LD	30%
ST	20%
Integer Arithmetic	30%
Branch	10%
Floating Point Arithmetic	10%

The processors clock speed is 4GHz and program execution runs 1million instructions (10^6 instructions). First consider a processor which has a perfect cache (1 cycle hit time, 0% miss rate). In that case, latency of each instruction is given below:

Instruction Type	Clock Cycles
LD	5
ST	5
Integer Arithmetic	4
Branch	4
Floating Point Arithmetic	20

a) Calculate the total number of clock cycles required for program execution with perfect cache?

Caches are never perfect. Consider that we have a shared (instruction and data) L1 cache that has a miss rate of 8% per memory access (instruction fetch is a memory access). RAM access in case of a miss takes 250ns. The hit time of L1 cache is 2 cycles. This means, a load instruction hitting cache for both instruction and data will take 5+1+1 = 7 clock cycles(1cycle for cache is already included for perfect cache so now additional 1 cycle is required at Fetch and Memory stages).

b) Calculate memory access cycles introduced when fetching instructions in program execution?

c) Calculate memory access cycles introduced when accessing data in program execution?

d) What is the total number of memory access cycles for the program execution?

For L2 cache the processor designer has 2 options:

I) Large off-chip L2 cache which reduces miss rate to 3% and has a hit time of 15ns.

II) Small on-chip L2 cache which reduces miss rate to 5% and has a hit time of 3ns.

f) Calculate memory access cycles for both (I) and (II) caches.

g) Calculate total program execution time for both cases and state which one is faster.