

	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2019
	Duration:	30 Minutes	Total Marks:	20
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	Exam Type:	Quiz 5c	Page(s):	2

**Student : Name:** \_\_\_\_\_ **Roll No.** \_\_\_\_\_

**Section:** \_\_\_\_\_

**Question 1 [2+2+4]**

Assume for specific system the:

Clock rate is 2 GHz, Base CPI is 4

L1 access time is 1 cycle, L2 access time is 10 cycles, Memory access time is 100 cycles,

L1 hit rate is 60%, L2 hit rate is 70%.

Memory Accesses Per Instruction = 80%

1. What is the average memory access time?
2. What is the global miss rate?
3. What is the effective execution time for a program with 1000 instructions?

**Question 2 [3+3+2+2+2]**

Consider a memory sub-system—with 16-bit addresses—that has two levels of cache (L1 and L2). L1 is a direct-mapped cache with 4 bytes block size and cache capacity of 4 KB. L2 is an 8-way set associative cache with 8 bytes block size and cache capacity of 32 KB.

<b>a. Calculate the size of tag, index, and offset fields for the L1 cache</b>	<b>Number of tag bits</b>	
	<b>Number of index bits</b>	
	<b>Number of offset bits</b>	
<b>b. Calculate the size of tag, index, and offset fields for the L2 cache</b>	<b>Number of tag bits</b>	
	<b>Number of index bits</b>	
	<b>Number of offset bits</b>	
<b>c. Suppose the byte with address 0001 1010 0001 1011 is stored in L1 cache. What are the addresses of the other bytes stored along with it in the same block?</b>		
<b>d. Calculate the size of tag array for L1 cache!</b>		
<b>e. Calculate the total bits of storage required for L2 cache!</b>		