	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2019
	Duration:	30 Minutes	Total Marks:	20
	Paper Date:	05-12-2019	Weight	~3
	Exam Type:	Quiz 5e	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1a [4]

What is the difference between TLB cache and Data cache?

Question 1b [4]

What is write-through policy? What are the pros and cons of this strategy?

Question 2 [12]

Assume the miss rate of an instruction cache is 10% and the miss rate of the data cache is 20%. If a processor has a CPI of 4 without any memory stalls and the miss penalty is 100 cycles for all misses. Proportion of all loads and stores instructions is 50% of the program.

a. **Calculate the instruction cache stall cycles.**

b. **Calculate the data cache stall cycles.**

c. **Calculate the effective CPI.**

d. **Calculate the execution time for a program of 1000 instruction on a processor with frequency of 2Ghz.**