National University of Computer and Emerging Sciences, Lahore Campus

Course:	Advance Computer Architecture	Course Code:	EE502
Program:	MS(Computer Science)	Semester:	Spring 2017
Duration:	30 Minutes	Total Marks:	30
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Section:	A	Page(s):	2
Exam:	Quiz 1		

Q1: Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table [10 marks]

Processor	Clock Rate	CPI
P1	5 GHz	4.0
P2	1 GHz	2.0
P3	10 GHz	5.0

(a) Which processor has the highest performance? Show complete working.

(b) If processor P2 executes a program in 10 seconds, find the number of cycles and number of instructions.

Q2:
```
load   R5, 100(R3)
and    R3,  R5, R1
add    R2, R5, R3
store  R2, 100(R3)
sub    R14, R3, R2
```

Find all types of hazards in above code. If there is a hazard between two instructions 1 and 2, write 1 &2 in front of that hazard below: [10 marks]

RAW:

WAR:

WAW:

Q3: The 5 stages of the processor have the following latencies: [10 marks]

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	500ps	100ps

A. For a non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?

B. For a pipelined processor assume, what is the cycle time in this case? What is the latency of an instruction? What is the throughput?