Computer Architecture – Fall 2020

Assignment # 5

Due Date: *December 11, 2020*
Time: *5 pm*

You may be called for evaluation of this assignment and you will have to justify your solutions before the course instructors and the TA. Failure to justify your answers will result in negative marks. Severity of the plagiarism can result in F as well.

You can expect a class presentation for your solution where you will have to solve the questions in front of the class. You can expect to have cross questioning from the instructor, TA or classmates.

Q1. Below is a list of 32-bit memory address references, given as word addresses

27, 196, 201, 163, 61, 168, 62, 193, 121, 143, 144, 77

a. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

b. Show the final contents of the cache in terms of block numbers, tag bits for each block and valid bit

Index #	Valid bit	Tag bit	Block

Reference	Binary address	Tag bits	Index bits	Hit/Miss?

Q2. Repeat question 1 with a direct-mapped cache with two-word blocks and a total size of 8 blocks.

Q3. Consider a cache with 64KB size with 4-word block size.

a. Calculate the total number of bits required for the cache listed in the table, assuming a 32-bit address
b. Generate two series of references (at least 10 different references in each series), where first series has 5 cache miss and second series has 8 cache miss for the following cache configurations

    a. Direct mapped
    b. 2-way set associative
    c. 4-way set associative
    d. Fully associative