	Course Name:	Advance Computer Architecture	Course Code:	EE502
	Program:	MS (Computer Science)	Semester:	Spring 2017
	Duration:	180 Minutes	Total Marks:	70
	Paper Date:	10-05-2017	Weight	45
	Section:	ALL	Page(s):	9
	Exam Type:	Final		

Student : Name:_____ Roll No._____ Section:_____

Instruction/Notes:
1. Attempt all question in the provided space. You can use rough sheets but it should not be attached.
2. If you think some information is missing, write your assumption and solve accordingly.

Question1: **Marks 15**

Explain the purpose of following techniques. How we use them and what benefit we obtain by employing these techniques.

1. **Reorder buffer**
2. **Pipelined caches**
3. **Non blocking caches**
4. **Omega Network**
5. **VLIW**

Question2: **Marks 15**

Consider the following program that will be executed on a **2-issue Superscalar MIPS** architecture with **Static Branch Prediction (BACKWARD TAKEN)**

Consider the following specification for our pipelined processor:

- Five stages MIPS pipeline with **execution stage consuming 2 clock** cycles whereas all other stages consume 1 cycle.
- **Forwarding is implemented**
- Computation of PC and TARGET ADDRESS for branch & jump instructions anticipated in the **ID stage**

```
L1: lw R2, 50 (R4)
    addi R2, R2, 4
    lw R3, 150 (R4)
    addi R3, R3, 8
    add R5, R2, R3
    sw R5, 250 (R4)
    addi R4, R4, 4
    bne R4, R7, L1
```

a. In-order issue and out-of-order execution and completion rules are applied. For each cycle, show which instructions is at which stage by filling the following table. You don't need to write complete instructions. Just write the instruction numbers from the code above. Remember you cannot re-arrange the instructions for this part of the question.

Cycle No.	IF	ID	EX	MEM	WB
1					
2					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					

b. Now unroll the loop for level-2 (2 iterations only) and reschedule (rearrange) the instructions to get best execution time with the specifications described above. Also mention the changes required in instructions.

c. Show the execution of this sequence of instruction for In-order issue and out-of-order execution and completion. Don't write whole instructions instead use the Instruction number assigned in part a.

Cycle No.	IF	ID	EX	MEM	WB
1					
2					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					
.					

Question 3: **Marks 10**

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. **How is a 16-bit memory address divided into tag, index and offset?**

b. **Into what line would bytes with each of the following addresses be stored?**
0001 0001 0001 1011
1101 0000 0001 1101

c. **Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?**

d. **If the cache is 4-way set associative then tell the location of values (given in part b) in this cache**

e. **If the cache is fully associative then what would be the size of index bits and tag bits?**

Question4: **Marks 10**

Consider the following MIPS assembly code to be executed on a pipelined CPU.

```
Loop: beq R6, R7, exit
        lw R2, 0(R6)
        sw R2, 100(R6)
       lw R2, 200(R6)
       addi R2, R2, R6
       sw R2, 300(R6)
       addi R6, R6, 4
       j Loop
exit
```

Your task is to do dynamic scheduling using **Scoreboard**. There are:

- 3 LOAD/STORE Functional Units (LDU1, LDU2,LDU3) with latency of 4 cycles
- 2 ALU/BR/J Function Units (ALU1, ALU2) with latency 2 cycles

Moreover you have to identify:

- Structural hazards in ISSUE phase
- RAW hazards in Read Operand phase
- Check WAR and WAW in Write back phase
- Forwarding is implemented

Assume static branch prediction (backward taken, forward not taken) is used.

Instruction status:

Instruction	Issue	Read Operands	Exec Start	Exec Comp	Write Result
Loop: beq R6, R7, exit					
lw R2, 0(R6)					
sw R2, 100(R6)					
lw R2, 200(R6)					
addi R2, R2, R6					
sw R2, 300(R6)					
addi R6, R6, 4					
j Loop					
exit					

Register result status:

R0	R1	R2	R3	R4	R5	R6	R7

Question 5: **Marks 10**

Processor X has a clock speed of 1 GHz, and takes 1 cycle for integer operations, 2 cycles for memory operations, and 4 cycles for floating point operations. Empirical data shows that programs run on Processor X typically are composed of 35% floating point operations, 30% memory operations, and 35% integer operations. You are designing Processor Y, an improvement on Processor X which will run the same programs and you have 2 options to improve the performance:

1. Increase the clock speed to 1.2 GHz, but memory operations take 3 cycles
2. Decrease the clock speed to 900 MHz, but floating point operations only take 3 cycles

Compute the speedup for both options and decide the option Processor Y should take.

Question 6: **Marks 10**

Suppose we have following two configurations
a. 32-bit operating system, 4-KB pages, 1 GB of RAM
b. 64-bit operating system, 16-KB pages, 16 GB of RAM

1. How many bits are required for each of the following entries: P stands for Physical and V stands for Virtual

Config.	V. Addr bits	P. Addr bits	V. Page no. bits (index in V. addr)	P. Page no. bits (index in P. addr)	Offset
a					
b					

2. What are some advantages and disadvantages of using a larger page size?

3. What is TLB cache and what purpose it serves?