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Student : Name:_____ Roll No._____ Section:_____

Question 1 [10]

Suppose we have 4 way set-associative L1 cache that has the following division of 32-bit address:

bits 0 - 5 = offset, bits 6 - 17 = index, bits 18 - 31 = tag

a. **What is the size of each cache block?**

b. **How many sets are present in the cache?**

c. **What is the size of the cache (data bits)?**

d. **How much space is required to store the tags for the L1 cache (size of tag array)?**

e. **If cache is direct-mapped then what will be the size of tag array?**

Question 2 [10]

```
Loop:  ld R4, 200 (R2)
       subi R4, R4, 4
       ld R3, 300 (R2)
       subi R3, R3, 8
       Add R5, R4, R3
       st R5, 400 (R2)
       subi R2, R2, 4
       bne R2, R0, Loop
```

Consider the following specification for our pipelined processor:
Five stages MIPS pipeline where all arithmetic type instructions consume 1-cycle in each stage (5-cycle latency) but Instructions with data memory operation (Load, Store) consumes 2 cycles in the memory stage (6-cycle latency).
Forwarding has been implemented

a) **Add stalls in the above code for proper execution**

b) **Reschedule the code to remove as many stalls as possible**