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Student : Name:_____ Roll No._____

Question 1 [10]

Suppose we have a cache that has the following division of 32-bit address:

bits 0 - 5 = offset
bits 6 - 17 = index
bits 18 - 31 = tag

a. What is the total size of the cache (data bytes only) if above figures are considered for a direct mapped cache?
Cache size = no. of sets x associativity x block size
= 2^{12} x 1 x 2^{6}
= 256 KB

b. What is the total size of the cache (data bytes only) if above figures are considered for an 8-way set associative cache?
Cache size = no. of sets x associativity x block size
= 2^{12} x 8 x 2^{6}
= 2 MB

c. Calculate the number of sets for a 4-way set associate cache.
2^{12} = 4096

d. How many total bits of storage (tag+data +valid) are required if it is considered as an 8-way set associate cache
No. of sets x associativity x tag bits
2^{12} x 8 x 14

e. In case of an 8-way set associate cache, Into what set would bytes with each of the following addresses be stored

Set number (decimal)

0001 1011 1111 00**01 0001 0001 10**11 1010

0001 1100 1111 00**11 1111 0011 01**00 1101

Question 2 [15]

You need to design a memory system that has 32 bit address bus and 32 bit data bus. The memory system will have 2 cache levels.

- L1 cache is a 2-way set associative cache containing 64 MB data and has a line/block size of 64 bits
- L2 cache is a direct mapped cache containing 512 MB data and has a line/block size of 64 bits.

Design the memory system clearly showing the inter connection between the 2 caches and memory. You should label the tag, index and offset bits clearly with their relevant sizes. Also calculate the size of tag array for each cache.

No. of blocks of L1 are 2^{23} (64MB/8 = $2^{26}/2^3$)

No. of blocks of L2 are 2^{26} (512MB/8 = $2^{29}/2^3$)

Question 3 [10]

Each instruction fetch means a reference to the instruction cache and 35% of all instructions reference data memory (Load/Store instructions).

With the first implementation (separate instruction and data cache):
- The average miss rate in the L1 instruction cache was 5%
- The average miss rate in the L1 data cache was 12%
- In both cases, the miss penalty (time to access main memory) is 100 CCs

For the new design, with unified memory (same cache for instruction and data), the average miss rate is 8% for the cache as a whole, and the miss penalty is again 100 CCs.

a) **Which design is better and by how much?**

Seperate
AMAT = (1 + 0.05 x 100) + 35% (1 + 0.12 x 100)
= (1 + 5) + 0.35 (1 + 12)
= (6) + 0.35 (13)
= 6 + 4.55
= 10.55 clock cycles

Unified
AMAT = (1 + 0.08 x 100) + 35% (1 + 0.08 x 100)
= (1 + 8) + 0.35 (1 + 8)
= (9) + 0.35 (9)
= 9 + 3.15
= 12.15 clock cycles

The original design is better by 15% (12.15/10.55).

b) If we add L2 cache in the new design with access time equal to 20cc, it reduces the memory accesses to main memory from 8 % to 3%. What will be the new average memory access time?

AMAT = (1 + 0.08 x 20 +0.03 x 100) + 35% (1 + 0.08 x 20 + 0.03 x 100)
= (1 +1.6 +3) + 0.35 (1 +1.6 + 3)
= (5.6) + 0.35 (5.6)
= 5.6 + 1.96

= 7.56 clock cycles