National University of Computer and Emerging Sciences, Lahore Campus

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Student : Name:_____ **Roll No.**_____ **Section:**_____

NOTE: Answer in the space provided. You can ask for rough sheets but they won't be graded.

Question 1 [8] Encircle the right answer.

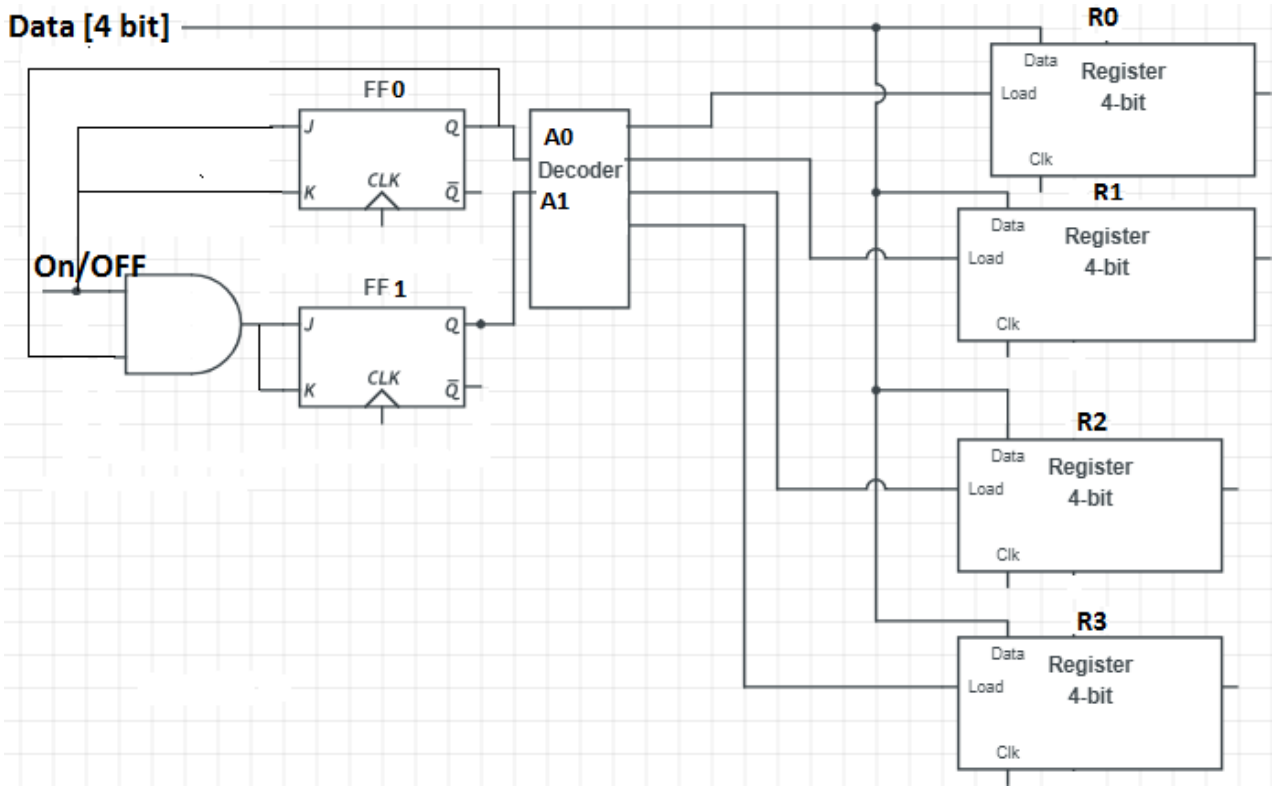
1. There are 32 general purpose registers. So a machine instruction must use a bit field of what size to designate a register?
   a) 3
   b) 4
   c) 5
   d) 16
2. How many bits are there in each MIPS machine instruction?
   a) 8
   b) 16
   c) 32
   d) Different instructions are of different lengths
3. Consider the following 32-bit j instruction 000010 00 0001 0000 0000 0000 0000 1000. The first 6 bits are the op-code and rests of the 26 bits are allocated for jump address. Here is the value of the PC+4 while the target address is being constructed: 0000 1000 0001 0000 0000 1100 0110 1000.
   What address does the j put into the PC?
   a) 0000 1000 0001 0000 0000 1100 0110 1000
   b) 0000 10 0001 0000 0000 1100 0110 1000 00
   c) 0000 00 0001 0000 0000 0000 0000 1000 00
   d) 1000 00 0001 0000 0000 0000 0000 1000 00
4. The value of the function field (funct) for lw and sw instructions is:
   a) 0
   b) 10
   c) 34
   d) Not applicable
5. A 3-to-8 decoder can be constructed with _____ 2-to-4 decoders:
   a) 1
   b) 2
   c) 3
   d) 4
6. A combinational circuit that receives binary information from one of 2^n input data lines and directs it to a single output line is called:
   a) Decoder
   b) Multiplexer
   c) Flip-flop
   d) Binary Counter
7. An overflow can be detected while performing arithmetic left shift by the following condition. Here R_{n-1} represents the MSB while R_0 represents the LSB.
   a) $R_{n-1} \wedge R_{n-2}$ (AND)
   b) $R_{n-1} \oplus R_{n-2}$
   c) $R_{n-1} \vee R_{n-2}$ (OR)
   d) $R_0 \oplus R_1$

8. In binary adder-subtractor, the addition and subtraction can be combined into one common circuit by including a/an _____ gate with each full adder:
    a) OR gate
    b) XOR gate
    c) NOR gate
    d) NOT gate (inverter)

Question 2 [8]

Consider the circuit below.

- FF0 and FF1 are JK Flip Flops and both are initialized to 0.
- All the circuit components are attached to the same clock (Although it is not mentioned in the circuit below)
- Each register(R0-R3) is 4 bit and the decoder is 2 x 4



Initial values for the registers are as follows

R0	1011
R1	0101
R2	1001
R3	0010

Following is the input to the circuit for next 5 Clock Cycles

1. Clock Cycle 1: ON/OFF : 1, Data: 0000
2. Clock Cycle 2: ON/OFF : 1, Data: 0000
3. Clock Cycle 3: ON/OFF : 1, Data: 1100
4. Clock Cycle 4: ON/OFF : 1, Data: 1100
5. Clock Cycle 5: ON/OFF : 1, Data: 1111

What are the contents of the registers after Clock Cycle 5? Fill in the table below to answer the question.

R0	**1111**
R1	**0000**
R2	**1100**
R3	**1100**

Question 3 [2+6+3+3]

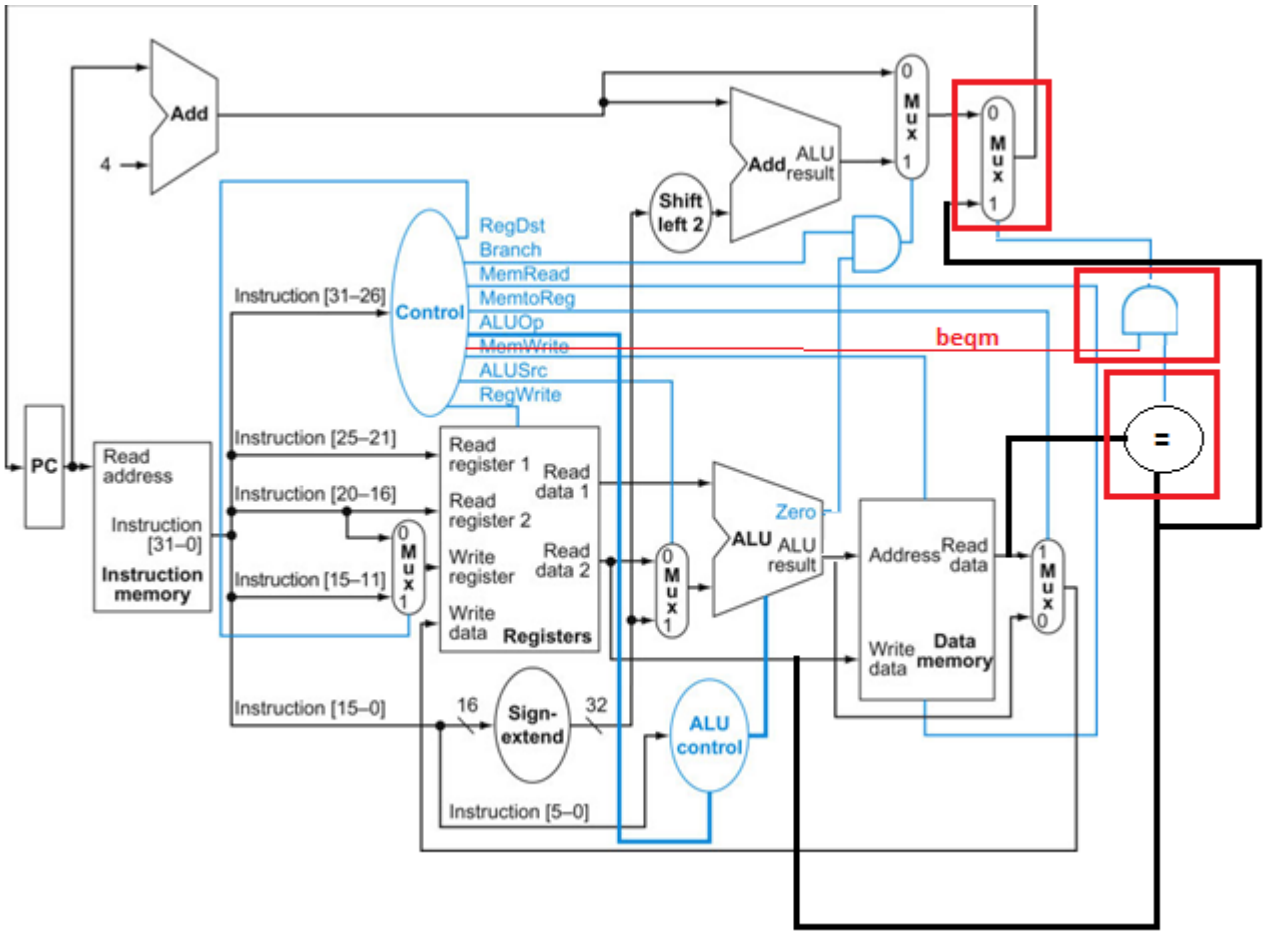
Suppose we want to add support for the following instruction in our MIPS architecture.

Instruction	RTL	Description
BeqM Rt, Rs, Offset	If Rt = = Mem[Offs +Rs] then PC = Rt	If the value in Rt is equal to the value at memory location (Offset + value in register Rs) then set PC to the value of Register Rt

a. Convert the following assembly instruction into 32 bit binary instruction
BeqM R9, R8, 44
(Opcode for BeqM instruction is 101101)

101101 01000 01001 0000000000101100

b. What must be changed in the data-path to add this instruction to the MIPS Instruction Set Architecture? Make the changes to the following diagram to answer this question. Use space provided around the diagram to draw any new required resources. You can draw lines from/to the diagram for input/output of these units. Draw neatly so that it's easier for the instructor to understand your logic.



c. For this instruction, specify the value of all control signals shown in the diagram plus any additional signals you may have added. Name the signal and briefly describe its purpose in the table below.

Control Signal	Value	Description
ALUOp	**00**	**2 bit value to ALU control for BeqM instruction**
RegDst	**x**	
Branch	**0**	
MemRead	**1**	
MemWrite	**0**	
MemToReg	**x**	
AluSrc	**1**	
RegWrite	**0**	
BeqM	**1**	**If this signal is 1 and Rt = = Mem[Offs +Rs] then set PC == Rt**

d. If each register contain the value equal to its register number (R4 contains value 4 etc.) and in Data memory at each address, value is double of its address (at address2, value is 4 and at address3, value is 6 etc.) then what would be the value of rt after the completion of **BeqM** instruction.

The value of Rt is simply the value stored in register Rt (R9 == 9)