| | | | | |
|---|---|---|---|---|
| | Course Name: | Advanced Computer Architecture | Course Code: | EE502 |
| | Program: | MS (Computer Science) | Semester: | Fall2020 |
| | Duration: | 90 Minutes | Total Marks: | 30 |
| | Paper Date: | 20-10-2020 | Weight | 15 |
| | Exam Type: | Midterm I Solution | Page(s): | 4 |

**Student : Name:_____ Roll No._____**

Instruction:
1. Attempt all question in the provided space. You can use rough sheets but it should not be attached.
2. If you think some information is missing, write assumption and solve accordingly.

## Question 1a [4](Multiple options can be selected in each question)

1. Structural hazards can be avoided by
   A. adding stalls
   B. forwarding
   C. **adding more hardware**
   D. register renaming

2. Typically during pipelined execution, the read operation on the register file and the memory is performed during _____
   A. first half of the cycle
   **B. later half of the cycle**
   C. any half of the cycle
   D. throughout the cycle

3. False data dependencies can be avoided by
   A. adding stalls
   B. forwarding
   C. adding more hardware
   D. **renaming**

4. We can convert an instruction into stall by
   A. disabling IF/ID register
   B. **converting all instruction bits in IF/ID to 0**
   C. **converting all control signals to 0**
   D. None of the above

## Question 1b [4]

Consider the following code snippet's execution on a 5-stage pipelined processor. Hazard detection and full forwarding is implemented

Instruction 1: Lw R1, R2, 20
Instruction 2: sub R2, R3, R4
Instruction 3: Add R1,R1,R2
Instruction 4: St R1, R2, 40
Instruction 5: Add R4,R5,R4

1. Is the following condition true for Instruction 1 and Instruction 3 at the start of 5th clock cycle?
   EX/Mem.RegisterRt = ID/EX.RegisterRs
   **True/False: ___FALSE_____**

2. Is the following condition true for Instruction 1 and Instruction 3 at the start of 5th clock cycle?
   MEM/WB.RegisterRt = ID/EX.RegisterRs
   **True/False: ___TRUE_____**

3. Is the following condition true for Instruction 2 and Instruction 4 at the start of 6th clock cycle?
   EX/MEM.RegisterRd = ID/EX.RegisterRs
   **True/False: ___ FALSE _____**

4. Is the following condition true for Instruction 3 and Instruction 4 at the start of 6th clock cycle?
   EX/MEM.RegisterRd = ID/EX.RegisterRs

   **True/False: ___ FALSE _____**

## Question 3[12]

Consider the following instruction sequence:

```
Loop:   ld R2, 20 (R6)
        addi R2, R2, 4
        add R4, R2, R3
        ld R5, R6, 8
        sw R4, 30 (R5)
        addi R6, R6, 4
        bne R6, R7, Loop
```

Assume that the following code is being run on 5-stage MIPS processor with each stage consuming one clock cycle and the branch is always predicted to be taken.

1. If there is no forwarding, how many cycles including stalls will be required to complete the execution of this code if values of the registers and memory are such that the loop takes only 2 iterations?

Required Cycles: ____**36**_____

Explain your answer by inserting stalls/NOPs in the code where the stalls are required.

```
Loop:   ld R2, 20 (R6)
        2 stalls
        addi R2, R2, 4
        2 stalls
        add R4, R2, R3
        ld R5, R6, 8
        2 stalls
        sw R4, 30 (R5)
        addi R6, R6, 4
        2 stalls
        bne R6, R7, Loop
        1 stall
```

2. Now consider that full forwarding and hazard detection unit is implemented, how many cycles including stalls will be required to complete execution of this code if values of the registers and memory are such that the loop takes only 2 iterations?
   Required Cycles: _____**26**_____
   Explain your answer by inserting stalls/NOPs in the code where the stalls are required.

```
Loop:   ld R2, 20 (R6)
        1 stall
        addi R2, R2, 4
        add R4, R2, R3
        ld R5, R6, 8
        1 stall
        sw R4, 30 (R5)
        addi R6, R6, 4
        1 stall
        bne R6, R7, Loop
        1 stall
```

**3.** Now consider the above code written in part 2 with forwarding available and reschedule the instructions to remove all stalls (Use unrolling if required to remove all stalls)

```
Loop:  ld R2, 20 (R6)
       ld R5, R6, 8

       addi R2, R2, 4
       addi R6, R6, 4

       add R4, R2, R3
       bne R6, R7, Loop
       sw R4, 30 (R5)
```

## Question3 [3+3+4]

A compiler designer is trying to decide between two code segments to be executed on a machine with clock rate 2 GHz. The hardware designers have provided the following data about the CPI for each class, and the instruction counts being considered for each code sequence.

| Instruction Class | CPI for Instructions of this class |
|---|---|
| A | 3 |
| B | 2 |

| | Instruction Count for each code Sequence | |
|---|---|---|
| Code Sequence | Class A type Instructions | Class B type Instructions |
| 1 | 4 | 3 |
| 2 | 2 | 4 |

1. How many cycles are required for code sequence1?

**18 Cycles**

2. What is the CPI for code sequence 2?

**2.33**

3. What is the execution time for each code sequence? Which will be faster?

**EX1 = $9 \times 10^{-9}$**

**EX2 = $7 \times 10^{-9}$**

**Sequence 2 is faster**