National University of Computer and Emerging Sciences, Lahore Campus

Course:	Computer Architecture	Course Code:	EE204
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Exam:	Mid1		

NOTE: Answer in the space provided. You can ask for rough sheets but they won't be graded.
If you think some information is missing, write your assumptions clearly and solve accordingly.

Question 1a [5]

1. The 8-bit signed extended value of $(1101)_2$ is **__1111 1101___.**
2. A multiplexor with 32 inputs will have **__1___** no. of outputs.
3. A + A′B + A′B′ = 0 True/**False**
4. A+B+C = A′B′C′ True/**False**
5. From what memory address does the following lw instruction read a word to store in the R1 register? lw R1, 4(R2). The address for lw instruction is 24. The register R2 contains 10.
   Memory read address:**___14____**

Question 1b [2+3]

a) Multiply $(0000\ 0101)_2$ with $(8)_{10}$ without using multiplier or multiplication algorithm. Brief the method.

Answer:

We can simply shift the number left 3 times which is equivalent to multiply by 8 so the answer will be 00101000

b) Convert the following number from IEEE 754 representation to decimal floating point representation.

1	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

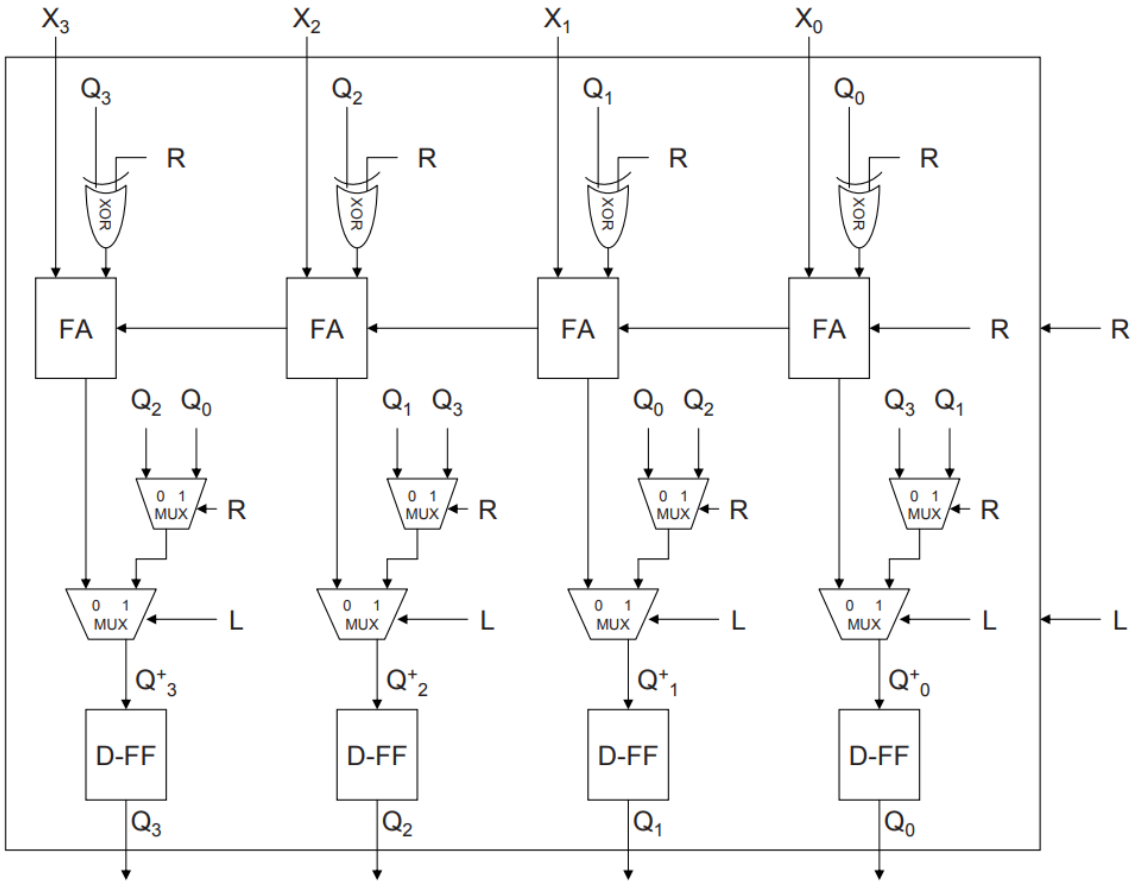
Show your working here:
- 1.01011×2^3

= -1010.11

= -10.75

Question 2[10]

Consider the following sequential circuit. Note that the names of wires are repeated for clarity. For example, the output of the far right D-FF (bottom), Q_0, is connected to the input of the far right XOR gate (top).It is assumed that the clock signal is provided to all D-FFs in the circuit. Being a sequential circuit, the output is dependent on the number of elapsed clock cycles.



For the following four input combinations, write the resulting output of the above circuit after specified number of cycles.

Inputs				After how many clock cycles?	Output after specified # of clock cycles
L	R	$X_3X_2X_1X_0$	$Q_3Q_2Q_1Q_0$		$Q^+_3Q^+_2Q^+_1Q^+_0$
0	0	0010	0011	1	**0101**
0	1	1101	0101	2	**0101**
1	0	1101	1011	2	**1110**
1	1	1100	0101	3	**1010**

Question 3[2+6+2]

Suppose we want to add support for the following instruction in our MIPS architecture.

Instruction	Operation being performed
addM Rt, Rs,offset	Rt ← M[Rs] + offset

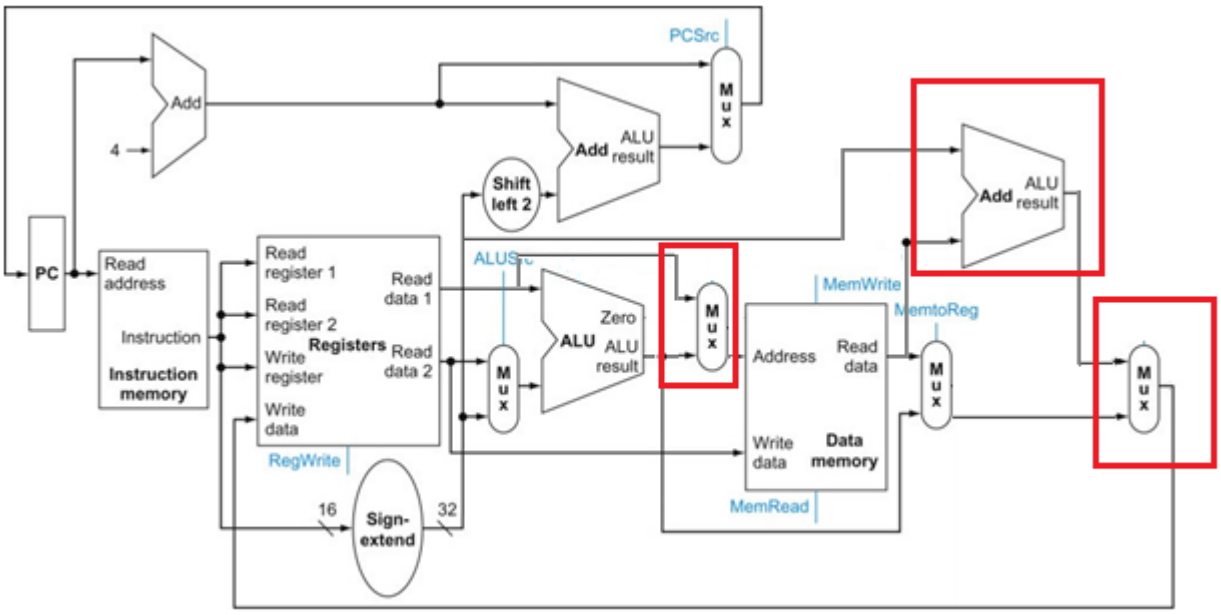
The **addM** instruction is a variant of 'add instruction' which adds two operands but one of the operands is a memory value. Example of this kind of instruction is as follows:

addM R5, R2, -45

The first operand of add instruction is memory value at address stored in register R2 and second operand is the immediate signed value. The result will be stored in R5 register. This is an I-type instruction with opcode 110011.

a) Convert the assembly language instruction (**addM R5, R2, -45**) to 32-bit instruction bits.
110011 00010 00101 1111111111010011

b) What must be changed in the following data-path to add support for this instruction to the MIPS Instruction Set Architecture? Draw any new required resources and join them with lines from/to the diagram for input/output of these units. Draw neatly so that it's easier for the instructor to understand your logic.



c) Identify which resources (blocks) produce outputs but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?

ALU not required for this instruction

Adder for branch not required for this instruction

Data Memory produces no output for this instruction