Computer Architecture (EE 204)

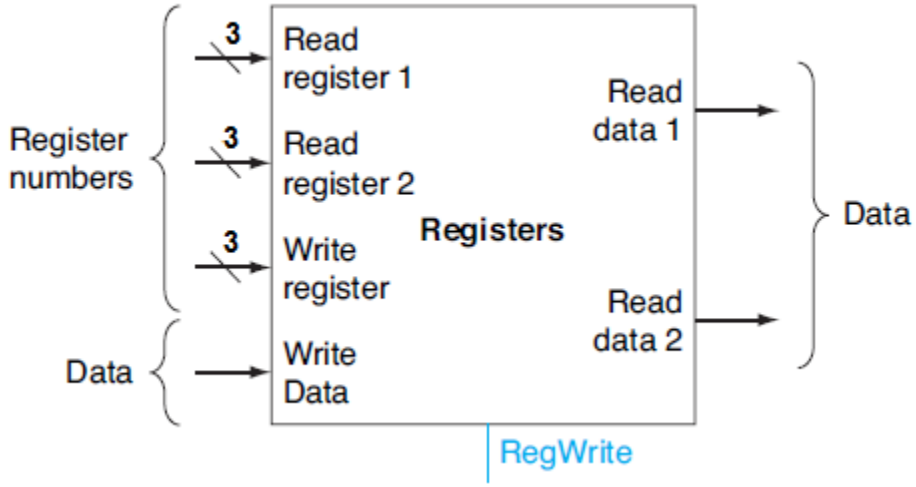
Assignment # 2, Total marks 60 Due Date: 17 – 10 -2016

Plagiarism policy: All the students involved will be awarded zero in the first instance.
You need to submit hardcopy. Please show your work clearly.

Assignment Description:
Assignment covers concepts related to MIPS Datapath, Control Unit, Arithmatic Unit, Performance of the system.

Question1: **(20 marks)**

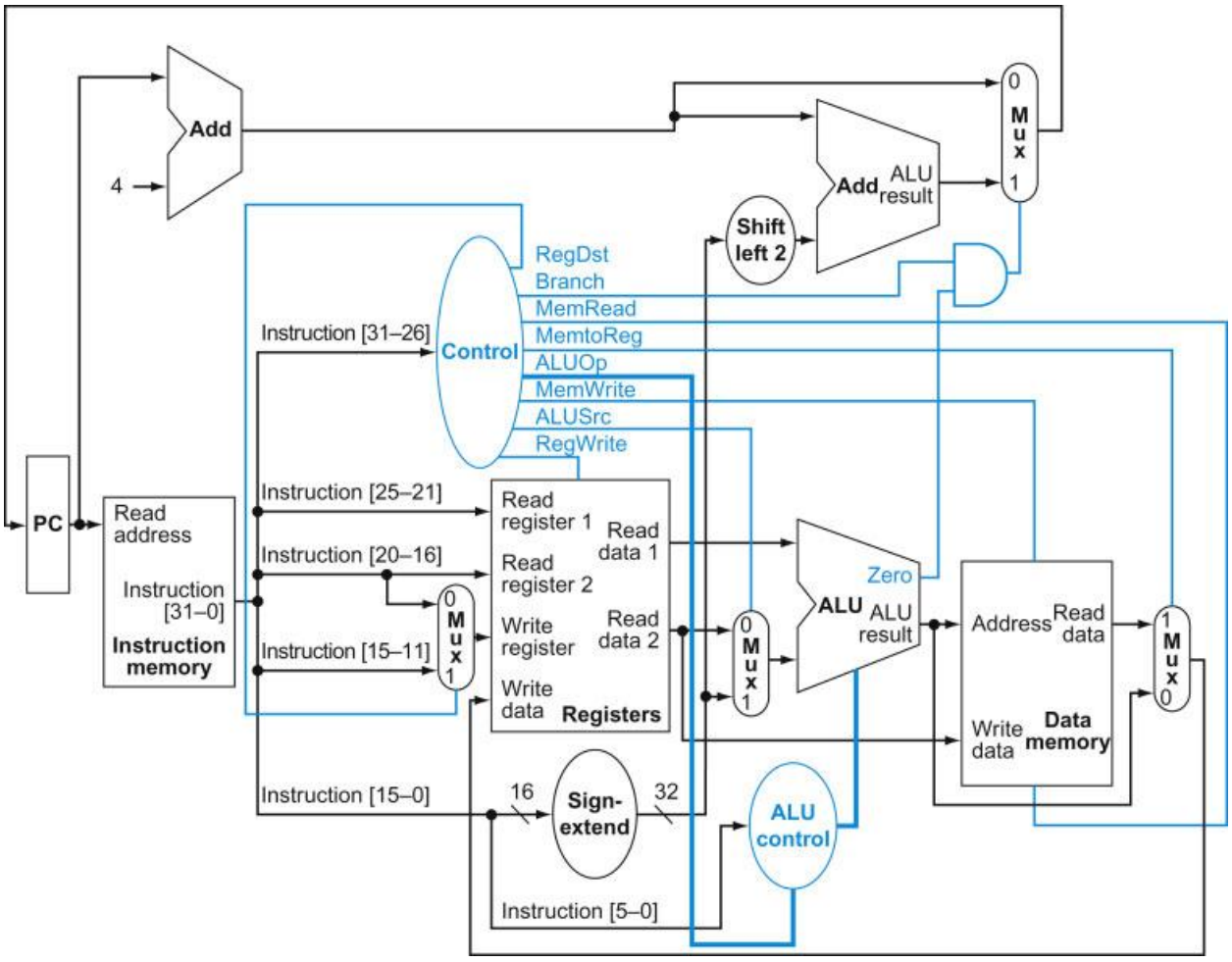
We have studied Register file in MIPS datapath which is as follows.



Till now we considered it as a block box but inactual that is built using different components. In this question you have to design the complete functionality of Register file. Show Registers and circuitry to choose specific register based on inputs and write its contents on Data ports and also the support to add Data contents onto the registers.

Question2: **(5+10 marks)**

We have studied a single-cycle MIPS as shown below with datapath and control unit.



a) We want to add support for the following instructions:
Jump R
that jumps to the instruction with address contained in register R. Add support for this instruction in current implementation by adding datapath units, MUXes, data wires, and control signals in order to handle jump register (Jump R) instructions.

b) Sub3 R3, R2, R1
The above mentioned Sub3 instruction is used to do subtraction in the following manner. It will add R1 and R2 and then it will subtract this result from R3. The resultant result will be stored in R3. Register R3 is used as a source as well as a destination.

Add support for the above mentioned instructions by adding datapath units, MUXes, data wires, and control signals in order to handle "addA".

Question3: **(10 marks)**

Processor X has a clock speed of 1 GHz, and takes 1 cycle for integer operations, 2 cycles for memory operations, and 4 cycles for floating point operations. Empirical data shows that programs run on Processor X typically are composed of 35% floating point operations, 30% memory operations, and 35% integer operations. You are designing Processor Y, an improvement on Processor X which will run the same programs and you have 2 options to improve the performance:

1. Increase the clock speed to 1.2 GHz, but memory operations take 3 cycles
2. Decrease the clock speed to 900 MHz, but floating point operations only take 3 cycles

Compute the speedup for both options and decide the option Processor Y should take.

Question 4: **(15 marks)**

Following are 3 instructions in hexadecimal format for a single-cycle MIPS datapath shown in Question 3 above.

1. **0x AE2A0028**
2. **0x 01288020**
3. **0x 1573FFFC**

Decode these instructions and provide details like instruction type, micro-operation being performed and control singals being generated for each instruction.
You can see op-codes for different instructions