	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS (Computer Science)	Semester:	Fall 2020
	Duration:	90 Minutes	Total Marks:	30
	Paper Date:	17-10-2020	Weight	20
	Exam Type:	Midterm I	Page(s):	4

Student : Name:_____ Roll No._____ Section: _____

Instruction:
1. Attempt all questions in the provided space. You can use rough sheets but it should not be attached.
2. If you think some information is missing, write assumption and solve accordingly.

Question 1a [4+2+4]

a) Minimize the following equation using Boolean algebra and also draw circuit diagram.

$$A\,B + \overline{A}\,C\,D + \overline{A}\,B\,D + \overline{A}\,C\,\overline{D} + A\,B\,C\,D$$

Simplification/Minimization steps	Circuit Diagram

b) Divide $(01010000)_2$ with $(16)_{10}$ without using divider or add/subtract operations. Brief the method by telling the operation being used to achieve the required functionality.
Answer:

c) Convert the following floating point number to IEEE 754 representation.
6.022×10^3

Show your working here:

Question 2[2+6+2]

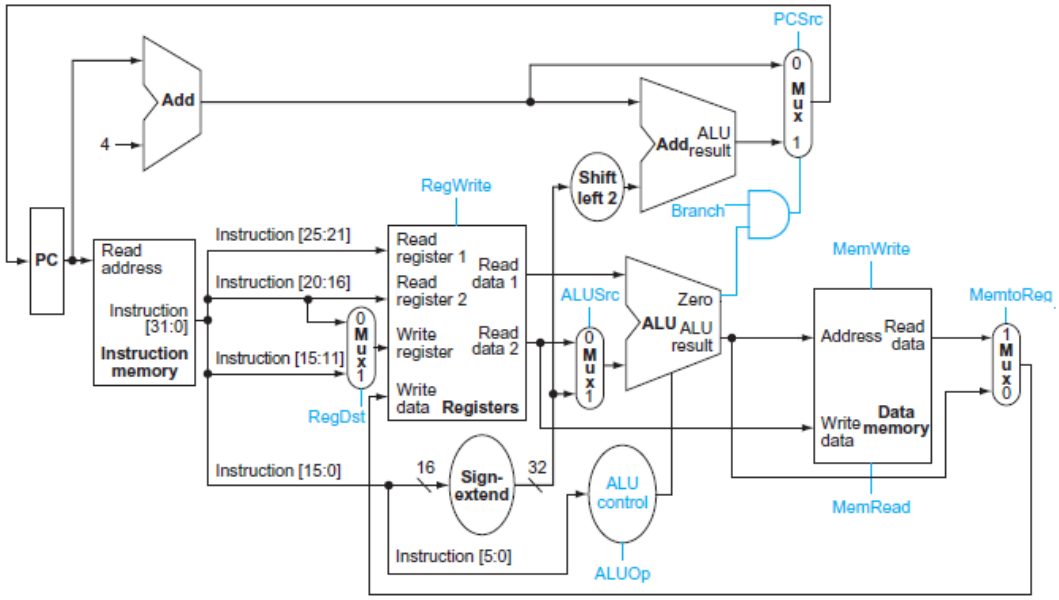
Suppose we want to add support for the following instruction in our MIPS architecture.

BeM Rs,Rt, offset	If Mem[Rs] = = Rt then PC = PC + offset

The **BeM** instruction is a variant of 'branch instruction' which compares the value of **Rt** register with memory value at address pointed by Register **Rs**.
Example of this kind of instruction is as follows:
BeM R5, R2, 28
This is an I-type instruction with opcode 101011.

a) Convert the assembly language instruction (**BeM R5, R2, 28**) to 32-bit instruction bits.

b) What must be changed in the following data-path to add support for this instruction to the MIPS Instruction Set Architecture? Draw any new required resources and join them with lines from/to the diagram for input/output of these units. Draw neatly so that it's easier for the instructor to understand your logic.



c) Write the value of each control signal when the above instruction is decoded. Also mention if any new signal is needed.

Control Signal	Value
RegDst	
Branch	
MemRead	
MemWrite	
MemToReg	
AluSrc	
RegWrite	

Question 3[2+3+5]

Consider following code snippet for execution on a 5-stage pipelined processor. Assuming that data hazard cannot occur in the processor.

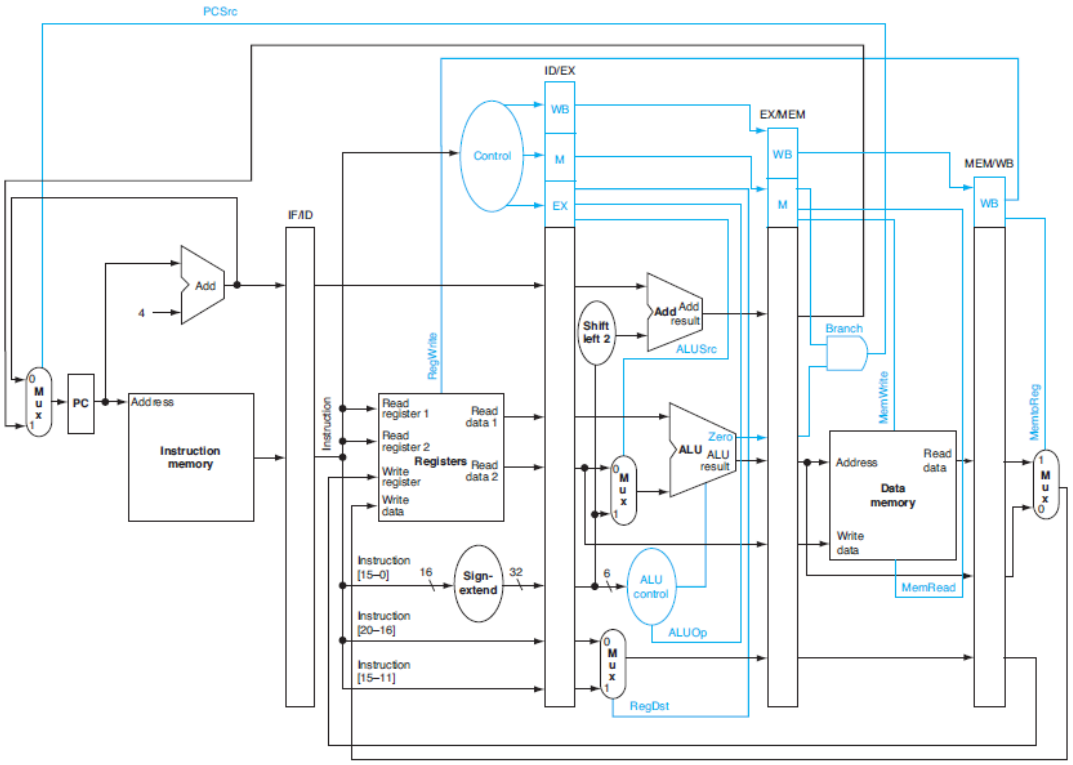
Add R1, R2, R3
Sub R4, R5, R6
Lw R7, 16(R8)
Add R9, R10,R11
Sw R12, 100(R13)

a. How many clock cycles are required for execution of the code?

b. Consider clock cycle no. 5, write down instructions that will be executing in each of the following stages.

Pipeline Stage	**Instruction**
Instruction Fetch	
Instruction Decode	
Execution	
Memory Stage	
Write back	

c. Considering the following pipelined figure, whatwould be the contents stored in ID/EX stage in clock cycle no. 5 (Data values, control signal values).



PC Value when the first instruction is fetched = 0x000….0010 (32-bit hex value with left most 30 bits equal to 0)

Content type/name	**Value**
e.g Value of RS register	