National University of Computer and Emerging Sciences, Lahore Campus

Course:	Advance Computer Architecture	Course Code:	EE502
Program:	MS(Computer Science)	Semester:	Spring 2017
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Section:	A	Weight	3.3
Exam:	Assignment 2	Page(s):	2

Question1: **[25 marks]**

Consider the following MIPS assembly language loop. Assume that we run this code on the 5 stages pipelined data path. Adder requires 2 cycles and Multiplier requires 3 cycles. Forwarding has been implemented.

```
1. Loop: ld R4, 0(R1)
2.       mul R4, R4, R0
3.       ld R5, 0(R2)
4.       add R4, R4, R5
5.       sw R4, 0(R2)
6.       sub R3, R3, 1
7.       addi R1, R1, 4
8.       addi R2, R2, 4
9.       bne R3, 0, Loop
```

a) Find all possible hazards in the above code. Write numbers of both instructions in front of the following if a specific hazard exists (e.g. 1 & 2, 3 & 4, ...)

WAR:
WAW:
RAW:

b) Add stalls in the above code. Find the number of clock cycles needed to execute this code (all iterations), accounting for all possible stalls. Assume that R3 is initially set to 10.

c) Re-arrange the instructions in the code above to eliminate as many stall cycles as possible. If all stalls are not eliminated then do 2-level loop unrolling.

Question 2: **[20+20+5 marks]**

Consider the following MIPS assembly code to be executed on a pipelined CPU with frequency of 3 GHz.

Assume initial value of R6 = 0 and R7 = 10

```
Loop: beq R6, R7, END
      ld R2, 100 (R6)
      ld R3, 200 (R6)
      add R2, R2, R3
      sw R2, 100 (R6)
      addi R6, R6, 4
      j  Loop
END:
```

Your task is to do dynamic scheduling based on Score boarding and Tomasulo algorithms. There are:

- **2 LOAD/STORE Functional Units (LDU1) with latency of 4 cycles**
- **2 ALU/BR Function Units (ALU1) with latency 2 cycle**
- **2 RESERVATION STATIONS (RS1, RS2) for ALU/BR operation**
- **2 Buffers for LOAD/STORE (LDST1, LDST2)**

Moreover you have to identify:

- **Structural hazards for RS in ISSUE phase**
- **RAW hazards and Structural hazards for FUs in START EXECUTE phase**

Assume static branch prediction (backward taken, forward not taken) is used.

a) **Show two iterations of the loop using scoreboarding**
b) **Show two iterations of the loop using tomasulo**
c) **If the clock frequency is 3GHz, what would be average CPI in both cases, and speed up.**

Note: Reservations stations are only usable in Tomasulo, not in scoreboarding.