		Course Name:	Computer Architecture	Course Code:	EE204
		Program:	BS(Computer Science)	Semester:	Fall 2019
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Student : Name:_____ Roll No._____ Section:_____

Question 1 [6]

What is the difference between following memories: OTP, EEPROM and NVRAM in terms of write ability and storage permanence?

Question 2 [14]

1. **L1: lw R3, 100 (R4)**
2. **Mul R5, R3, 8**
3. **lw R2, 200 (R4)**
4. **add R6, R2, R5**
5. **sw R6, 100 (R4)**
6. **add R4, R4, 4**
7. **bne R4, R7, L1**

Consider the following specification for our pipelined processor:
Five stages MIPS pipeline where multiplication consumes 4 cycles in execution. All other instructions consumes 1 cycle in each stage. Branch calculation is done in decode stage.
Full Forwarding has been implemented.

a) Add stalls in the above code to avoid data and control hazards	**b) Rearrange the code to remove stalls**

c) Perform 2-level un-roll and reschedule the code to remove as many stalls as possible

Unrolled code	**Rescheduled unrolled code**