National University of Computer and Emerging Sciences, Lahore Campus

Course:	**Computer Architecture**	**Course Code:**	**EE204**
Program:	**BS(Computer Science)**	**Semester:**	**Fall 2018**
Due Date:	**6-12-2018**	**Total Marks:**	**10**
Section:	**C**	**Weight**	**3**
Exam:	**Quiz 4**	**Page(s):**	**1**

Question 1:

(10 marks)

You have 3 cache designs for a 16-bit address machine.

Alpha: Direct-mapped cache. Each cache line is 1 byte. 10-bit index, 6-bit tag. 1 cycle hit time.
Bravo: 2-way set associative cache. Each cache line is 1 word (4 bytes). 7-bit index, 7-bit tag. 2 cycle hit time.
Charlie: fully associative cache with 256 cache lines. Each cache line is 1 word. 14-bit tag. 5 cycle hit time.

	Alpha	Bravo	Charlie
What is the total size of the cache in KB? (3 marks)			
How much space does each cache need to store tags? (3 marks)			
Which cache design has the most conflict misses? Which has the least? (1 mark)			
If someone told you the hit rate for the 3 caches is 50%, 70% and 90% but did not tell you which hit rate corresponds to which cache, which cache would you guess corresponded to which hit rate? (3 marks)			
Assuming the miss time for each is 20 cycles, what is the average service time for each? (Service Time = (hit rate)*(hit time) + (miss rate)*(miss time)). ***[not graded]***			