Computer Architecture (CS-E) **Quiz2**
Date: 30-10-2018
Roll No: _____
Question1:

```
Loop: ADD R1,R2,R1
      LW R2,0(R1)
      LW R2,16(R2)
      Sub R4,R3,R2
      BEQ R4,R5,Loop
```

Show a pipeline execution diagram for the third iteration of this loop, from the cycle in which we fetch the first instruction of that iteration up to (but not including) the cycle in which we can fetch the first instruction of the next iteration. Show all instructions that are in the pipeline during these cycles (not just those from the third iteration). Assume that the hazard detection unit is present, however, the forwarding unit is not added to the pipelined processor yet. You might have to insert stalls to make the execution work properly.