Computer Architecture – Fall 2020

Assignment # 1

Due Date: *25/09/2020*
Time: *5 pm*

You may be called for evaluation of this assignment and you will have to justify your solutions before the course instructors and the TA. Failure to justify your answers will result in negative marks. Severity of the plagiarism can result in F as well.

Q1: Using a table similar to that shown in Slide 15 of the slides shared as "4. Multiplication & Division Architecture", calculate 75 divided by 20 using the hardware and algorithm described in Slide 14. You should show the contents of each register on each step.

Q2: Repeat Q1 with the hardware shown on in Slide 16 of the slides shared as "4. Multiplication & Division Architecture" i.e. Improved Version for the division algorithm

Q3. Write down the binary representation of the following decimal numbers, assuming the IEEE 754 single precision format.

a. 65.24
b. -23.765

Q4. Write down the binary representation of the decimal number, assuming the IEEE 754 double precision format.

a. 65.24
b. -23.765

Q5. Compute following addition using the Floating Point Addition algorithm from Slide 8 of the slides shared as "5. Data Representation"

$$2.6125 \times 10^{1} + 4.1503 \times 10^{-1}$$

Assume that we need to store 5-bit precision for the final answer, hence, compute the Round off step appropriately.

a. Show all steps of the algorithm.
b. Display the answer in the IEEE 754 single precision format.