Computer Architecture – Fall 2020

Assignment # 3

Due Date: 06/11/2020
Time: 5 pm

You may be called for evaluation of this assignment and you will have to justify your solutions before the course instructors and the TA. Failure to justify your answers will result in negative marks. Severity of the plagiarism can result in F as well.

Question 1: Consider following instructions

a. ADDM Rd,Rt+Offs(Rs) Rd=Rt+Mem[Offs+Rs]
b. BEQM Rd,Rt,Offs(Rs) if Rt=Mem[Offs+Rs] then PC = Rd

Answer following questions for each of the above instructions separately

1. What must be changed in the pipelined datapath to add this instruction to the MIPS ISA(Instruction Set Architecture)? [Take the diagram of the architecture and make changes to it and paste here]
2. Which new control signals must be added to your pipeline?
3. Does support for this instruction introduce any new hazards? If yes, explain with the help of an example. If not, explain with proper reasoning.
4. Are stalls due to existing hazards made worse? If yes, explain with an example if these instructions can cause more stalls to some sequence of instructions. If not, explain with proper reasoning.

Question 2: Consider following two loops and answer questions below separately for each loop. Assume that the loop takes 2 iterations before exiting.

Loop: ADD R1,R2,R1
LW R2,0(R1)
LW R2,16(R2)
Sub R1,R2,R1
BEQ R1,R9,Loop

Loop: SW R1,0(R1) AND R1,R1,R2 LW R1,0(R1) LW R1,0(R1) BEQ R1,R0,Loop

How many stalls are required to execute these 2 iterations? Show a pipeline execution diagram which shows complete flow of the instructions along with all possible stalls for following MIPs processor

1. A processor without any forwarding and hazard detection hardware. Also, branch related hardware is not moved to ID stage yet.
2. A processor with forwarding hardware but without hazard detection hardware at ID stage. Also, branch related hardware is not moved to ID stage yet. [Hint: carefully handle load-use hazard]
3. A processor with forwarding, hazard detection unit and branch related hardware moved to ID stage.
4. At the start of the cycle in which we fetch the first instruction of the third iteration of this loop, what is stored in the IF/ID register in the processor with forwarding, hazard detection unit and branch related hardware moved to ID stage.