# Computer Architecture – Fall 2020

Assignment # 6

**Due Date:** *December 24, 2020*
**Time:** *5 pm*

***Question 1:*** Assume 4 KB pages, a 4-entry fully associative TLB, and LRU replacement. What will be the contents of the TLB if the following virtual addresses are generated by the system

**3769, 2127, 11916, 30587, 41870, 13608, 41225, 3169, 2147, 12916, 31587, 41871, 13609, 41225**

Consider the start of the system where nothing is placed in the TLB and page table. Bring the pages to the main memory as required by the address references above and show the page table and TLB updates for each reference separately.

| Valid | Tag | Physical Page number |
|---|---|---|
| | | |
| | | |
| | | |

| Valid | Physical page number or in Disk |
|---|---|
| | |
| | |
| | |
| | |

***Question 2:*** Repeat question 1 with following parameters changed

1. Page size is 16KB
2. TLB is 2-way set associative

***Question 3:*** Compare the two approaches of Question 1 & 2 and give your observations on how the page size and associativity effected the miss rate.