Computer Architecture

Quiz 1

Total Marks: 20

Name:_____ Student Id:_____

Section:____

Question 1:

Marks 10

How an instruction is decoded in the second stage of MIPS data path? Draw all components that are being used in this stage and also show control signals that are required at this stage. You do not have to design control unit. Just write the value of control singles for R-Type instructions that are required in decode stage.

Question 2:

Marks 10

Suppose you have three processes P1, P2, and P3 with clock speeds of 4 GHz, 1 GHz , 7 GHz and Average cycles per instruction as 3, 1, 5 respectively. If they execute the same instruction set then calculate performance

(a) Calculate performance of each one of them and identify the processor with maximum performance.

(b) If processor P1 executes a program in 20 seconds, find the number of cycles and number of instructions.