Computer Architecture – Fall 2020

Assignment # 4

Due Date: *22/11/2020*
Time: *5 pm*

You may be called for evaluation of this assignment and you will have to justify your solutions before the course instructors and the TA. Failure to justify your answers will result in negative marks. Severity of the plagiarism can result in F as well.

You can expect a class presentation for your solution where you will have to solve the questions in front of the class. You can expect to have cross questioning from the instructor, TA or classmates.

Q1. Schedule one iteration of the following loop on a 2-issue processor that can execute R-Type & Branch type instructions in first slot, whereas memory instructions can be issued in the second slot only

```
Loop:
        ADD R1,R2,R1
        LW R2,0(R1)
        LW R3,16(R2)
        Sub R1,R2,R3
        SW R1, 0(R5)
        Add R5,R5,4
        BEQ R1,R9,Loop
```

Show scheduled code for 2-issue processor by filling following table

Slot 1: Only R-TYPE/Branch Instructions allowed	Slot 2: Only Mem Type instructions allowed

Q2. Unroll loop from Q1 two times and schedule it on 2-issue processor having same properties as described in Q1. Give followings to answer this part properly

1. Show two iterations of the code
2. Show two iterations with reduced instructions (if possible to reduce number of instructions)
3. Show code with renamed registers
4. Show scheduled code for 2-issue processor by filling following table

Slot 1: Only R-TYPE/Branch Instructions allowed	Slot 2: Only Mem Type instructions allowed