National University of Computer and Emerging Sciences, Lahore Campus

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Course Name:	Advance Computer Architecture	Course Code:	EE502
Program:	MS (Computer Science)	Semester:	Fall2018
Duration:	90 Minutes	Total Marks:	40
Paper Date:	31-10-2018	Weight	20
Exam Type:	Midterm	Page(s):	6

Student : Name: Roll No.

Instruction:

- 1. Attempt all question in the provided space. You can use rough sheets but it should not be attached.
- 2. If you think some information is missing, write assumption and solve accordingly.

Question 1 [5]

- 1. Which of the following statements regarding pipeline hazards is TRUE? (Multiple options can be selected)
 - A. All data hazards can be avoided by forwarding
 - B. Branching causes both data and control hazards
 - C. Data hazards may cause error in execution result
 - D. Structural hazards occur whenever an instruction depends on another for operand
 - E. None of the above
- 2. Following MIPS code fragment is executed on the 5-stage pipelined datapath with forwarding.

add R3, R1, R2

sub R1, R1, R2

andi R2, R3, 0xFF

In the EX stage, the operand R3 for the **andi** instruction gets forwarded from

- A. Pipeline register IF/ID
- B. Pipeline register ID/EX
- C. Pipeline register EX/MEM
- D. Pipeline register MEM/WB
- E. No forwarding is necessary
- 3. CPU time can be reduced by reducing: (Multiple options can be selected)
 - A. Instruction count
 - B. Clocks per instruction
 - C. Clock cycle time
 - D. Clock frequency
 - E. None of the above
- 4. How many stall cycles will be introduced during execution of the following code fragment on a 5-stage pipelined datapath without forwarding?

ADD R3, R3, R1

SUB R3, R1,R2

SW R3, 2 (R1)

- A. 0
- B. 1
- C. 2
- D. 3
- E. 4
- 5. Structural hazards can be avoided by (Multiple options can be selected)
 - A. adding stalls
 - B. forwarding
 - C. adding more hardware
 - D. register renaming
 - E. loop unrolling

Question 2[15] Loop: LD R2, 100 (R4) Addi R2, R2, 4 LD R3, 200 (R4) Addi R3, R3, 8 Add R5, R2, R3 ST R5, 300 (R4) Addi R4, R4, 4 bne R4, R7, Loop Consider the following specifive stages MIPS pipeline Instructions with data memory

bne R4, R7, Loop Consider the following specification for our pipelined processor: Five stages MIPS pipeline where all arithmetic type instructions consume 1-cycle in each stage (5-cycle latency) but Instructions with data memory operation (Load, Store) consumes 2 cycles in the memory stage (6-cycle latency). Forwarding has been implemented a) Add stalls in the above code for proper execution b) Reschedule the code to remove as many stalls as possible

c)	If stalls are not remove stalls.	removed	in	part	(b)	then	do	2-level	loop	unrolling	and	then	reschedule	the	code	to

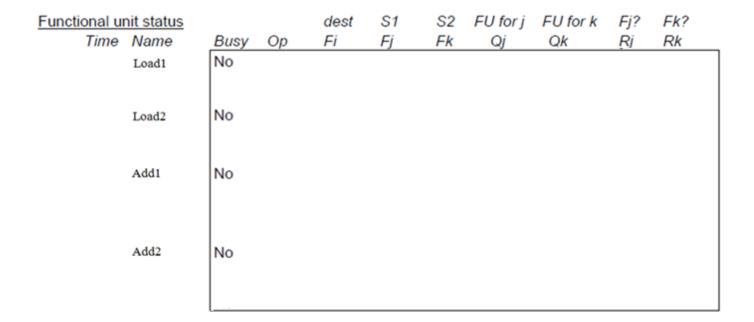
Question 3[15]

Loop: LD R2, 100 (R4)
Addi R2, R2, 4
LD R3, 200 (R4)
Addi R3, R3, 8
Add R5, R2, R3
ST R5, 300 (R4)
Addi R4, R4, 4
bne R4, R7, Loop

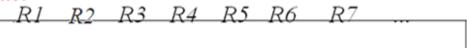
The above program is to be executed on a CPU with dynamic scheduling based on the SCOREBOARD technique with:

- o 2 LOAD/STORE Functional Units (Load1, Load2) with latency 2 cycles
- o 2 ALU/BR Functional Units (Add1, Add2) with latency 1 cycle
- o Check structural hazards in ISSUE phase
- o Check RAW hazards in READ OPERANDS phase
- o Check WAR and WAW in WRITE BACK phase
- o No forwarding
- O Static branch prediction for backward branches: branch always taken
- a) Show one iteration of this loop using SCOREBOARDING technique
- b) If the processor clock cycle is 2 ns, calculate CPI and execution time for 1 iteration of this code.

Instruction status:		Read	Exec	Exec	Write
Instruction Instruction	Issue	Operands	Start	Comp	Result
Loop: LDR2, 100 (R4)					
Addi R2, R2, 4					
LDR3, 200 (R4) AddiR3, R3, 8					
Add R5, R2, R3					
STR5, 300 (R4)					
AddiR4, R4,4 bne R4, R7, Loop					



Register result status:



Answer for part b:

Question 4 [5] Suppose the execution time of a program is 200 milliseconds. 120 milliseconds of this time is spent on multiplication, 40 milliseconds on addition and 40 milliseconds on load store instruction. How much do we have to improve the speed of multiplication if we want the program to run 2 times faster?