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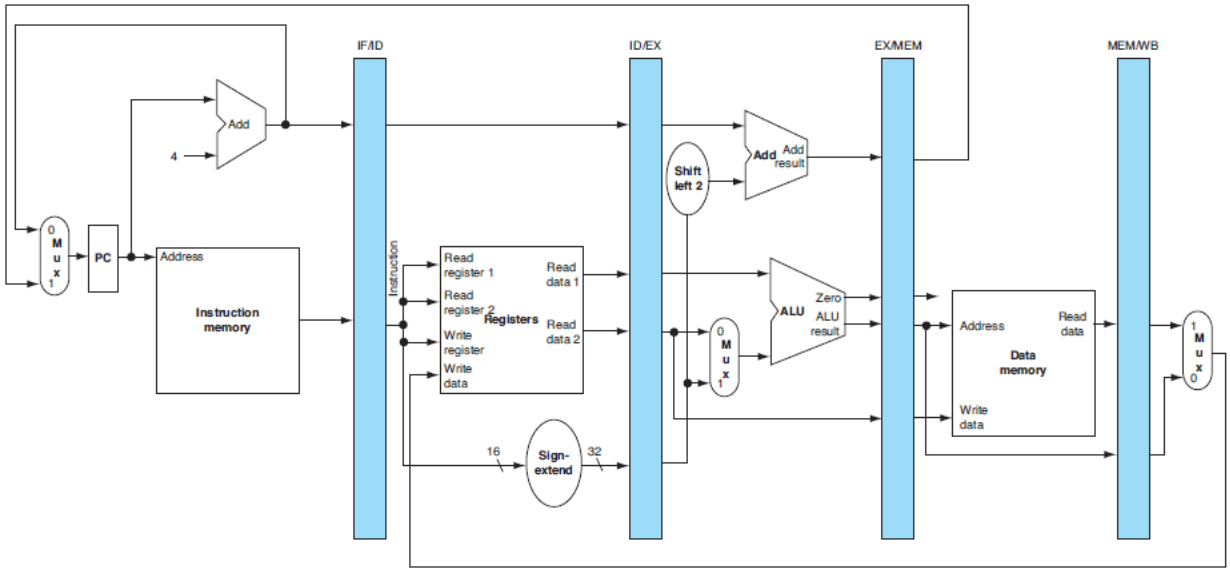
**Student : Name:_____ Roll No._____ Section:_____**

# Question 1 [10]




Suppose we have the following **generic architecture with maximum 5 stages**. We want to customize our architecture **where we may not need all stages or all components.**

Latencies of the major elements used in processor design are as follows:

| Instruction Memory | Adder | Mux | ALU | Register File | Data Memory | Sign-Extension unit | Shift-Left Unit |
|---|---|---|---|---|---|---|---|
| 250ps | 50ps | 30ps | 120ps | 150ps | 300ps | 20ps | 5ps |

1. What is the clock cycle time if the only type of instructions we need to support are ALU instructions in a Single Cycle processor (Un-pipelined)?
   Clock Cycle Time: _____

2. What is the clock cycle time if the only type of instructions we need to support are ALU instructions in a Pipelined processor?
   Clock Cycle Time: _____

3. What is the total latency of the lw instruction (Load word instruction) in a un-pipelined processor?
   Clock Cycle Time: _____

4. What is the total latency of the lw instruction (Load word instruction) in a pipelined processor?
   Clock Cycle Time: _____

# Question 2 [3+3+4]

**Consider three different processors P1, P2, and P3.**
**P1 has a 3 GHz clock rate and a CPI of 1.5.**
**P2 has a 2.5 GHz clock rate and a CPI of 1.0.**
**P3 has a 4.0 GHz clock rate and has a CPI of 2.2.**

**a. If a program is executed on each one of them, which processor has the highest performance?**

**Processor: _____**

**Instructions per second: _____**
**Calculations:**

**b. Now let's suppose the best processor identified in part (a) executes a program in 10 seconds, find the number of cycles and the number of instructions of the program.**

**Number of Cycles: _____**

**Number of Instructions of the Program: _____**
**Calculations:**

**c. We want to reduce the execution time of this processor by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?**

**Clock Rate:_____**
**Calculations:**