Course Name:	Computer Architecture	Course Code:	EE204
Program:	BS(Computer Science)	Semester:	Fall 2019
Duration:	30 Minutes	Total Marks:	20
Paper Date:	09-10-2019	Weight	~3
Exam Type:	Quiz 2d	Page(s):	2

Student : Name:_____ Roll No._____
Section:_____

Question 1a [4]

New control signal are generated at each clock cycle in a pipelined processor. However instruction at each stage requires its own signals in different stages. How this problem is handled in Multi-cylce MIPS pipeline?

Question 1b [6]

We have a program that runs in 15 seconds on computer A, which has a clock speed of 300 Mhz. Another computer B runs the same program in 10 seconds. We only know that clock cycles required in Computer B are double as compared to Computer A. Calculate the clock rate of Computer B.

Question 2 [3+4+3]

a) If we have the following times for 6-staged Pipelined MIPS architecture: 20ns, 25ns, 10ns, 40ns, 10ns and 15ns then what would be the frequency of the processor and latency of a single instruction.

b) If we have the liberty to convert it into 7-staged pipeline by splitting any one stage into two equal stages then which stage should be split and what would be the new frequency and latency of a single instruction.

c) Calculate the speedup we obtain by using 7-staged pipeline.