National University of Computer and Emerging Sciences, Lahore Campus

Course:	Advance Computer Architecture	Course Code:	EE502
Program:	MS(Computer Science)	Semester:	Spring 2017
Submission Date:	2/4-05-2017	Total Marks:	50
Section:	A	Weight	3.3
Exam:	Assignment 3	Page(s):	2

Due date: As mentioned in class, if you have presentation on Thursday then you have to submit your assignment on Tuesday 2nd of May and if you have presentation on Tuesday then you can submit assignment till Thursday, 4th of May, 2017.

Question1: **[20 marks]**

Consider the following program that will be executed on a **2-issue Superscalar MIPS** architecture with **Static Branch Prediction (BACKWARD TAKEN FORWARD NOT TAKEN)**

Consider the following specification for our pipelined processor:

- **1 ALU/BRANCH** and **1 LOAD/STORE unit**
- Five stages MIPS with each stage of the pipeline consuming 1 clock cycle
- **Forwarding is implemented**
- Computation of PC and TARGET ADDRESS for branch & jump instructions anticipated in the **ID stage**

```
L1: lw R2, 100 (R4)
addi R2, R2, 4
lw R3, 200 (R4)
addi R3, R3, 8
add R5, R2, R3
sw R5, 300 (R4)
addi R4, R4, 4
bne R4, R7, L1
```

Complete the pipeline scheme **by inserting instructions in the proper issue line as well as the stalls** needed to solve the given hazards

Question 2: **[10 marks]**

a) Design and draw complete diagram of a 4-way set associative, 8MB cache with data bus size of 32 bits (4 bytes) and a cache line size of 128 bits (16 bytes). The address bus for the memory system is 64 bits wide. You need to label each connection properly in order to receive full marks.

b) What is the size of the maximum memory that can be addressed by the memory system in which this cache is used?

Question 3: **[20 marks]**

Suppose we have separate direct-mapped L1 instruction and data caches that both have the following division of 32-bit address:

bits 0 - 4 = offset
bits 5 - 14 = index
bits 15 - 31 = tag

a. What is the size of each cache line?
b. How many cache lines are present in each cache?
c. What is the size of each cache?
d. How much space is required to store the tags for the L1 instruction cache?

It these caches have the following interesting properties:

- all data loads are to distinct, often random, memory locations
- there are no forward branches.
- branch targets are never more than 5 instructions back.

e. For each of these pairs, identify which is likely to be higher, and why.
   i. Spatial locality of instruction cache references and spatial locality of data cache references.
   ii. Temporal locality of instruction cache references and spatial locality of instruction cache references.

f. For each of the following, identify whether it might increase or decrease (or it's impossible to tell) the hit rate for the instruction cache and data cache.
   i. Increase the offset to bits 0-9, decrease the index to 10-14.
   ii. Decrease the offset to bit 0, shift the index to bits 1-11, and increase the tag to bits 12-31.