Course Name:	Advanced Computer Architecture	Course Code:	EE502
Program:	MS(Computer Science)	Semester:	Fall 2020
		Total Marks:	30
Due Date:	21-12-2020	Weight	~3
Evaluation Type:	Assignment 5	Page(s):	3

Question 1 [10]

Suppose we have following two configurations
a. 32-bit operating system, 4-KB page size, 1 GB of RAM
b. 64-bit operating system, 16-KB page size, 16 GB of RAM

1. How many bits are required for each of the following entries: P stands for Physical and V stands for Virtual

Config.	V. Addr bits	P. Addr bits	V. Page no. bits (index in V. addr)	P. Page no. bits (index in P. addr)	Offset
a					
b					

2. What are some advantages and disadvantages of using a larger page size?

Question 2 [20]

Consider a memory sub-system—with 16-bit addresses—that has two levels of cache (L1 and L2). L1 is a direct-mapped cache with 16 bytes block size and cache capacity of 4 KB. L2 is an 8-way set associative cache with 256 bytes block size and cache capacity of 32 KB.

a. Calculate the size of tag, index, and offset fields for the L1 cache (3 marks)

Number of tag bits	
Number of index bits	
Number of offset bits	

b. Calculate the size of tag, index, and offset fields for the L2 cache (3 marks)

Number of tag bits	
Number of index bits	
Number of offset bits	

c. A test application attempts to read the following 16-bit memory addresses (in right column). List all generated events that might take place for each read access. Possible events include L1-Hit, L1-Miss, L2-Hit, L2-Miss, and Mem (for memory read). (10 marks)

Note that memory blocks are only transferred between adjacent memory levels. This means that when data is read from memory, the block containing it will be moved into L2 only. L1

Memory Address (to read from)	Generated Events (L1-Hit, L1-Miss, L2-Hit, L2-Miss, and Mem)
0x1562	
0x1588	
0x1581	
0x1562	

will be populated when relevant data is found in the L2 cache. Least Recently Used (LRU) replacement policy is used where required. The caches are initially empty.

The following cases (see below) generate the following events (see below). Use this information to fill the table in the right-box.

Cases	Generated Events
L1-Hit	L1-Hit
L2-Hit	L1-Miss, L2-Hit
Memory Access	L1-Miss, L2-Miss, Mem

0x4562	
0x45BC	
0x4562	
0x1562	
0x45BC	
0x45B2	

d. Assume that the:
Clock rate is 1 GHz,
L1 access time is 2 cycle,
L2 access time is 15 cycles,
Memory access time is 200 cycles,
L1 hit rate is 80%,
L2 hit rate is 90%.

What is the average memory access time? (4 marks)

d. solution