Computer Architecture (CS-E) Quiz1
Date: 11-09-2018
Roll No: _____

Question: Following are the initial values of all register components of the following circuit

r0: 0000 0000 0000 0000, r1: 1111 1111 1111 1111,r2: 1010 1010 1010 1010,r3: 1100 1100 1100 1100

The input signal on the next clock cycle is as follows

DA: 010 Load:0 Clk:0 D: 0010 0010 0010 0010 AA: 011 BB:010

What will be contents of the registers, output A and Output B after this signal?

r1:	r2:
r3:	r4:
A:	B:

AA[2..0] INPUT VCC
BA[2..0] INPUT VCC
D[15..0] INPUT VCC
CLK INPUT VCC
Load INPUT GND
DA[2] INPUT VCC
DA[1] INPUT VCC
DA[0] INPUT VCC
VCC

octal_decoder
A2 X0
A1 X1
A0 X2
E   X3
    X4
    X5
    X6
    X7
decd

AND2 load0
AND2 load1
AND2 load2
AND2 load3

register_parallel_load
D[15..0] Q[15..0]
Load
CLK
r0

register_parallel_load
D[15..0] Q[15..0]
Load
CLK
r1

register_parallel_load
D[15..0] Q[15..0]
Load
CLK
r2

register_parallel_load
D[15..0] Q[15..0]
Load
CLK
r3

multiplexer_8_1
A0[WIDTH-1..0]   X[WIDTH-1..0] OUTPUT A
A1[WIDTH-1..0]
A2[WIDTH-1..0]
A3[WIDTH-1..0]
A4[WIDTH-1..0]
A5[WIDTH-1..0]
A6[WIDTH-1..0]
A7[WIDTH-1..0]
S[2..0]
muxa

multiplexer_8_1
A0[WIDTH-1..0]   X[WIDTH-1..0] OUTPUT B
A1[WIDTH-1..0]
A2[WIDTH-1..0]
A3[WIDTH-1..0]
A4[WIDTH-1..0]
A5[WIDTH-1..0]
A6[WIDTH-1..0]
A7[WIDTH-1..0]
S[2..0]
muxb