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Question 1 [12]

Suppose we have separate 4 way set-associative L1 instruction and data caches that both have the following division of 32-bit address:
bits 0 - 3 = offset, bits 4 - 14 = index, bits 15 - 31 = tag

a. **What is the size of each cache block?**

b. **How many sets are present in each cache?**

c. **What is the size of each cache (data bits)?**

d. **How much space is required to store the tags for the L1 instruction cache (size of tag array)?**

It these caches have the following interesting properties:

- **all data loads are to distinct, often random, memory locations**
- **there are no forward branches.**
- **branch targets are never more than 5 instructions back.**

e. **For each of these pairs, identify which is likely to be higher, and why.**
   i. **Spatial locality of instruction cache references and spatial locality of data cache references.**

   ii. **Temporal locality of instruction cache references and spatial locality of instruction cache references**

Question 2 [8]

Each instruction fetch means a reference to the instruction cache and 25% of all instructions reference data memory (Load/Store instructions).
With the first implementation (separate instruction and data cache):
- The average miss rate in the L1 instruction cache was 3%
- The average miss rate in the L1 data cache was 8%
- In both cases, the miss penalty (time to access main memory) is 200 CCs
For the new design, with unified memory (same cache for instruction and data), the average miss rate is 5% for the cache as a whole, and the miss penalty is again 200 CCs.

a) **Which design is better and by how much?**

b) **If we add L2 cache in the new design with access time equal to 20cc, it reduces the miss rate to 2.5 % from 5 %. What will be the new average memory access time?**