National University of Computer and Emerging Sciences, Lahore Campus

Course Name:	Computer Architecture	Course Code:	EE204
Program:	BS(Computer Science)	Semester:	Fall 2018
Duration:	30 Minutes	Total Marks:	20
Paper Date:	13-11-2018	Weight	~3
Exam Type:	Quiz 3c	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1a [5]

What is the difference between execution hazard and memory hazard?

Question 2 [10 + 3 +2]

Consider the following program fragment executing on a basic 5-stage MIPS pipeline **with no data forwarding**. All stages take 1 cycle, except the Execute stage, which takes a variable number of cycles, depending on the functional unit used:

Functional unit	Number of EX cycles
Integer ALU	2
Floating Point Add	3
Floating Point Load/Store	2
Floating Point Multiply	4

a. For each instruction, determine in which clock cycle the instruction is safely completed after inserting stalls. **F** at the end of instruction op-code denotes floating point instruction e.g. MULT**F**. **Assume no data forwarding occurs**. **Ignore Structural hazards while scheduling.**

Instruction
1: MULTF F1, F2, F3
2: ADD R1, R1, R2
3: LF F5, 0(R1)
4: SUBF F5, F6, F1
5: SF F5, 0(R1)
6: MULTF F5, F3, F4

Show timing in the table below:

Cycle / Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
(1)	F	D																												
(2)																														
(3)																														
(4)																														
(5)																														
(6)																														

b. Calculate the average CPI and throughput (in instructions per cycle) of the processor for the above code.

c. If we run this program on a processor with frequency of 1 MHZ, what would be its execution time?