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Student : Name:_____ Roll No._____ Section:_____

Question 1 [6]

Suppose you have 128MB cache with 32 byte line sizes, assume a 32-bit address:

A. How many total bits of storage(tag+data+valid) are required for a direct mapped cache:

_____

Provide details:

B. How many total bits of storage(tag+data +valid) are required for a 4-way set associate cache:

_____

Provide details:

Question 2 [14]

1. **Loop: ld R4, 0(R3)**
2. **div R4, R4, R2**
3. **ld R5, 100(R3)**
4. **mul R6, R4, R5**
5. **sw R6, 0(R3)**
6. **sub R3, R3, 4**
7. **bne R3, 0, Loop**

Consider the following specification for our pipelined processor:
Five stages MIPS pipeline where multiplication and division consumes 3 cycles in execution. All other instructions consumes 1 cycle in each stage. Branch calculation is done in decode stage.
Full Forwarding has been implemented.

a) Add stalls in the above code to avoid data and control hazards	**b) Rearrange the code to remove stalls**

c) Perform 2-level un-roll and reschedule the code to remove as many stalls as possible

Unrolled code	**Rescheduled unrolled code**