Computer Architecture – Fall 2020

Assignment # 2

Due Date: *11/10/2020*
Time: *5 pm*

You may be called for evaluation of this assignment and you will have to justify your solutions before the course instructors and the TA. Failure to justify your answers will result in negative marks. Severity of the plagiarism can result in F as well.

Answer your questions in this file and submt your final solution as PDF file only.

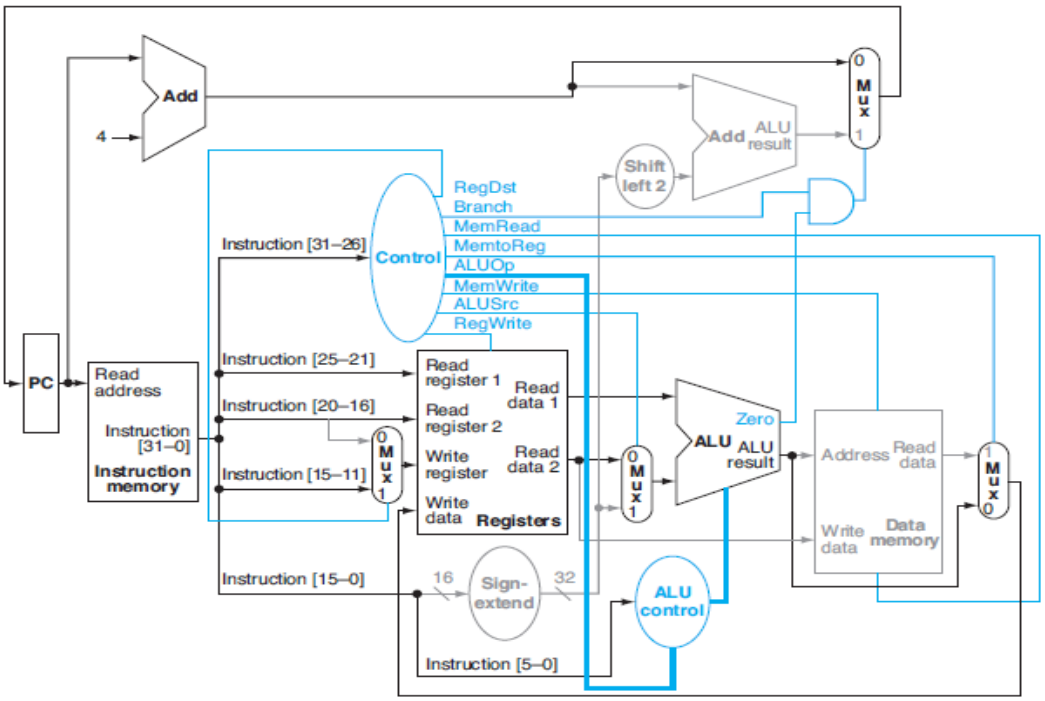
Q1: Design the internal circuit of a ***Register file*** which contains 4 registers only. Each register can contain 4 bits. No need to design internal circuit of the register. You can assume that the registers are provided.

Following are the inputs to the register file

1. 2-bit Register number to read data
2. 2-bit Register number to read data
3. 2-bit Register number to write data to
4. 4-bit data to be written

Insert your circuit diagram here.

Following datapath for a Single Cycle processor design should be used to answer Q2-Q4.



Q2: Following statement has to be added to the datapath

SEQ Rd,Rs,Rt

Interpretation: Reg[Rd] = Boolean value (0 or 1) of (Reg[Rs] == Reg[Rs]) Value of Register Rd will be either zero or one after the instruction execution. If the contents of Register Rs and Rt are equal, the Rd will have 1, otherwise Rd should be set to 0.

1. Which existing blocks (if any) can be used for this instruction?
   Answer:

2. Which new functional blocks (if any) do we need for this instruction?
   Answer:

3. What new signals do we need (if any) from the control unit to support this instruction?
4. Answer:

5. Show the updated datapath that can execute this instruction. Modify the datapath shown above and highlight the changes that you made to add this new instruction to the existing datapath.

   Insert your updated path here

Q3: The processor fetches the following instruction word

10001100011000100000000000010100

Following are the register values when the instruction is fetched

R0	R1	R2	R3	R4	R5	R6	R8	R12	R31
0	-1	2	-2	-8	10	6	8	2	-16

1. Which instruction does this binary word describe?
2. Answer:

3. What are the outputs of the sign-extend and the jump "Shift left 2" unit for this instruction word?
   Answer:

4. What are the values of the ALU control unit's inputs for this instruction?
   Answer:

5. What is the new PC address after this instruction is executed? Assume that the PC had some arbitrary value x.
   Answer:

6. For each Mux, show the values of its data output during the execution of this instruction and these register values.
   Answer:

7. For the ALU and the two add units, what are their data input values?
   Answer:

8. What are the values of all inputs for the "Register file" unit?
   Answer:

9. What are the registers values after the instruction execution? Assume that the memory has been initialized with all 0s.

R0	R1	R2	R3	R4	R5	R6	R8	R12	R31

Q4: Consider the following latencies for pipeline stages

IF	ID	EXE	MEM	WB
300ps	200ps	150ps	300ps	200ps

1. What is the clock cycle time for the pipelined processor?
   Answer:
   Briefly explain how you computed this value

2. What is the clock cycle time for a non-pipelined processor?
   Answer:
   Briefly explain how you computed this value

3. What is the total latency of an LW instruction in the pipelined processor?
   Answer:
   Briefly explain how you computed this value

4. What is the total latency of an LW instruction in the non-pipelined processor?
   Answer:
   Briefly explain how you computed this value