	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Spring 2019
	Duration:	30 Minutes	Total Marks:	20
	Paper Date:	08-04-2019	Weight	~3
	Exam Type:	Quiz 3a	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1a [6]

What is the difference between superscalar and VLIW processor? How in ideal case we can achieve 4 times improvement in both designs?

Question 1b [4]

What is the difference between static and dynamic branch prediction?

Question 2 [10]

Consider the following MIPS assembly language code. Assume that we run this code on the five stages pipelined data path. Multiplication consumes 2 cycles in execution.

1. **Loop: ld R4, 0(R3)**
2. **ld R5, 100(R3)**
3. **mul R6, R6, R5**
4. **sw R6, 0(R3)**
5. **add R4, R4, 10**
6. **sub R3, R3, 4**
7. **bne R3, 0, Loop**

a) Add stalls in the above code to remove all data and control hazards. Assume full forwarding (Exe to Exe, Mem to Exe, Exe to Dec, Mem to Mem) is implemented.

b) Rearrange the code to remove as many stalls as possible.