	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2019
	Duration:	30 Minutes	Total Marks:	20
	Paper Date:	04-12-2019	Weight	~3
	Exam Type:	Quiz 5b	Page(s):	2

Student : Name:_____ Roll No._____
Section:_____

Question 1 [2+2+2+2]

Consider the following facts for the page table and answer the questions below.

   a) Each page table entry consists of a physical page number, 1 valid bit, 1 dirty bit
   b) Virtual addresses are 24 bits - Physical addresses are 16 bits - The page size is 4 Kbytes

1. How many virtual pages will be there?

2. How many physical pages will be present?

3. What is the size of the page table if we store information of all pages?

4. What is the size of the page table if we only store information of physical pages?

Question 2 [3+3+3+3]

Consider a machine with a byte addressable main memory of 64 KB and block size of 4 bytes. Assume that a 4-way set associate cache of 512 bytes is used with this machine.

a. How the main memory address will be divided into tag, index and offset bits?

b. Into what set would bytes with each of the following addresses be stored?

Set no. (in decimal)

0001 1001 1011 1011
1101 0000 1010 1101

c. Suppose the byte with address 0001 1010 0001 1011 is stored in the cache. What are the addresses of the other bytes stored along with it in the same block?

d. What would be the size of tag array?