	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2018
	Duration:	30 Minutes	Total Marks:	20
	Paper Date:	23-10-2018	Weight	~3
	Exam Type:	Quiz 2c	Page(s):	2

Student : Name:_____ Roll No._____
Section:_____

Question 1a [15]

Consider the following MIPS assembly language loop. Assume that we run this code on the five stages pipelined data path.

```
Instruction 1:    Lw r1, r2,0
Instruction 2:    Lw r2, r2,20
Instruction 3:    Add r3,r1,r2
Instruction 4:    Lw r4,r1, 30
Instruction 5:    Lw r5,r4,40
Instruction 6:    St  r4, r3,15
Instruction 7:    Add r6,r6,r7
```

a) Find all possible hazards in the above code. Fill the following table by writing lines and register in front of particular hazard. For example if a **WAR** hazard exist between instruction 1 and 2 due to register R0 then write **1 & 2** in column "Lines" and Register number **R0** in column "Register".

Without Forwarding			With Forwarding		
Hazard	**Lines**	**Register**	**Hazard**	**Lines**	**Register**
WAR					
WAW					
RAW					

b) Add stalls in the above code to remove all hazards

Without Forwarding	With Forwarding

c) Reschedule the code to remove as many stalls as possible with forwarding. How many stalls are still required?

Question 2 [5]

Assume that registers r1, r2, r3 and r4 contain the values 10, 20, 30, 40 respectively. Moreover memory contains the following values at mentioned addresses

Address	Value
40	150
44	250
48	350
52	450
56	550

Write the value of r3 and r2 after execution of each line of following code. No forwarding is implemented

Add r3, r3, - 20
Add r3, r3, r1
Load r2, r3, 28