


# National University of Computer and Emerging Sciences, Lahore Campus

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**Student : Name:** \_\_\_\_\_ **Roll No.** \_\_\_\_\_  
**Section:** \_\_\_\_\_

## Question 1a [15]

Consider the following MIPS assembly language loop. Assume that we run this code on the five stages pipelined data path.

```

Instruction  Lw r1, r3,0
1:
Instruction  Lw r3, r3,40
2:
Instruction  Sub r2,r1,r3
3:
Instruction  Lw r4,r1, 30
4:
Instruction  Lw r6,r4,100
5:
Instruction  St  r4, r2,15
6:
Instruction  OR r5,r5,r7
7:

```

- a) Find all possible hazards in the above code. Fill the following table by writing lines and register in front of particular hazard. For example if a **WAR** hazard exist between instruction 1 and 2 due to register R0 then write **1 & 2** in column “Lines” and Register number **R0** in column “Register”.

Without Forwarding			With Forwarding		
Hazard	Lines	Register	Hazard	Lines	Register
WAR					
WAW					
RAW					

- b) Add stalls in the above code to remove all hazards

Without Forwarding	With Forwarding

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- c) Reschedule the code to remove as many stalls as possible with forwarding. How many stalls are still required?

## Question 2 [5]

Assume that registers r1, r2, r3 and r4 contain the values 20, 30, 40, 50 respectively. Moreover memory contains the following values at mentioned addresses

Address	Value
40	150
44	250
48	350
52	450
56	550

Write the value of r3 and r2 after execution of each line of following code. No forwarding is implemented

**Add r3, r3, - 20**

**Add r3, r3, r1**

**Load r2, r3, 8**