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Student : Name:_____ Roll No._____
Section:_____

Question 1a [4]

In Pipelined processor, multiple instructions are in different pipelined stages at the same time. In each clock cycle, new control signals are created by instruction at decode stage, however instructions at other stages require their own signals. How this problem is handled in Multi-cylce MIPS pipeline?

Question 1b [6]

We have a program with execution time of 20 seconds on computer A. The clock speed of computer A is 500 MHz. Another computer B runs the same program in 15 seconds. We only know that clock cycles required in Computer B are double as compared to Computer A. Calculate the clock rate of Computer B.

Question 2 [3+4+3]

a) If we have the following times for 4-staged Pipelined MIPS architecture: 20ns, 10ns, , 30ns, and 15ns then what would be the frequency of the processor and latency of a single instruction.

b) If we have the liberty to convert it into 5-staged pipeline by splitting any one stage into two equal stages then which stage should be split and what would be the new frequency and latency of a single instruction.

c) Calculate the speedup we obtain by using 5-staged pipeline.