	Course Name:	Computer Architecture	Course Code:	EE204
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	Paper Date:	27-11-2019	Weight	~3
	Exam Type:	Quiz 4c	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1a [4]

What types of caches suffer from conflict miss and which one suffer from capacity miss among direct-mapped, set associative and fully associative cache? Provide reasoning!

4 marks

Question 1b [4]

If a loop originally iterates 500 times and we want to use 3-level loop unrolling then how will we manage 500 iterations? How many times the new loop iterates?

Question 2 [2+2+2+2+2+2]

Assuming a cache of 512 blocks, a 16-bytes block size, and a 20-bit memory address.

1. **The total number of sets for a direct-map cache: _____**

2. **The total number of sets for an 8-way set associate cache: _____**

3. **How many total bits of storage(tag+data +valid) are required for a direct mapped cache: _____**

4. **How many total bits of storage(tag+data +valid) are required for an 8-way set associate cache: _____**

5. **How many total bits of storage(tag+data +valid) are required for a fully associative cache: _____**

6. **In case of a 4-way set associate cache, Into what set would bytes with each of the following addresses be stored**

   Set number (decimal)

   - **0001 0001 0001 1011 1111**

- **1100 1111 0011 0011 0100**