


National University of Computer and Emerging Sciences, Lahore Campus

	Course Name:	Computer Architecture	Course Code:	EE204
	Program:	BS(Computer Science)	Semester:	Fall 2019
	Duration:	30 Minutes	Total Marks:	20
	Paper Date:	08-10-2019	Weight	~3
	Exam Type:	Quiz 2b	Page(s):	2

Student : Name: _____ **Roll No.** _____
Section: _____

Question 1 [5+5]

a) What is the effect of Pipelining on Frequency and latency of a single instruction? Tell for each one of them either it increases or decreases? Briefly describe the reason behind it.

b) A program of 2000 instructions executes in 10 milliseconds on a computer with 500 KHz clock. Calculate the average CPI?

Question 2 [10]

An unpipelined processor takes 10 ns to work on one instruction. It then takes 0.2 ns to latch its results into latches. We were able to convert the circuits into 8 pipeline stages. The stages have the following lengths: 1.3ns; 0.9ns; 0.8ns; 1.2ns; 1.6ns; 0.4ns; 1.5ns; 1.3ns. Answer the following, assuming that there are no stalls in the pipeline.

1. What are the clock speeds in both processors?
2. How long does it take to finish a single instruction in both processors (in nano-seconds and cycles)?
3. What is the throughput for each processor?
4. What is the speedup provided by the 8-stage pipeline?