	Course Name:	Computer Architecture	Course Code:	EE204
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	Exam Type:	Midterm	Page(s):	4

Student : Name:_____ Roll No._____ Section: _____

Instruction:
1. Attempt all question in the provided space. You can use rough sheets but it should not be attached.
2. If you think some information is missing, write assumption and solve accordingly.

Question 1a [6] (Multiple options can be selected in each question)

1. Which of the following statements regarding pipeline hazards are TRUE?
   A. all data hazards can be avoided by forwarding
   B. branching causes both data and control hazards
   C. data hazards may cause error in execution result
   D. structural hazards occur whenever an instruction depends on another for operand
2. Typically during pipelined execution, the read operation on the register file and the memory is performed during _____
   A. first half of the cycle
   B. later half of the cycle
   C. any half of the cycle
   D. throughout the cycle
3. CPU time can be reduced by reducing:
   E. Instruction count
   F. clocks per instruction
   G. clock cycle time
   H. clock frequency
4. Structural hazards can be avoided by
   A. adding stalls
   B. forwarding
   C. adding more hardware
   D. register renaming
5. We can flush an instruction by
   A. disabling IF/ID register
   B. disabling PC register
   C. flushing IF/ID register
   D. flushing PC register
6. Allowing jumps branches, and ALU instructions to take fewer stages/cycles than the five required by the load instruction will
   A. increase pipeline performance
   B. decrease pipeline performance
   C. increase clock cycle time
   D. decrease clock cycle time

Question 1b [4]

Consider three branch prediction schemes:

A: predict not taken

B: predict taken

C: dynamic prediction.

Assume that they all have zero penalty when they predict correctly and two cycles when they are wrong. Assume that the **average predict accuracy of the dynamic predictor is 65%**. Which predictor is the best choice for the following branches? Write A, B, or C in last column representing the best choice.

	Actual Branch outcome	Additional cycles(penalty) for each option			Best choice
		A	B	C	
1	Branch taken with 15% frequency				
3	Branch taken with 70% frequency				

Question 2 [12]

Consider the following instruction sequence:

```
Loop: lw R1,20(R2)
      add R1,R1,R3
      sub R6,R1,R5
      sw R6, 20(R2)
      beq R6,R7,Loop
```

Assume that the following code is being run on 5-stage mips processor with each stage consuming one clock cycle and the branch is always predicted to be taken.

1. If there is no forwarding and hazard detection, how many cycles will be required to complete execution of this code if values of the registers and memory are such that the loop takes only 2 iterations?
   Required Cycles: _____
   Explain your answer by rewriting the code and inserting NOPs in the code where the stalls are required.

2. Now consider that full forwarding and hazard detection unit is implemented, how many cycles will be required to complete execution of this code if values of the registers and memory are such that the loop takes only 2 iterations?
   Required Cycles: _____
   Explain your answer by inserting NOPs in the code where the stalls are required

3. Consider the following initial values for the registers

Register Name -->	R1	R2	R3	R4	R5	R6	R7
Register Value -->	0	0	10	0	5	0	6

All the Data memory locations are initialized to 1.

a. Suppose we designed the hazard detection unit and assumed that forwarding will be implemented, but then we forget to actually implement forwarding, what are the final register values after the above code sequence executes (single iteration)?

Register Name -->	R1	R2	R3	R4	R5	R6	R7
Register Value -->							

b. If the processor has forwarding, but we forgot to implement the hazard detection unit, what are the final register values after the above code sequence executes (single iteration)?

Register Name -->	R1	R2	R3	R4	R5	R6	R7
Register Value -->							

Explanation:

Question 3 [8]

CPI of different instruction types is given as below

Arithmetic	Load/Store	Branch
2	5	3

Assume the following instruction breakdown for a given program

	No. of instructions
Arithmatic	500×10^6
Load/Store	300×10^6
Branch	200×10^6

a. **What is the execution time for the processor if the clock rate is 5 GHz**

b. **Suppose new, more powerful arithmetic instructions are added to the instruction set. So the number of arithmetic instructions in our program are reduced by 25% but clock cycle time is increased by 10%. Find the performance of this design and tell whether it is better than original one or not?**