National University of Computer and Emerging Sciences, Lahore Campus

	Course:	Advance Computer Architecture	Course Code:	EE502
	Program:	MS(Computer Science)	Semester:	Spring 2017
	Submission Date:	13-02-2017	Total Marks:	100
	Section:	A	Weight	3.3
	Exam:	Assignment 1	Page(s):	2

Note: Submit in hard form

Q1: Choose a latest mobile processor (2014 onwards) and provide details of its architecture, techniques being used to enhance its performance and strategies being employed to cater different problems. **Marks 50**

You should provide complete details of at-least the following features:

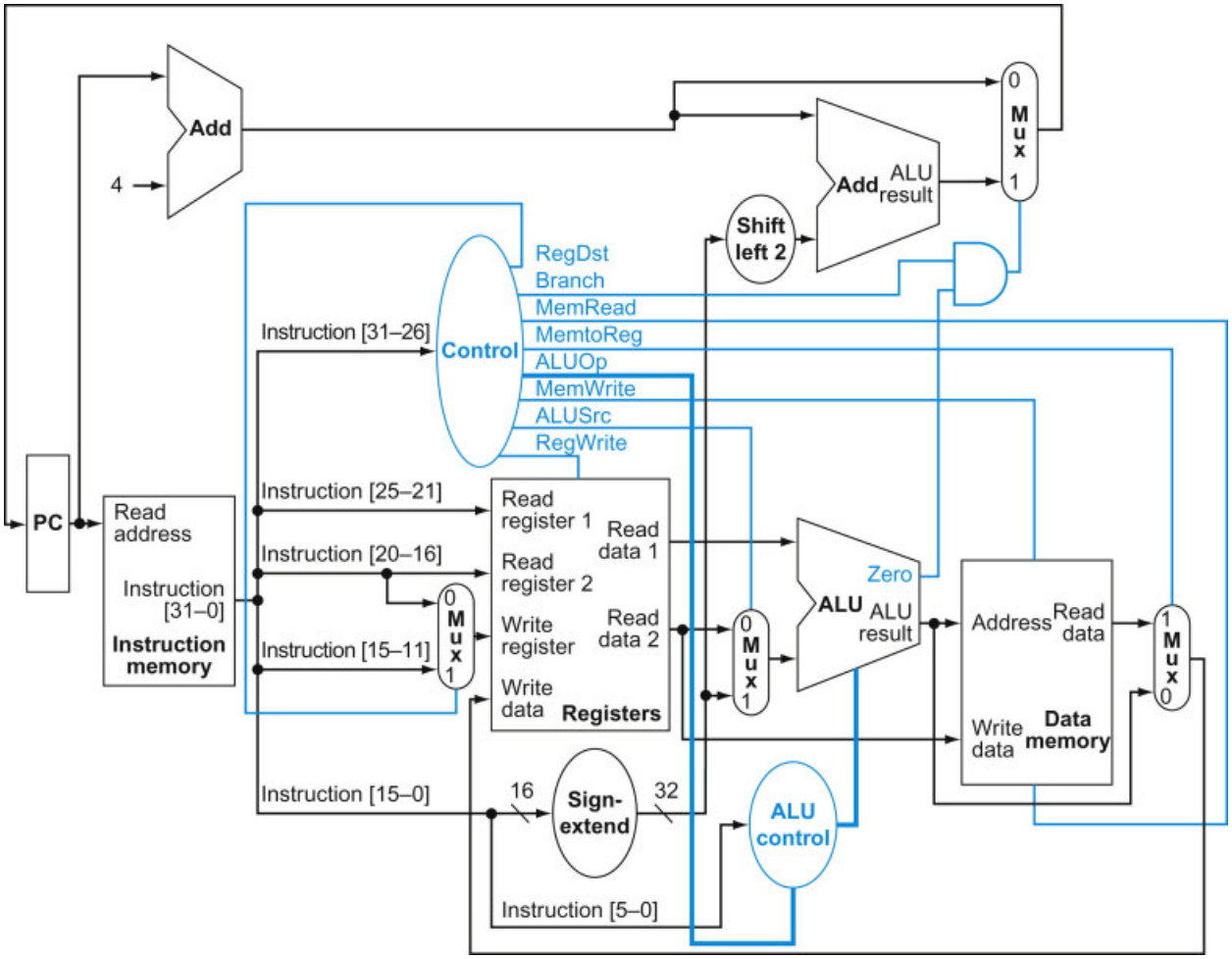
- Type of Instruction Set Architecture
- Micro-architecture Diagram
- Network on chip details
- No. of pipelining stages, clock cycle time, clock speed
- Multiprocessing
- Support for multithreading and different types of multithreading being supported
- Turbo boost
- Types and hierarchy of caches being used

Your answer should contain a section named **critical thinking** in which you will do a comparison of this processor with previous or current processors and provide reasoning that which architecture is better in particular functionalities, what are the reasons and what is the extra cost that we have to incur to get those functionalities. And what you think could be changed or modified in the architecture to make it better and more useful. **Also provide references of the information you include in your answer.**

Q2: Following are 3 instructions in hexadecimal format for a single-cycle MIPS data path shown on next page. **Marks 30**

1. **0x AE2A0028**
2. **0x 01288020**
3. **0x 1573FFFC**

Decode these instructions and provide details like instruction type, micro-operation being performed and control signals being generated for each instruction.
For this question refer to the 4th chapter of the book Computer organization and design by David Patterson 4th edition. The purpose of this question is to revise MIPS architecture and know its working.



Q3: Processor X has a clock speed of 1 GHz, and takes 1 cycle for integer operations, 2 cycles for memory operations, and 4 cycles for floating point operations. Empirical data shows that programs run on Processor X typically are composed of 35% floating point operations, 30% memory operations, and 35% integer operations. You are designing Processor Y, an improvement on Processor X which will run the same programs and you have 2 options to improve the performance:

1. Increase the clock speed to 1.2 GHz, but memory operations take 3 cycles
2. Decrease the clock speed to 900 MHz, but floating point operations only take 3 cycles

Compute the speedup for both options and decide the option Processor Y should take.

Marks 20