Course Name:	Computer Architecture	Course Code:	EE204
Program:	BS(Computer Science)	Semester:	Fall 2019
Duration:	30 Minutes	Total Marks:	20
Paper Date:	04-12-2019	Weight	~3
Exam Type:	Quiz 5d	Page(s):	2

Student : Name:_____ Roll No._____ Section:_____

Question 1 [2+2+4]

Assume for specific system the:

Clock rate is 4 GHz, Base CPI is 2
L1 access time is 2 cycle, L2 access time is 20 cycles, Memory access time is 200 cycles,
L1 hit rate is 80%, L2 hit rate is 70%.
Memory Accesses Per Instruction = 70%

1. **What is the average memory access time?**

2. **What is the global miss rate?**

3. **What is the effective execution time for a program with 1000 instructions?**

Question 2 [3+3+2+2+2]

Consider a memory sub-system—with 16-bit addresses—that has two levels of cache (L1 and L2). L1 is a direct-mapped cache with 8 bytes block size and cache capacity of 2 KB. L2 is an 4-way set associative cache with 16 bytes block size and cache capacity of 4 KB.

a. Calculate the size of tag, index, and offset fields for the L1 cache	**Number of tag bits**	
	Number of index bits	
	Number of offset bits	
b. Calculate the size of tag, index, and offset fields for the L2 cache	**Number of tag bits**	
	Number of index bits	
	Number of offset bits	
c. Suppose the byte with address 0001 1010 0001 1011 is stored in L1 cache. What are the addresses of the other bytes stored along with it in the same block?		
d. Calculate the size of tag array for L1 cache!		
e. Calculate the total bits of storage required for L2 cache!		