


National University of Computer and Emerging Sciences, Lahore Campus

	Course Name:	Computer Architecture	Course Code:	EE204
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	Exam Type:	Assignment 4	Page(s):	3

Student : Name: _____ **Roll No.** _____
Section: _____

Question 1 [10]

We have studied about static and dynamic branch prediction. Consider the following branch prediction schemes:

A: predict not taken (static)

B: predict taken (static)

C: dynamic prediction

Assume that they all have zero penalty when they predict correctly and three cycles penalty for each wrong prediction. Assume that the **average predict accuracy of the dynamic predictor is 70%**. Which predictor is the best choice for the following branches? Write A, B, or C in last column representing the best choice.

	Actual Branch outcome	Additional cycles(penalty) for each option			Best choice
		A	B	C	
1	Branch taken with 20% frequency				
3	Branch taken with 60% frequency				

Question 3 [4+4+6+6]

Consider the following instruction sequence:

Loop: lw R1,20(R2)

add R4,R1,R3

sub R6,R1,R4

sw R6, 20(R2)

add R2, R2, 4

beq R6,R7,Loop

Assume that the following code is being run on 5-stage mips processor with each stage consuming one clock cycle

1. If there is no forwarding, how many cycles will be required to complete execution of this code including stalls if values of the registers and memory are such that the loop takes only 2 iterations?

Required Cycles: _____

Explain your answer by rewriting the code and inserting NOPs in the code where the stalls are required.

2. Now consider that full forwarding and hazard detection unit is implemented, how many cycles will be required to complete execution of this code if values of the registers and memory are such that the loop takes only 2 iterations?

Required Cycles: _____

Explain your answer by inserting NOPs in the code where the stalls are required

3. Consider the following initial values for the registers

Register Name -->	R1	R2	R3	R4	R5	R6	R7
Register Value -->	10	4	5	0	10	0	6

All the Data memory locations are initialized to 1.

- a. Suppose we designed the hazard detection unit and assumed that forwarding will be implemented, but then we forget to actually implement forwarding, what are the final register values after the above code sequence executes (single iteration)?

Register Name -->	R1	R2	R3	R4	R5	R6	R7
Register Value -->							

- b. If the processor has forwarding, but we forgot to implement the hazard detection unit, what are the final register values after the above code sequence executes (single iteration)?

Register Name -->	R1	R2	R3	R4	R5	R6	R7
Register Value -->							

Explanation:

