Mansoura University

Faculty of Engineering

Department of Computer Engineering and Systems

Logic and digital design 2 (CSE3213)

ASM CHART APP.

Up/down counter and applications

Abstract

Applying what we had in the course, this report aims to discuss what is the project, how it is done and the tools we used

SEC 2

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Introduction

This project aims to apply a simple digital system from its ASM chart. this project is a sample of a system that tends to count the number of people entering and leaving a room or can be used as a security system for vital places or at workplaces.
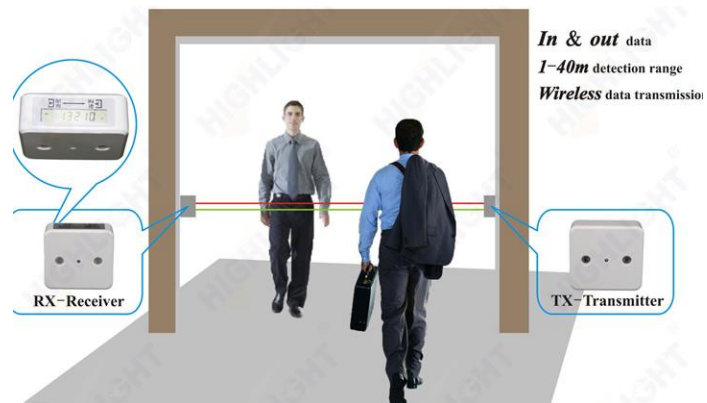

Figure 1 - Infrared people counter at workplace

1 Analyzing ASM chart

To count the people entering and leaving we need sensors to detect and a counter IC which consists of multiple Flip Flops to save the data, the sensors here are going to be our variables (inputs to the system), and an output screen.

1.1 Variables

One sensor which will be replaced with a button to count up for the counter.
another one to count down.

1.2 UpDown counter

We will use74LS191 to count up and down, save and show the output in the binary system.

1.3 Control unit

We will use some ORs, XORs, ANDs, and NOTs to control the system.

2 Control design

By analyzing 74LS191 datasheet we figured the inputs depending on the truth table

Table 1 - 74LS191 Modes

MODE SELECT TABLE

INPUTS				MODE
PL	CE	U/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			RC OUTPUT
CE	TC*	CP	
L	H	⊔⌐	⊔⌐
H	X	X	H
X	L	X	H

* TC is generated internally

If X is count up button and Y is count down button and we apply the deduced truth table to meet our desires:

PL → pin 11 → always high → 5v

CE → pin 4 → (X xor Y)'

U/D → pin 5 → X'Y

CP → clock pulse generated from 555 ic / button

Table 2 - Deduced truth table

X	Y	CE	U/D
0	0	1	0
0	1	0	1
1	0	0	0
1	1	1	0

3 Tools

Buttons / IR sensors

XOR 7486

NOT 74ls04

AND 74ls08

555

D flip flop 74ls175

Up/down counter **74ls191** / 74ls192

BCD to 7 seg. 74ls47

7 seg display

Regulator 7805

Figure 2 – IC AND / NOT / XOR / D flip flop
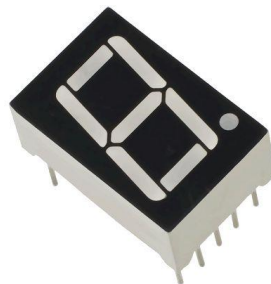
Figure 5 - Regulator

Figure 4 - 555 IC

Figure 3 - 7 segment display

4 Schematic Design

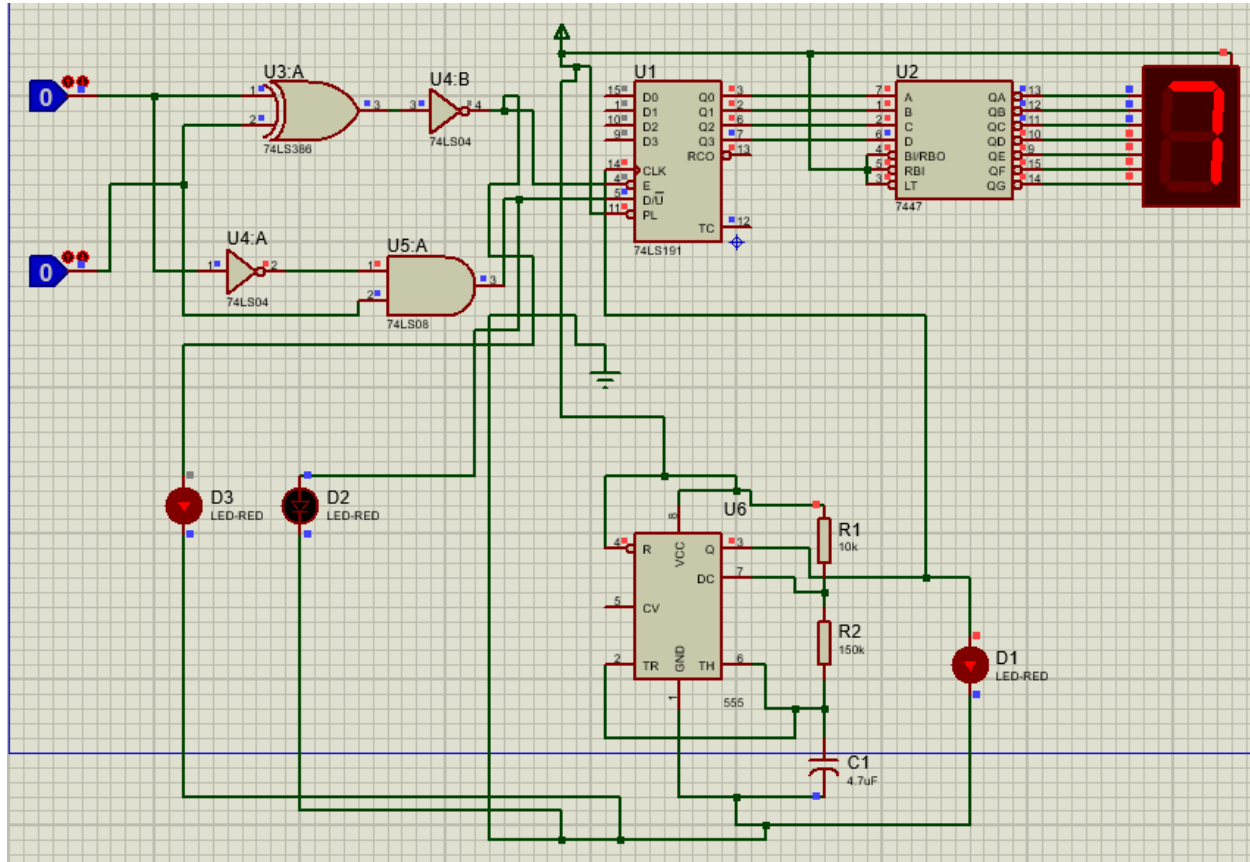We used PROTEUS design suit to simulate our idea and make sure it works correctly
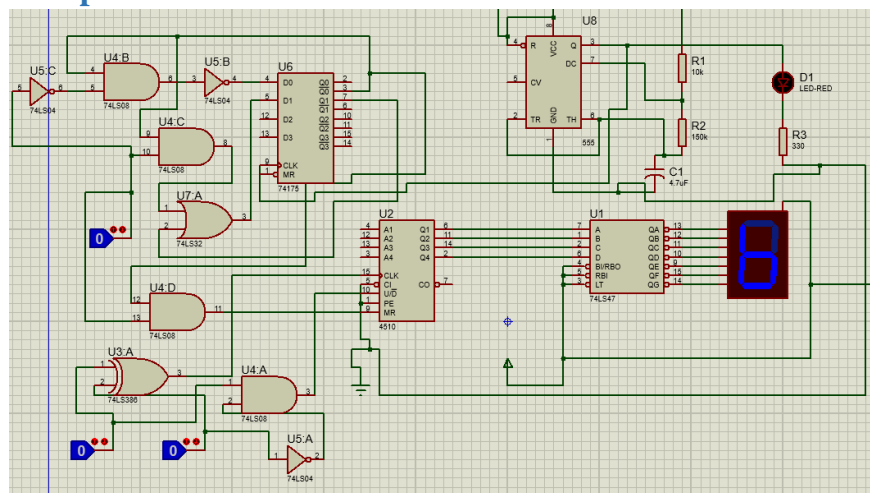

Figure 6 - PROTEUS simulation

4.1 Other attempts:

Figure 7 - other attempt using D flip flop