
# Practice Exam
# Design Verification

Module ID : CX-301

**Design Verification**

Instructor : Dr. Abid Rafique

Version 1.0

# Document History

The changes and versions of the document are outlined below:

| Version | State / Changes | Date | Author |
|---|---|---|---|
| **1.0** | Initial Draft | February, 2025 | Dr. Abid Rafique |
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# Table of Contents

## Objectives

By the end of this practice exam, students will be able to:

- verify circuits (basic to medium difficulty level) from a given requirement specification

## Required Files

The required files for this exam can be found on the shared folder at:

```
shared_folder/CX-301-DesignVerification/Exams/Practice-Exam/
```

## Deliverables

Following are the deliverables to be uploaded on the lms:

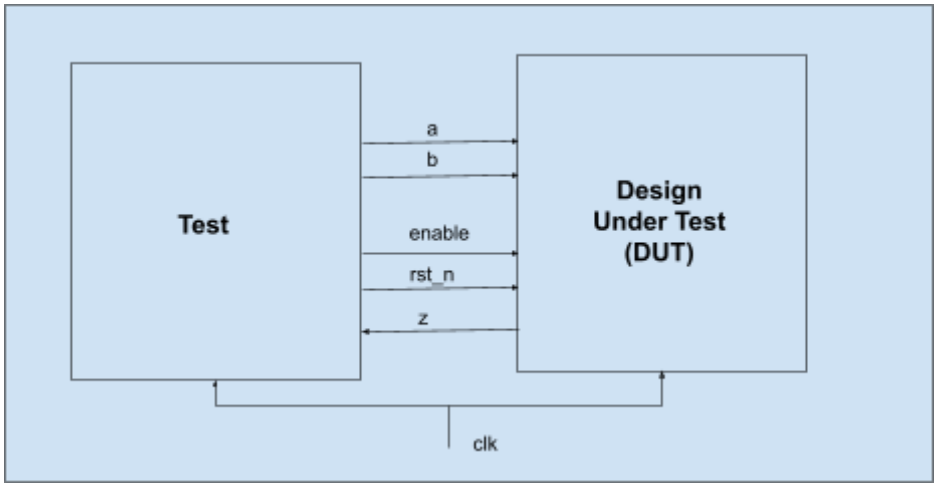
- Verification Plan.
- Testbench

# 1. Micro-Circuits Verification

## Task 1:

Write a testbench to verify a circuit which takes two inputs coming from the sensors **a** and **b.** If both of them are **ON,** the output will be '**1**' otherwise it will be '**0**'**.** The output should be registered using a flip flop with an **enable** signal. The flip flop has an active low **rst_n** as well.

| S.No. | Signal | Number of Bits | Input/Output | Remarks |
|---|---|---|---|---|
| 1. | clk | 1 | Input | |
| 2. | rst_n | 1 | Input | Active Low |
| 3. | enable | 1 | Input | Active High |
| 4. | a | 1 | Input | |
| 5. | b | 1 | Input | |
| 6. | z | 1 | Output | |



You need to perform the following tasks.

1. Write a verification plan (see the example)
2. Write the testbench to test all the test cases mentioned in the verification plan

## Task 2:

Write a testbench to verify a updown-counter circuit.

- If the load signal load = 1, the 8-bit value data_in is loaded into the counter.
- If the load signal is not active and enable signal en = 1:
    - The counter increments if the mode bit m = 0
    - The counter decrements if the mode bit m = 1.
- Active low rst_n signals will reset the count value asynchronously.

| S.No. | Signal | Number of Bits | Input/Output | Remarks |
|---|---|---|---|---|
| 1. | clk | 1 | Input | synchronous to posedge |
| 2. | rst_n | 1 | Input | active low reset |
| 3. | en | 1 | Input | counting enable |
| 4. | m | 1 | Input | counting mode |
| 5. | load | 1 | Input | load data_in |
| 6. | data_in | 8 | Input | the data to be loaded |
| 7. | count | 8 | Output | count value |

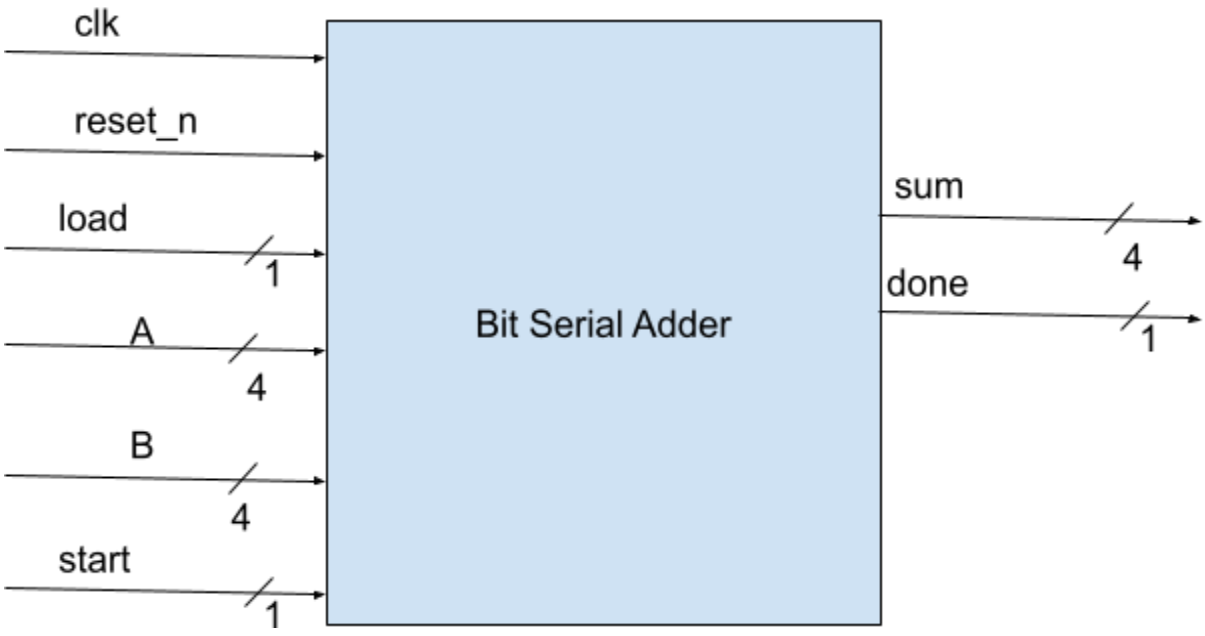
You need to perform the following tasks.

3. Write a verification plan (see the example)
4. Write the testbench to test all the test cases mentioned in the verification plan

# 2. Mini-Circuits Design

Write a testbench to verify a Bit Serial Adder which takes two inputs **'A**' and **'B'** each 4-bit wide and performs addition using a multi-cycle single full-adder using following steps.

- The values will be loaded into the adder when the **load** signal is **'1'.**
- When the **start** signal is '1', the adder starts performing addition
- Once the addition is finished, it generates a **done** signal indicating the result is valid.




You need to perform the following tasks.

5. Write a verification plan (see the example)
6. Write the testbench to test all the test cases mentioned in the verification plan

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# Good Luck 🙂