YAPP Router Specifications

The YAPP router accepts packets on a single input port (YAPP) and based on the address in the packet, it routes it onto any of the 3 output channels (channel0, channel1, channel2). It has a configuration port (HBUS) which is used to configure a number of internal registers.

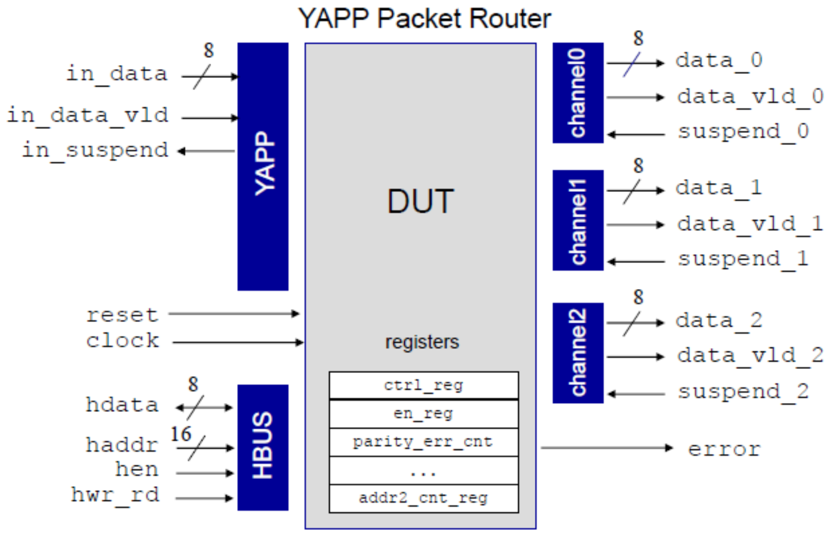


Figure 1. YAPP Router DUT

1. Packet Data Specifications

A packet is a sequence of bytes with

- First byte containing a header
- Next variable set of bytes is the packet payload
- Last byte is the parity byte

Header

The header contains two sub-fields

- A 2-bit address specifier for the channel
  - Address 3 is Illegal.
- A 6-bit length specifier indicating the number of bytes in the payload

Payload

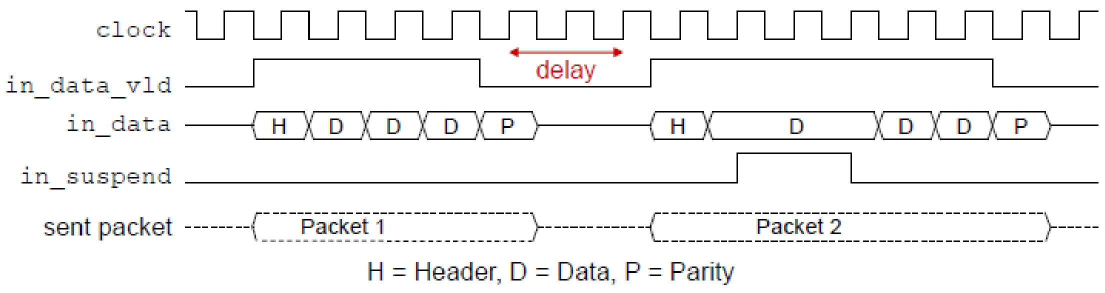
Payload has a minimum size of 1 and a maximum size of 63 bytes

Parity

Parity is a full byte of even parity calculated by XORing the header and every byte of the payload.

Router raises error output on receiving a bad parity packet.

2. YAPP Input Port Protocol



- All *input* signals are active high and are to be driven on the *falling* edge of the clock.
- in_data_vld must be asserted on the same clock when the first byte of a packet (the header byte) is driven onto the in_data bus. Because the header byte contains the address, this tells the router to which output channel the packet should be routed.
- Each subsequent data byte will be driven on the in_data bus with each new falling clock.
- After the last payload byte has been driven, on the next falling clock, the in_data_vld signal must be de-asserted, and the packet parity byte should be driven.
- The input data cannot change while the in_suspend signal is active (indicating FIFO full).

Figure 2. YAPP Input Port Protocol

3. YAPP Output Port Protocol

There are three output ports in YAPP (channel0, channel1 and channel2). All output signals are active high and are to be sampled at the falling edge of the clock. Each output port is internally buffered by a FIFO of depth 16 and a width of 1 byte. The router asserts the data_vld_x when valid data appears on the data_x output bus. The suspend_x signal must then be de-asserted on the falling edge in which the data_x is read from the output bus. As long as the suspend_x remains de-asserted, a valid byte is sent on the data_x bus on each rising edge of the clock.

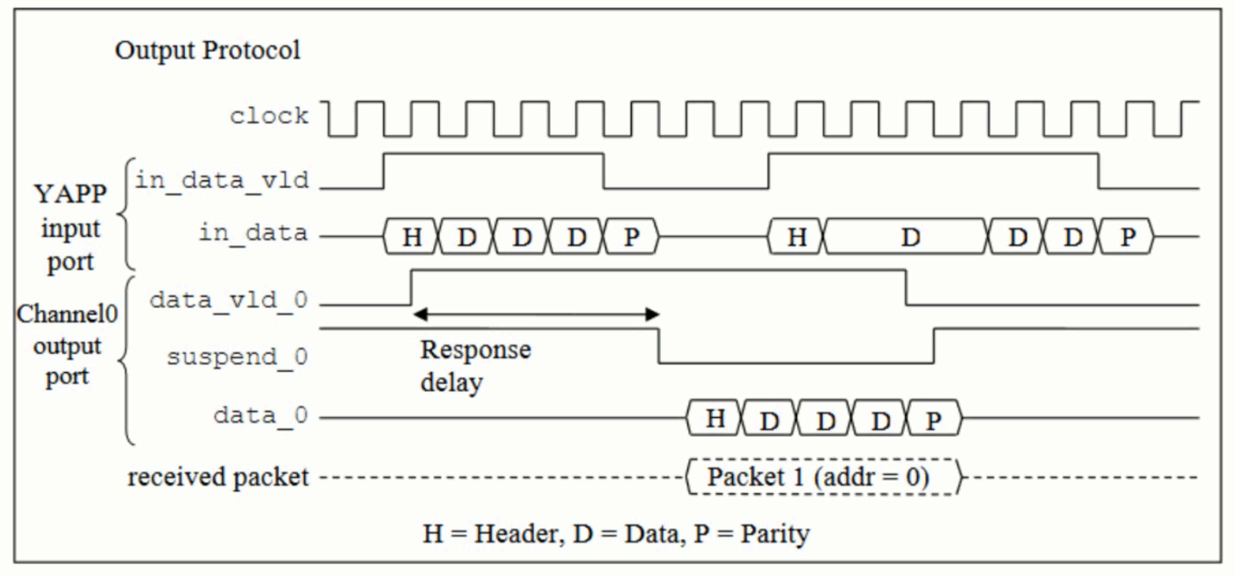
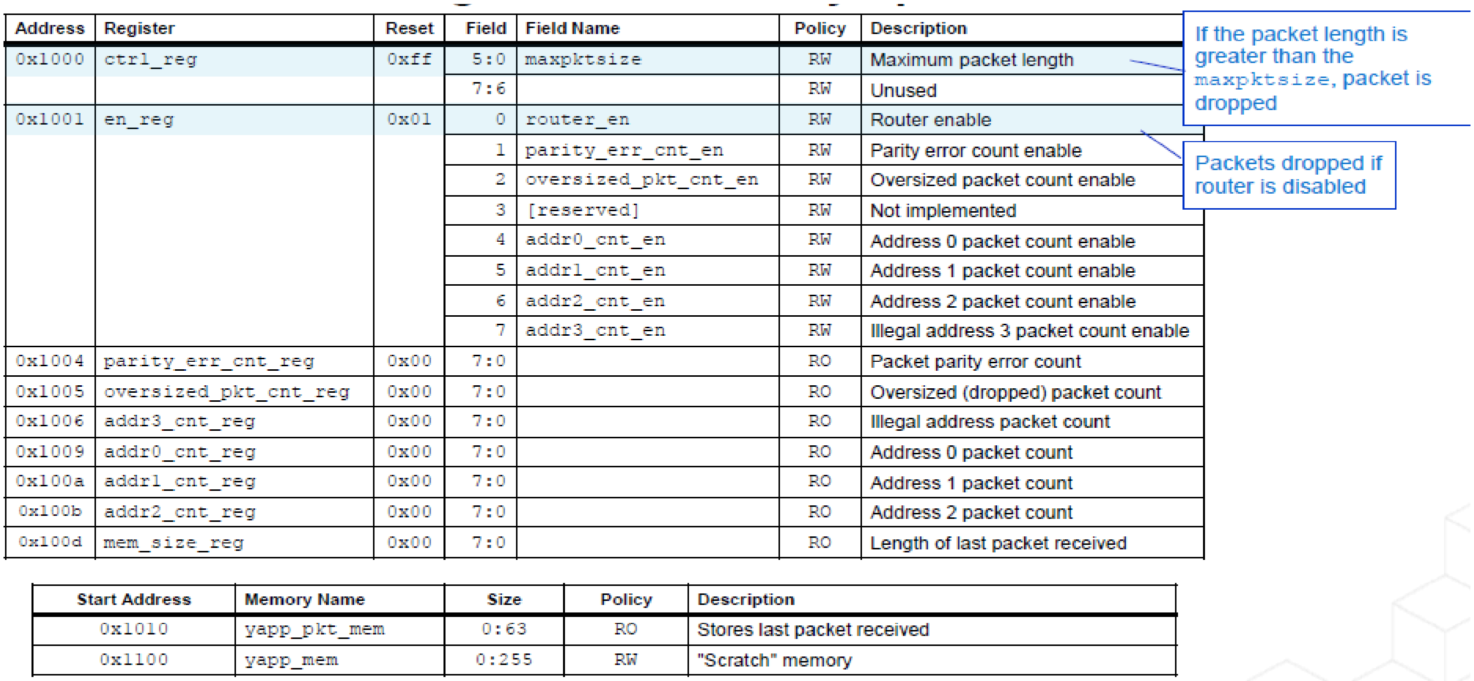


Figure 3. YAPP Output Port Protocol

4. YAPP Registers

YAPP has a number of registers which can be accessed using the HBUS interface as shown in Figure 1.



Address	Register	Reset	Field	Field Name	Policy	Description
0x1000	ctrl_reg	0xff	5:0	maxpktsize	RW	Maximum packet length
			7:6		RW	Unused
0x1001	en_reg	0x01	0	router_en	RW	Router enable
			1	parity_err_cnt_en	RW	Parity error count enable
			2	oversized_pkt_cnt_en	RW	Oversized packet count enable
			3	[reserved]	RW	Not implemented
			4	addr0_cnt_en	RW	Address 0 packet count enable
			5	addr1_cnt_en	RW	Address 1 packet count enable
			6	addr2_cnt_en	RW	Address 2 packet count enable
			7	addr3_cnt_en	RW	Illegal address 3 packet count enable
0x1004	parity_err_cnt_reg	0x00	7:0		RO	Packet parity error count
0x1005	oversized_pkt_cnt_reg	0x00	7:0		RO	Oversized (dropped) packet count
0x1006	addr3_cnt_reg	0x00	7:0		RO	Illegal address packet count
0x1009	addr0_cnt_reg	0x00	7:0		RO	Address 0 packet count
0x100a	addr1_cnt_reg	0x00	7:0		RO	Address 1 packet count
0x100b	addr2_cnt_reg	0x00	7:0		RO	Address 2 packet count
0x100d	mem_size_reg	0x00	7:0		RO	Length of last packet received

If the packet length is greater than the maxpktsize, packet is dropped

Packets dropped if router is disabled

Start Address	Memory Name	Size	Policy	Description
0x1010	yapp_pkt_mem	0:63	RO	Stores last packet received
0x1100	yapp_mem	0:255	RW	"Scratch" memory

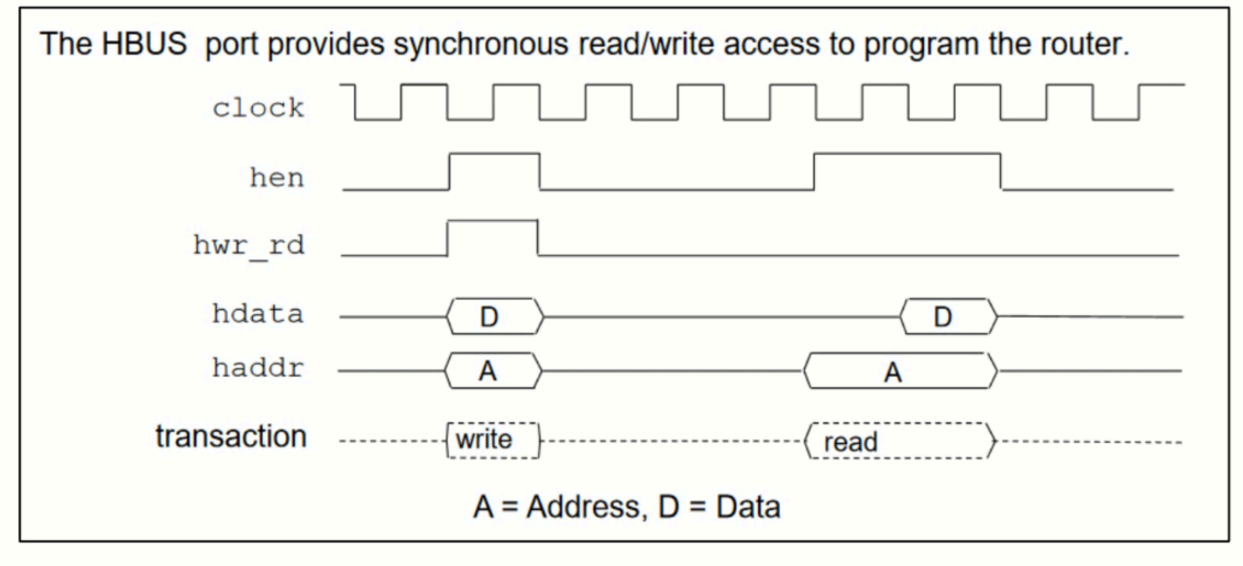
Figure 4. YAPP Registers

5. Host Interface Port Protocol (HBUS)

All input signals are active high and are driven on the falling edge of the clock. There are two transactions: write and read.

- *write* : when **hen** is asserted and **hwr_rd** is high, it means there is a write transaction on a register whose address is specified in **haddr** and data is specified in **hdata**

- *read* : when **hen** is asserted and **hwr_rd** is low, it means there is a read transaction from a register whose address is specified in **haddr.** The data will become available one cycle later on **hdata.** Hen is then de-asserted after 2 cycles as shown in Figure 5.


The HBUS port provides synchronous read/write access to program the router.

A = Address, D = Data

Figure 5. HBUS Port Protocol