19-June-2022

CSE 306
Computer Architecture Sessional
Assignment on Floating Point Adder

Problem Description:

In this assignment, you are required to design a floating point adder circuit which takes two floating points as inputs and provides their sum, another floating point as output. Each floating point will be **32 bits** long with following representation:

Sign	Exponent	Fraction
1 bit	10 bits	21 bits (Lowest bits)

You have to implement your design in any simulator software of your choice. Please note that, if your chosen simulator does not provide support for 32-bit ALU, you can construct one by cascading number of smaller ALUs. Moreover, since construction of ALU is not major focus of this assignment, you can take help from the Internet or other sources (or even use someone else's implementation) for the 32 bit ALU part only. The shifter circuit provided by the simulator software tool may be used as needed. Alternately, you may implement them yourselves. The rest of the circuit design and implementation must be done by you.

For this assignment, you will work in a group (same as the group for assignment on ALU). The report should contain introduction, problem specification, flowchart of the addition/subtraction algorithm, high-level block diagram of the architecture, detailed circuit diagram of the important blocks, ICs used with count as a chart, simulator used along with the version number and discussion.

Submission:

You have to submit the software simulation file renamed with your section followed by the group id (e.g., B1_Group9). If there are multiple files, zip the folder containing the files and rename the zip file using the same format. Only a single person from each group should submit. The submission deadline is the same for all sections and it is *11:55 PM, June 29, 2022 (Wednesday)*.