Section

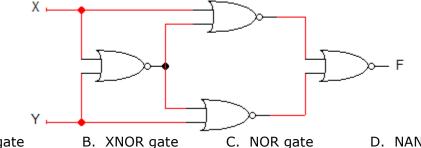
Final Exam (Spring 2013 Semester) Part I

Digital Logic Design

Marks: 40 Time: 25 mins

Note:

- There are 2 printed sides in this question paper.
- This part of the paper comprises of 20 MCQ's
- Encircle the correct option to each question on this paper.
- Cutting or overwriting is not allowed.
- Once done, hand in the question paper with your roll no. and Section mentioned on top.
- Q1) Odd parity of a word can be conveniently tested by
- A. OR gate B. AND gate C. NOR gate
- D. XOR gate
- Q2) Identify the logic function performed by the circuit shown in the given figure:



- A. XOR gate
- B. XNOR gate
- D. NAND gate
- Q3) The number of full and half-adders required to add two 16-bit numbers is

- A. 8 half-adders, 8 full-adders
 C. 16 half-adders, 0 full-adders
 D. 4 half-adders, 12 full-adders
- Q4) Which of the following gates would output 1 when one input is 1 and other input is 0?
 - A. OR gate

- B. AND gate C. NAND gate D. both (A) and (C)
- Q5) A demultiplexer is used to
 - A. Route the data from single input to one of many outputs
 - B. Select data from several inputs and route it to single output
 - C. Perform serial to parallel conversion
 - D. All of the above
- Q6) An OR gate can be thought of as
 - A. Switches connected in series

 B. Switches connected in parallel
 - C. MOS transistors connected in series D. None of the above
- Q7) Which combination of gates does not allow the implementation of an arbitrary boolean function?

 - A. OR gates and AND gates only B. OR gates and exclusive OR gate only
 - C. OR gates and NOT gates only D. NAND gates only

- Q8) Parallel adders are
 - A. combinational logic circuits
- B. sequential logic circuits

C. both (A) and (B)

D. None of these

Q9) A	Α.	is sl		B. i	s faster						als that se me speed a				r	
Q10) can h		?	the lar	_	number 4	of dat C.		puts v	vhich D.		data select	or wit	th t	wo con	trol inp	uts
Q11)	А. В. С.	combinational circuit is one in which the output depends on the . input combination at the time . input combination and the previous output . input combination at that time and the previous input combination . present output and the previous output														
Q12)	 The function of a multiplexer is A. to decode information B. to select 1 out of N input data sources and to transmit it to single channel C. to transmit data on N lines D. to perform serial to parallel conversion 															
Q13)			B = C, C = E			3 ⊕ C	= A		C.	Α (⊕ B ⊕ C =	0 D).	All of th	nese	
Q14)			ber of $(N) +$		flops req			modı (N-1)			ınter is C. log₂ (N	I) D). N	N log ₂ (I	N)	
		regi	ber of ster is 10			neede C.		shift 16	one D.	byt	e of data f	rom ii	npu	it to the	e outpu	t of a
Q16)	Α.	D ty	pe flip	-flop		type					hen flip-flo . flip-flop	p will	be	have as	s a	
Q17)	7) A Register is a A. set of capacitor used to register input instructions in a digital computer B. set to paper tapes and cards put in a file C. temporary storage unit within the CPU having dedicated or general purpose use D. part of the main memory															
Q18)	The A.		comple 355	ment B.	t of 381 508	is C.	(618	D.		390					
	ers.	The		of in		nat ca	n be		esent	ted	compleme by this cor C2 ³¹ to	npute	er is	5	-	
Q20)	How A.		ny diffo 63	erent	number B.	s can 64	a 6	-bit bi	nary C.	wo	rd represe 124	nt? D).	128		