Roll No. _____ Section:_____

Final Exam (Spring 2013 Semester) Part II

Digital Logic Design

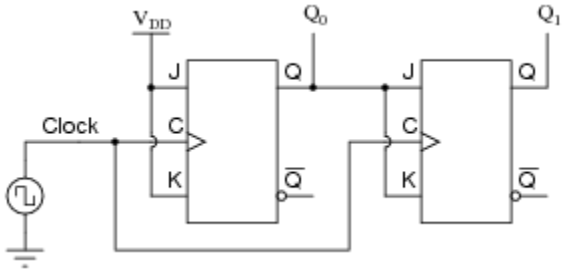
Marks: 150 **Time: 2 hrs 30 mins**

Note:

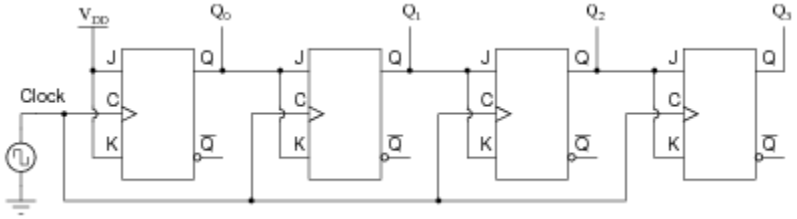
- There are 3 printed sides in this question paper.
- Make reasonable assumptions where and when required.
- Show all your working, otherwise no credit will be given.
- Manage your time wisely!

Q1. [20 marks]

A student just learned how a two-bit synchronous binary counter works, and he is excited about building his own. He does so, and the circuit works perfectly.



After that success, student tries to expand on their success by adding more flip-flops, following the same pattern as the two original flip-flops:



Unfortunately, this circuit didn't work. The sequence it generates is not a binary count. Determine what the counting sequence of this circuit is, and then try to figure out what modifications would be required to make it count in a proper binary sequence.

Q2. [20 marks]

A serial adder is a circuit that has two serial inputs (X and Y) and one serial output (S). The inputs represent two binary numbers that have bit values that appear serially beginning with the lowest significant bit first. The output is the serial sum of the two numbers. For example if two numbers, X = …01101 and Y = …11100 are presented as input, the corresponding output is S = …01001. Draw a state diagram for the serial adder.

Q3. [20 marks]

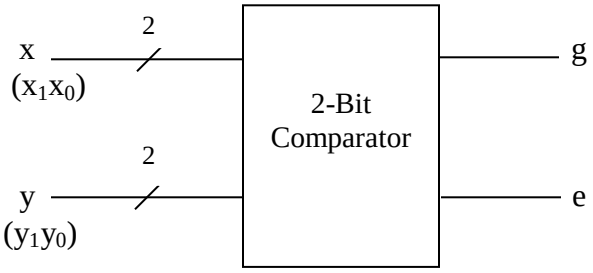
A set-dominate latch has a **set** (L) and a **reset** (M) input. It differs from a conventional SR latch in that an attempt to simultaneously set and reset the latch (i.e., when L=1 and M=1) results in **setting** the latch so that it stores a 1. In a normal SR latch these would be forbidden inputs.

a. Derive the characteristic equation for this latch.
b. Derive the excitation table for this latch.

Q4. [20 marks]

Given below is a two bit comparator circuit that compares two binary numbers, each two bits long, and gives the outputs such that:

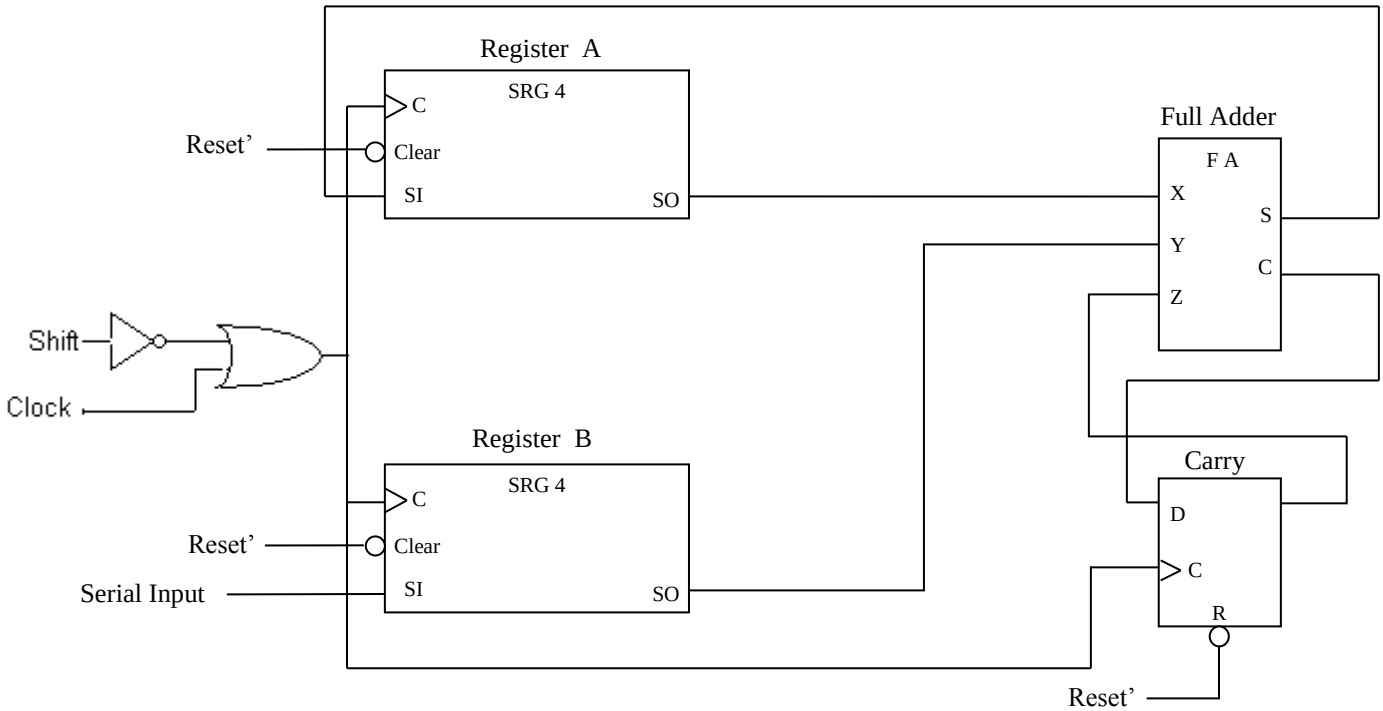
g=1 when (x > y);
e=1 when (x = y);
g=0, e=0 when (y > x);



Using two of these blocks and some additional logic, design a 4-bit comparator circuit for two 4 bit binary numbers **X** (X_3 $X_2X_1X_0$) and **Y**($Y_3Y_2Y_1$ Y_0). Your four bit comparator should have only two outputs namely **G** and **E** such that **G = 1** when **X > Y**, **E = 1** when **X = Y** and **G = 0, E = 0** when **Y > X**.

Q5. [20 marks]

The circuit below is the 4-bit serial adder from your text. It adds the contents of two 4-bit shift registers (A and B) and stores the result back in Register A, using a total of 4 clock cycles in the process. You are required to make slight modifications to the same circuit so that it becomes a serial Adder/Subtrator.



Q6. [20 marks]

Design a circuit that accepts two 2-bit binary numbers A_1A_0 and B_1B_0 and produces a 4-bit product $P_3P_2P_1P_0$ using an appropriate decoder and OR gates.

Q7. [30 marks]

Below is a state diagram showing a counter with a single input, X. When X is high the counter counts odd number and when it is low it counts even numbers. Design and Implement the circuit using only three dual 8x1 multiplexers, and JK flip-flops. You must show in detail every step of your circuit design.