LAB # 11

Objectives

To differentiate between the different types of shift register

Pre Lab

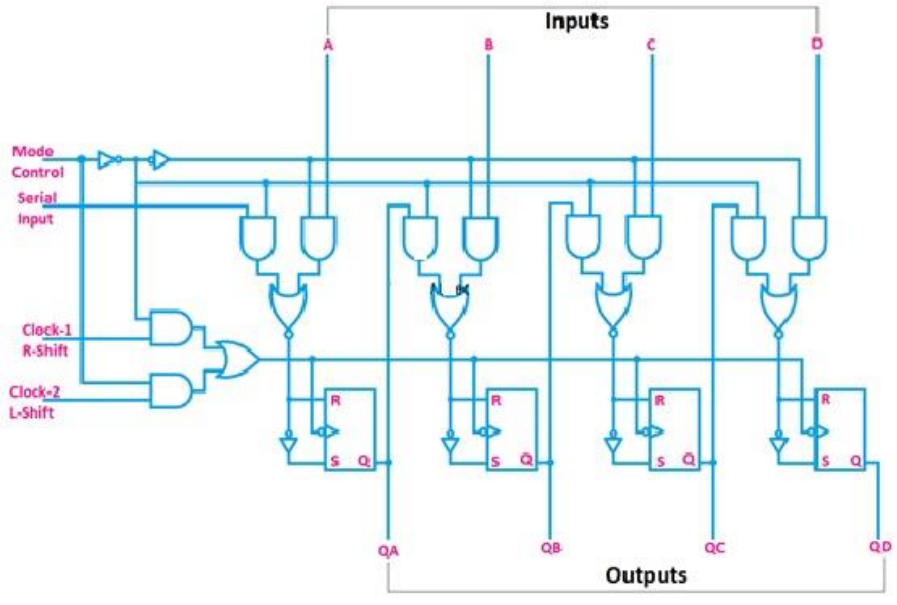
In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.

More generally, a shift register may be multidimensional, such that it's "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shiftregister'.

In Lab

Task 1: Create the shift register as per figure & fill the tables :



SERIAL IN SERIAL OUT (SISO) (Right Shift)

Serial i/p Data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-				
0	t1				
1	t2				
0	t3				
1	t4				
X	t5				
X	t6				
X	t7				
X	t8				

Table: 11.1

SERIAL IN PARALLEL OUT (SIPO)

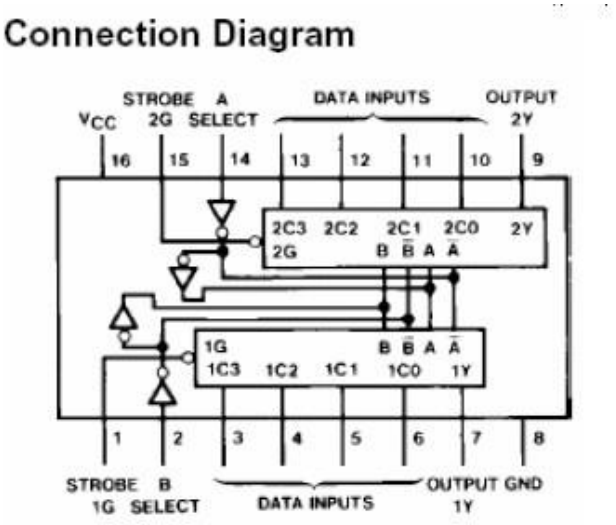
Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-				
0	t1				
1	t2				
0	t3				
1	t4				

Task 2: Draw the logic diagram of a shift register with D flip flops with mode selection inputs S1 and S0 and implement the circuit on the breadboard. The shift register is to be operated according to the following function table. One stage of this register should contain a 4-to-1 line MUX and a D-type flip-flop.

Mode Selection		Register Operations
S1	S0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load data

4X1 MUX:

Connection Diagram



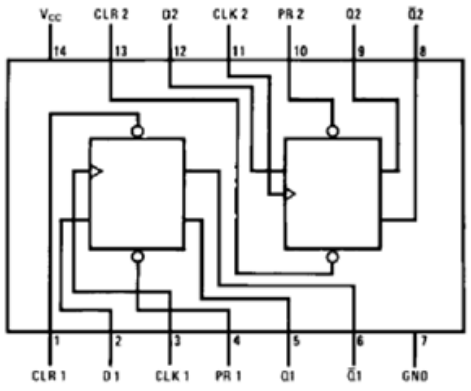
Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = HIGH Level
L = LOW Level
X = Don't Care

D FLIP FLOP

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.