

# Chapter 4

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## The Processor

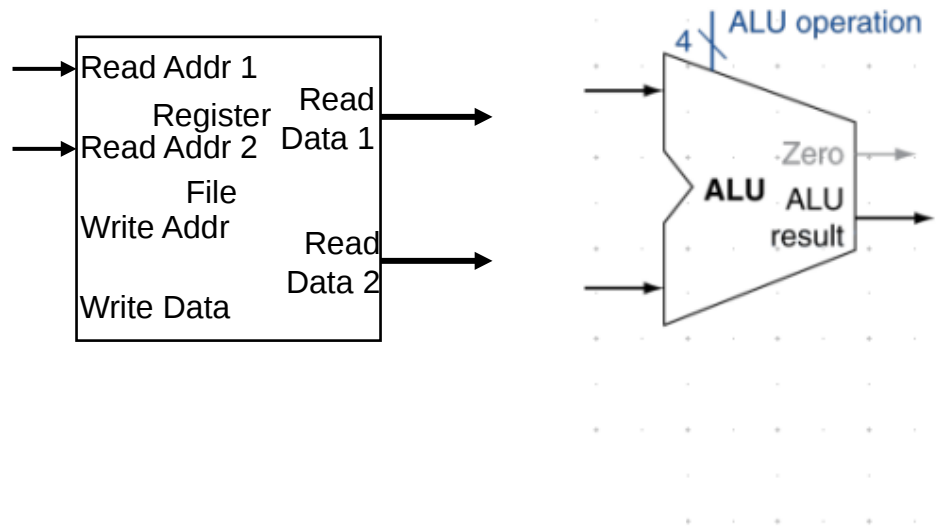
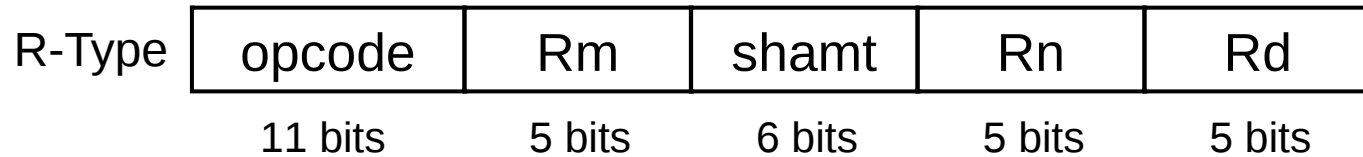
[Some slides adapted from A. Sprintson, M. Irwin, D. Paterson and others]

# Composing the Elements

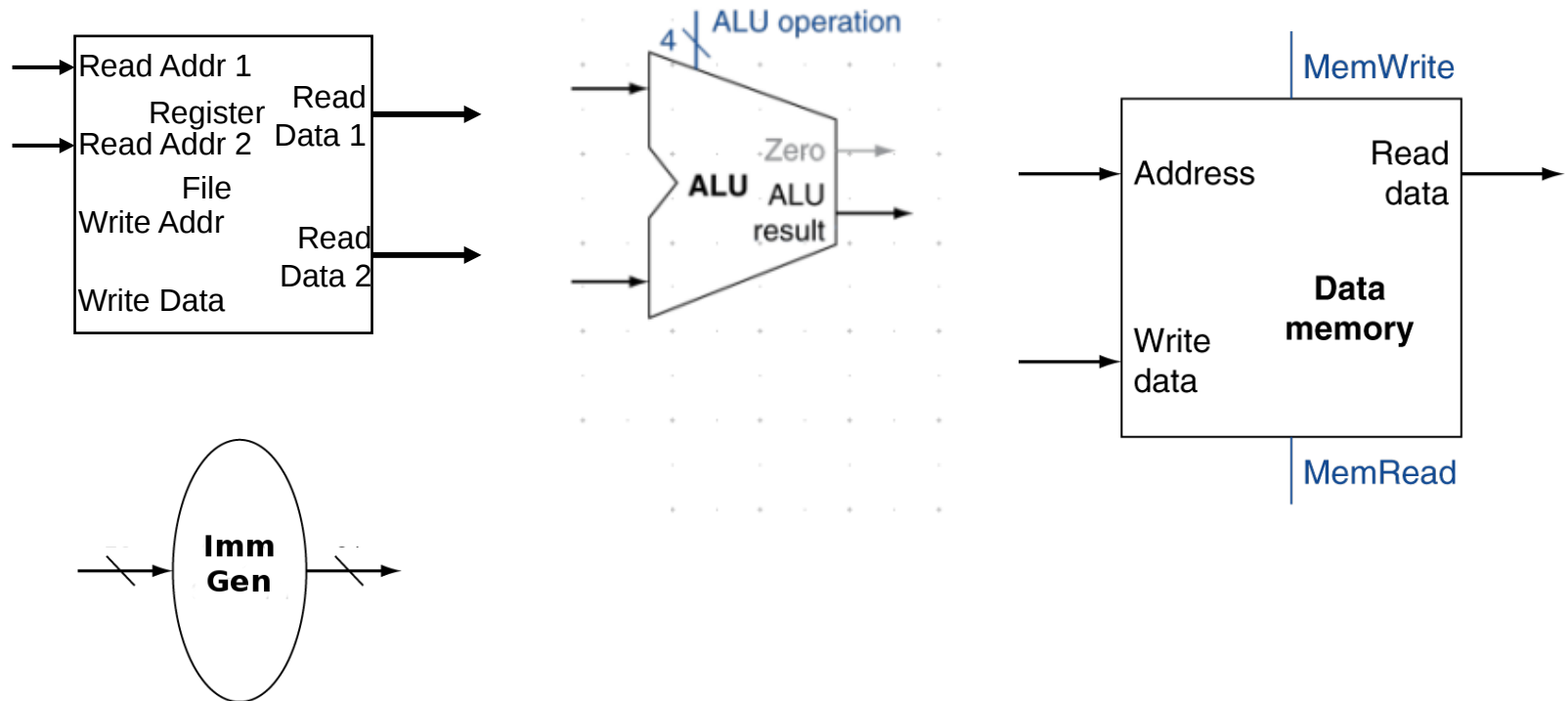
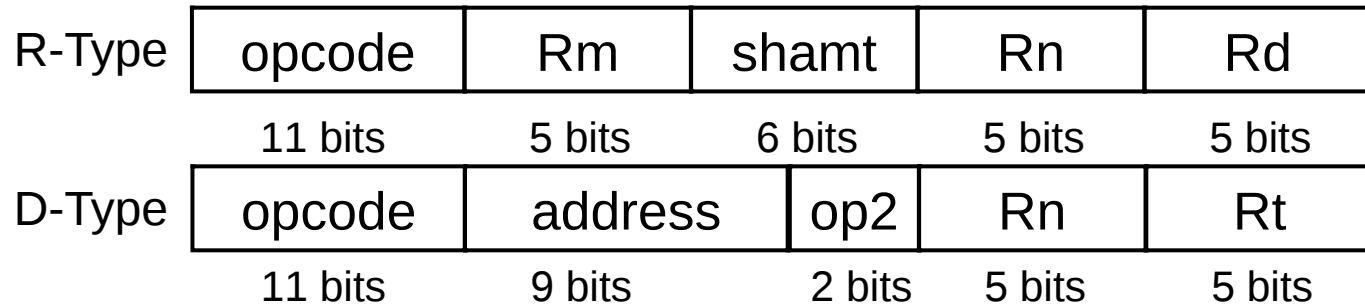
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- First-cut data path does an instruction in one clock cycle
  - Each datapath element can only do one function at a time
  - Hence, we need separate instruction and data memories
- Use multiplexers where alternate data sources are used for different instructions

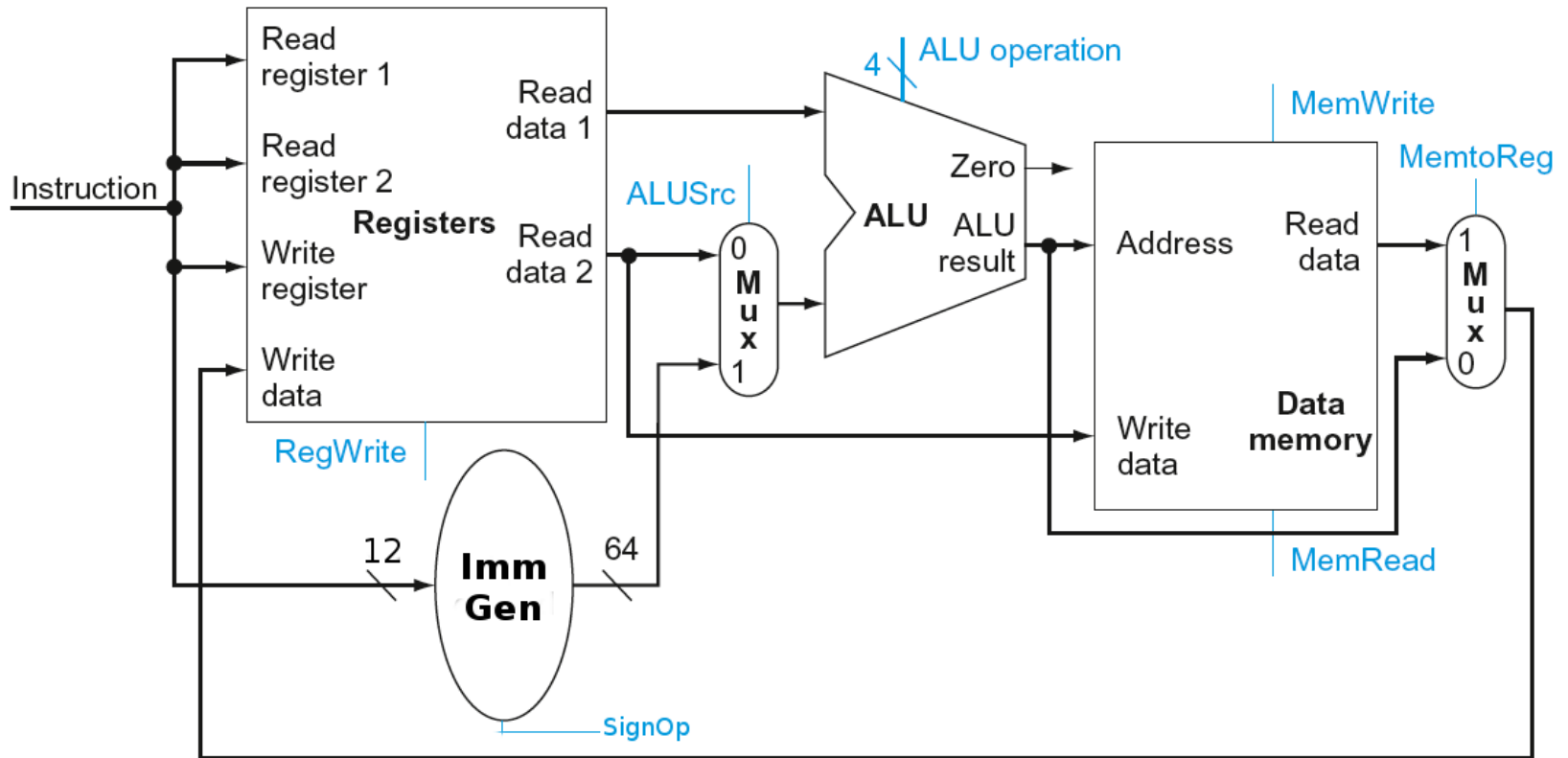
# Constructing a single Datapath:R-type



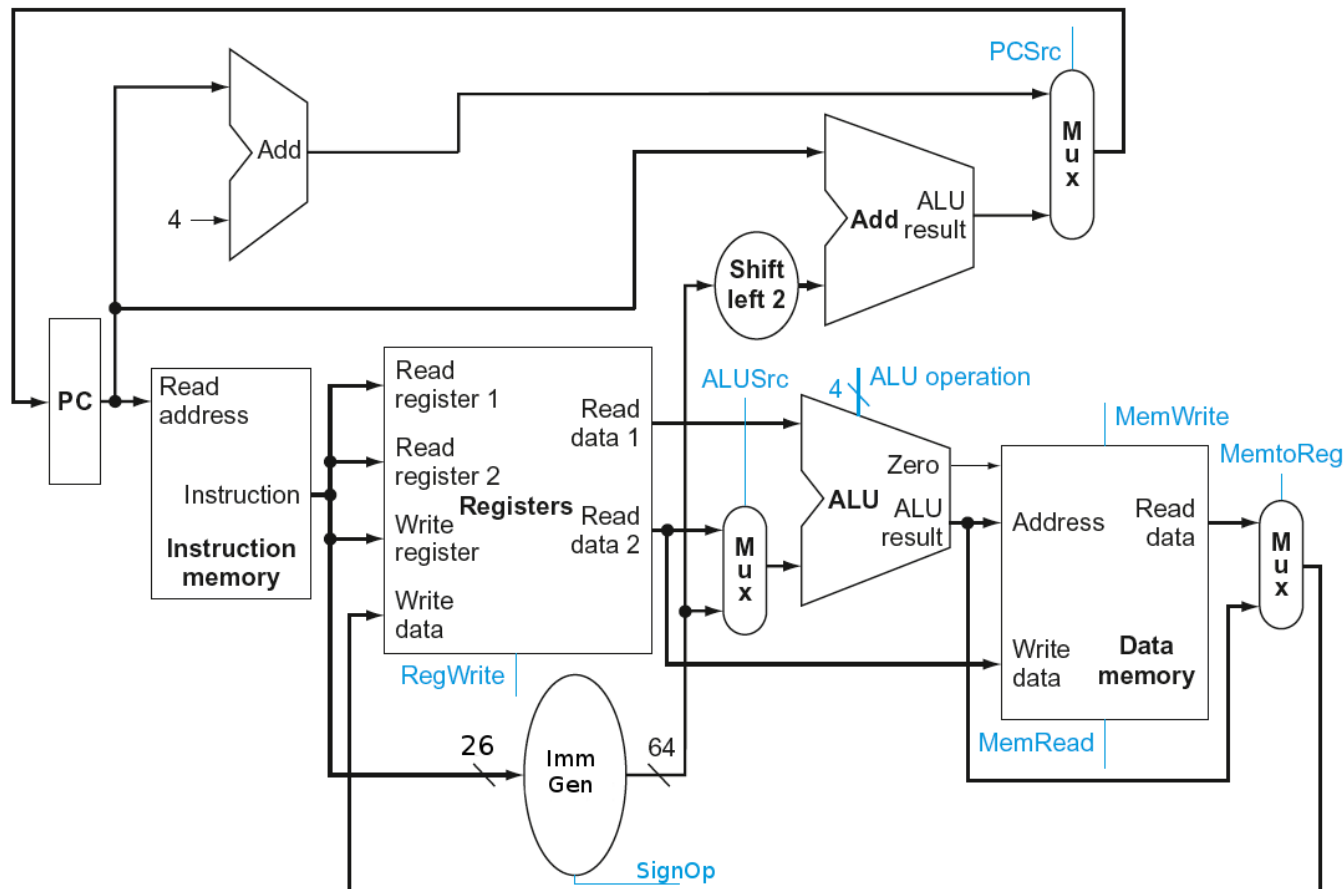
# Constructing a single Datapath: R-type, D-Type



# R-Type/Load/Store Datapath



# Full Datapath: Adding CB-Type



# ALU Control

- ALU used for
  - Load/Store:  $F = \text{add}$
  - Branch:  $F = \text{pass input } b \text{ (test for 0)}$
  - R-type:  $F$  depends on opcode

ALU control	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	pass input b
1100	NOR

# ALU Control

- Derive ALU control from Opcode field
  - Some Opcodes are only defined for 8-bits (or less) not 11...

opcode	Operation	Opcode field	ALU function	ALU control
LDUR	load register	11111000010	add	0010
STUR	store register	11111000000	add	0010
CBZ	compare and branch on zero	10110100XXX	pass input b	0111
R-type	ADD	10001011000	add	0010
	SUB	11001011000	subtract	0110
	AND	10001010000	AND	0000
	ORR	10101010000	OR	0001

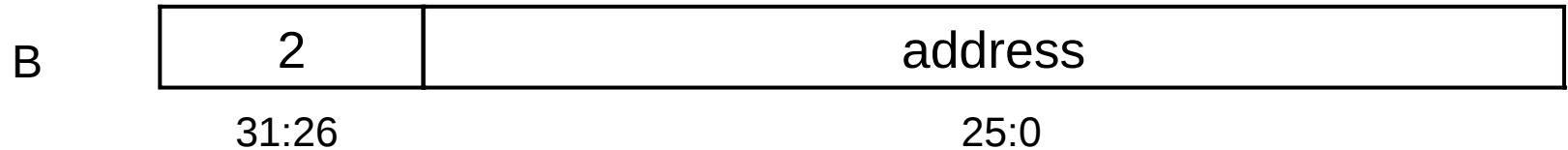


# Control Signals

- Derive control from Opcode field

	Opcode	Reg2 Loc	ALU Src	Mem toReg	RegW	MemR	MemW	PCSrc
LDUR	11111000010	X	1	1	1	1	0	0
STUR	11111000000	1	1	X	0	0	1	0
CBZ	10110100XXX	1	0	X	0	0	0	Zero?
R- type	10001011000	0	0	0	1	0	0	0
	11001011000							
	10001010000							
	10101010000							

# Implementing Uncnd'l Branch



- B uses word address
- Update PC with addition of
  - PC of the branch
  - Sign extended 26-bit address, left shifted by 2 bits
- Need an extra control signal decoded from opcode

# Datapath Adding B-Type

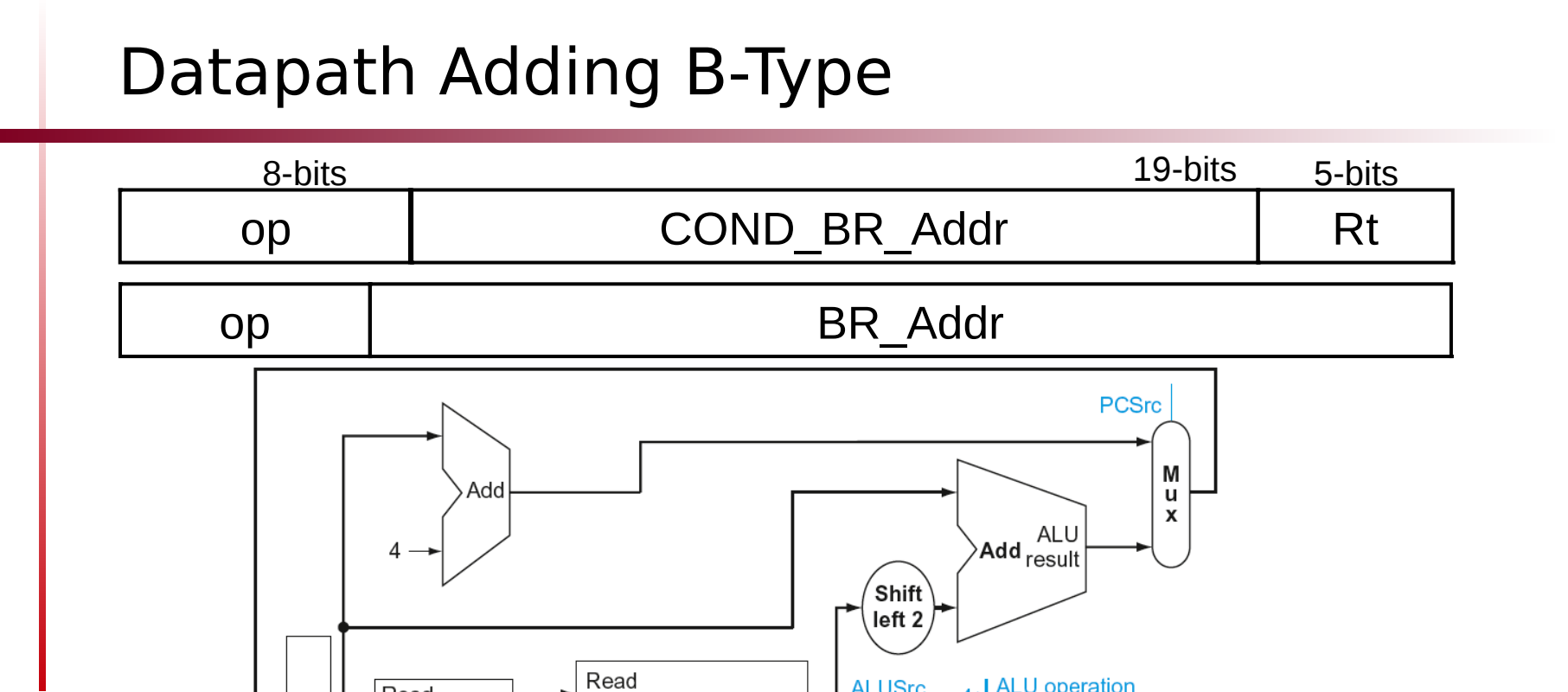
The diagram illustrates the B-Type instruction format and its datapath implementation.

**Instruction Format:**

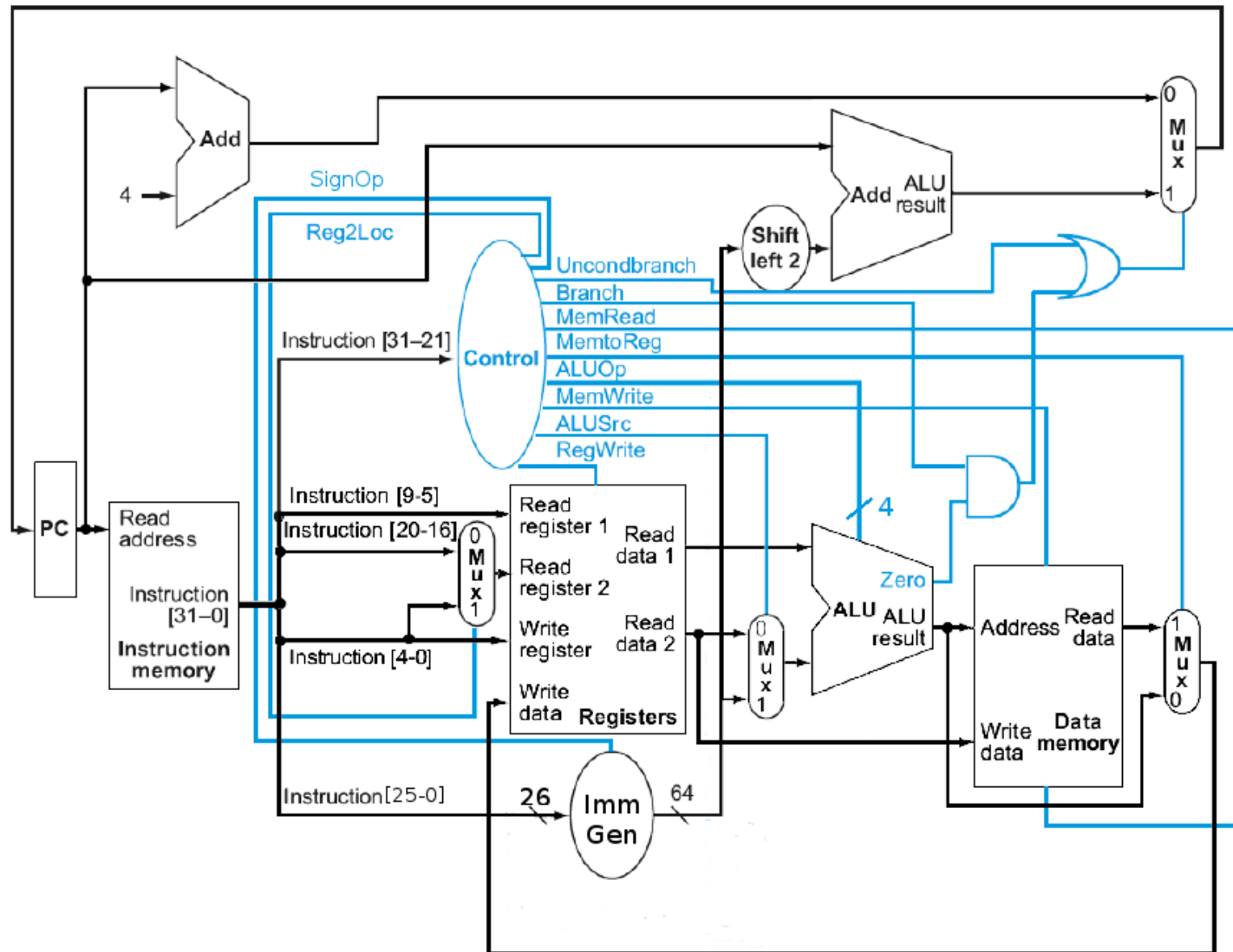
- 8-bits:** op
- 19-bits:** COND\_BR\_Addr
- 5-bits:** Rt

**Datapath Implementation:**

- The **op** field is used to control the **Add** and **Mux** components.
- The **COND\_BR\_Addr** field is used to control the **Shift left 2** component.
- The **Rt** field is used to control the **Mux** component.
- The **Add** component takes the **COND\_BR\_Addr** and the **PCSrc** as inputs and produces the **ALU result**.
- The **Mux** component takes the **ALU result** and the **PCSrc** as inputs and produces the **PCSrc** output.

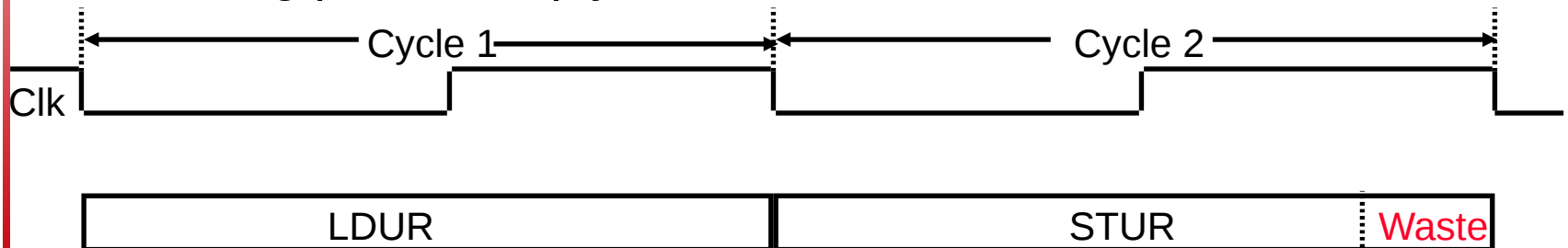


# Datapath With Control



# Single Cycle Disadvantages & Advantages

- Uses the clock cycle inefficiently – the clock cycle must be timed to accommodate the slowest instr
- especially problematic for more complex instructions like floating point multiply



- Each datapath component is used only for a small part of the cycle

but

- It is simple and easy to understand

# Where We are Headed

- Another approach
  - Sub-divide up the cycle into stages (pipelining)
  - Multiple instructions in flight at a time

