1)For the following instruction fill in the following blanks to answer the questions:

LDUR X3, [X4, 0x40]

Assume X3 currently has 0x100 in it and X4 currently has 0x200 in it.

Assume the following memory addresses have the associated data in them as listed in this table:

|  |  |
| --- | --- |
| Address | Data |
| 0x100 | 0x0 |
| 0x140 | 0x1 |
| 0x200 | 0x2 |
| 0x240 | 0x3 |
| 0x300 | 0x4 |

At the end of this instruction X3 = \_\_\_\_

and

X4 = \_\_\_\_\_

Note: Make sure your answers are preceded with a 0x (ie. 0x12).

**2)** For the following instruction fill in the following blanks to answer the questions:

STUR X3, [X4, 0x40]

Assume X3 currently has 0x100 in it and X4 currently has 0x200 in it.

Assume the following memory addresses have the associated data in them before the instruction is executed as listed in this table:

|  |  |
| --- | --- |
| Address | Data |
| 0x100 | 0x0 |
| 0x140 | 0x1 |
| 0x200 | 0x2 |
| 0x240 | 0x3 |
| 0x300 | 0x4 |

Fill in the table for what the values will be after the instruction has executed:

|  |  |
| --- | --- |
| Address | Data |
| 0x100 | \_\_\_ |
| 0x140 | \_\_\_ |
| 0x200 | \_\_\_ |
| 0x240 | \_\_\_ |
| 0x300 | \_\_\_ |

As always precede each value with 0x

**3)**

|  |
| --- |
| ARMv8 and many other RISC ISAs are considered to be a "Load/Store Architecture" because many computational instructions operate directly on the memory. |
| |  |  | | --- | --- | | Selected Answer: | Correct False | | Answers: | True | |  | Correct False |  |  |  | | --- | --- | | Response Feedback: | CISC instructions often operate directly on the memory, RISC instructions are load/store because they must first move from memory with a separate load instruction, perform the computation and store back with a store instruction. | |

**4)**

|  |
| --- |
| Which of the following correctly describes the effect of this load instruction:  LDUR X3, [X3, 0]  Where X3 initially has the value of 0x12340 in it and memory address 0x12340 has the value of 0x34 in it. |
| |  |  | | --- | --- | | Selected Answer: | Correct  The value 0x34 is copied into X3. | | **5)**   |  | | --- | | How are registers different from memory? Select all that apply | | |  |  | | --- | --- | | Selected Answers: | CorrectC.  Registers operate faster than memory. | |  | CorrectD.  Registers are internal to the processor core, while memory is external. | |  |  | |  |  | |  |  | |  |  | | |  | |  |  | |  |  | |  |  | |