* **Question 1**

1 out of 1 points

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | | |
| Correct | Given the following instruction:  LDURB X1, [X2, 0x4]  Where X1 = 0x123456789abcdef0  and X2 = 0x0  and memory currently has the following data:   |  |  | | --- | --- | | Address | Data | | 0x0 | 0xDEADBEEF12345678 | | 0x8 | 0xBA5EBA11F005BA11 |   What will be left in X1 after the instruction executes (assume little endian): \_\_\_\_\_\_ |  |  |  |
| |  |  | | --- | --- | | Selected Answer: | Correct 0x00000000000000EF |  |  | | --- | |  | |  |  |  |

* **Question 2**

1 out of 1 points

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | | |
| Correct | In general, control flow instructions do no work, i.e. they manipulate no data. |  |  |  |
| |  |  |  | | --- | --- | --- | | Selected Answer: Correct True |  |  | | |  |  | | --- | --- | | Response Feedback: | Control flow instructions choose which instruction will be exectued next but they do not change the state of the processor otherwise. | |  |  | |  |  |  | |  |  |  |

* **Question 3**

1 out of 1 points

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| --- | --- | --- | --- | --- |
|  |  | | | |
| Correct | Given the following instruction executed on ARMv8 in little endian mode:  STUR X3, [X4, 0x0]  Where the following register values are current:   |  |  | | --- | --- | | Register | Value | | X3 | 0x123456789abcdef0 | | X4 | 0x0 |     What byte will be stored in address 0x2? \_\_\_**[LE]**\_\_\_\_\_  What byte will be stored in the same address in big endian mode? \_\_**[BE]**\_\_\_\_\_ |  |  |  |
| |  |  | | --- | --- | | Specified Answer for: LE | Correct0xbc | | Specified Answer for: BE | Correct0x56 | |  |  |  |

* **Question 4**

1 out of 1 points

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| --- | --- | --- | --- | --- |
|  |  | | | |
| Correct | The following C code fragment:  if (a==b) {     c = 1;  } else {    c = 0;  }  Could be translated into binary as the following:  SUB X4, X0, X1  CBZ X4, HERE  ADD X3, XZR, 1  B END HERE: ADD X3, XZR, XZR END:  (assume a is in X0, b is in X1, and c is in X3) |  |  |  |
| |  |  | | --- | --- | | Selected Answer: Correct False |  | | |  |  | | --- | --- | | Response Feedback: | The CBZ should be a CBNZ or the ADDs should be swapped. | |  | |  |  | |  |  |  |

* **Question 5**

1 out of 1 points

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| --- | --- | --- | --- | --- |
|  |  | | | |
| Correct | If the condition in a conditional branch is false, the instruction is not executed. |  |  |  |
| |  |  | | --- | --- | | Selected Answer: | Correct False | |  |  | |  |  | |  |  |  |