Bangladesh Army University of Science and Technology

Department of Computer Science and Engineering

Referred/Improvement/Backlog Examination, Fall 2018 **Level-I Term-II**
Course code: EEE 1269 **Course Title: Electronic Devices and Circuits**
Time: 03 (Three) hours **Full Marks: 210**

N.B. (i) Answer any three questions from each PART (ii) Use separate answer script for each PART
(iii) Marks allotted are indicated in the margin (iv) Symbols and abbreviations bear usual meanings

PART A

1. a) What do you understand by a semi-conductor? Discuss some important properties of semiconductor. 10

   b) What is electronics? Mention some important applications of electronics. 10

   c) The *6.8-V* zenar diode in the circuit of Fig. 1(c) is specified to have $V_Z = 6.8V$ at $I_Z = 5mA$, $r_z = 20\Omega$, and $I_{ZK} = 0.2\ mA$. The supply voltage V is nominally *10 V* but can vary by *±1 V*. 15

      i. Find V_O with no load and with V at its nominal value.

      ii. Find the change in V_O resulting from the *±1-V* change in V

      iii. Find the change in resulting from connecting a load resistance R_L that draws a current $I_L = 1\ mA$.

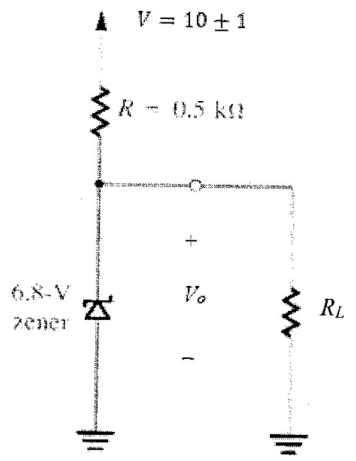

Fig. 1(c)

2. a) What do you understand by intrinsic and extrinsic semiconductors? Explain the formation of potential barrier in a pn junction. 15

   b) What is zenar diode? Write down the differences between ideal diode and zenar diode 10

   c) Why BJT is called bi-polar? Find out the relations between common base current gain (α) and common emitter current gain (β). 10

3. a) Design a diode logic circuit for the expression $V_0 = (A+B).(B+C)$ where *A, B & C* are inputs. 10

   b) Draw a full wave rectifier circuits and explain its operations with input and output wave shapes. 13

c) For the network of Fig. 3(c) determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V. 12

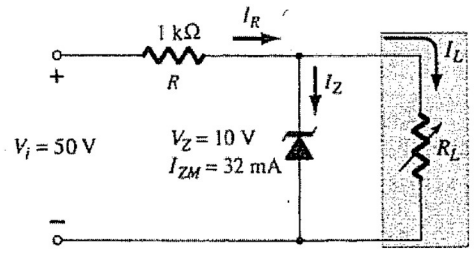

Fig. 3(c)

4. a) Claculate the constant current I in the circuit of Fig. 4(a) 10

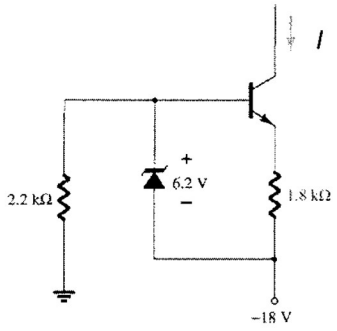

Fig. 4(a)

b) Draw the hybrid equivalent model for the common-emitter and common base transistor configuration. 15

c) What is stability factor? Derive the equation of stability factor for common emitter configuration in terms of I_{CBO} 10

PART B

5. a) For the parallel clipper given in Fig. 5(a), draw the output waveform and explain its operation. 10

Where $v_i = 10 \sin wt$

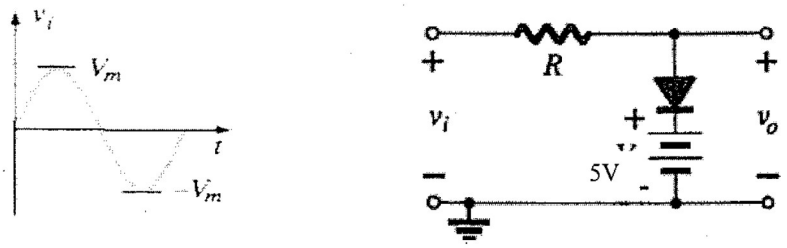

Fig. 5(a)

c) Determine V_o for the configuration given at Fig. 7(c) 10

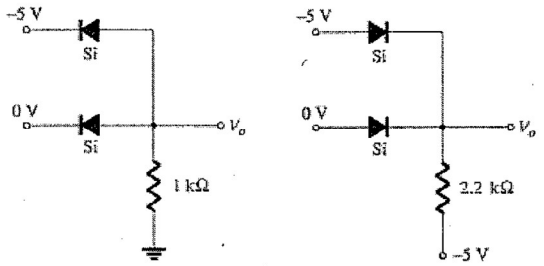

Fig. 7(c)

8. a) What is an operational amplifier? Write down the properties of an ideal op-amp. Also draw the equivalent circuit of the nonideal op amp. 13

b) Determine the output voltage for the following circuit given at Fig. 8(b) 12

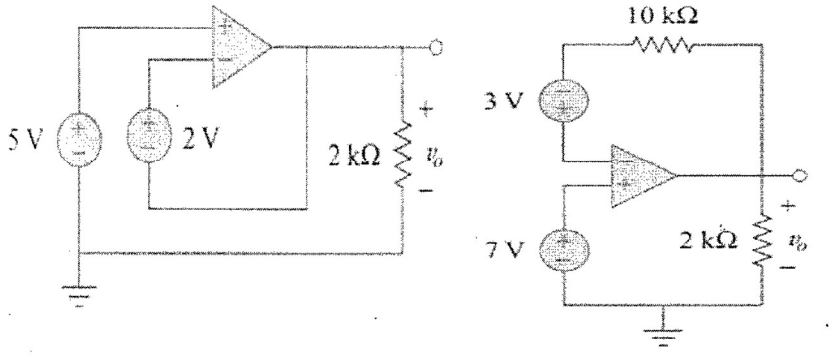

Fig. 8(b)

c) What is difference amplifier? Design an op amp circuit with inputs v_1, v_2 and v_3 such that 10

$v_o = v_1 + 2v_2 - 3v_3$

b) Draw the output characteristics of BJT in case of common emitter configuration and mark its different regions, also explain the operating principle of BJT in case of active mode n-p-n transistor. 15

c) What is biasing of a transistor? Draw a voltage divider biasing circuit using n-p-n transistor. 10

6. a) For the circuit shown in the Fig. 6(a), find out i) I_B ii) I_C iii) V_{CE} iv) V_{BC} 15

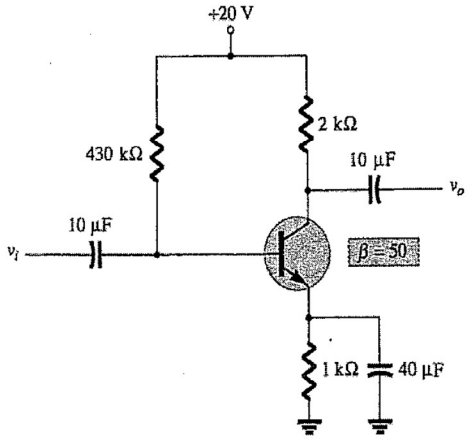

Fig. 6(a)

b) For the circuit in Fig. 6(b), find the value of R that results in $V_D = 0.8V$, The MOSFET has $Vtn = 0.5V$, $\mu_n C_{ox} = 0.4\ mA/V^2$, $W/L = 4$. 10

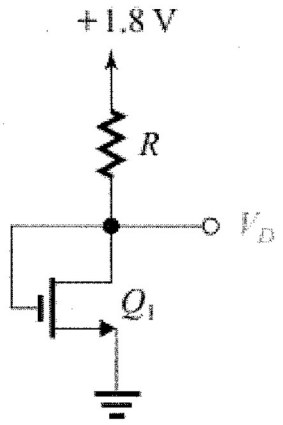

Fig. 6(b)

c) What are the differences between FET and BJT? Write down the families of FET. 10

7. a) What are the differences between JFET and MOSFET? Explain the output characteristics of n-channel JFET with several values of V_{GS} and V_{DS} with some positive values. 15

b) Describe the modes of operation of BJT. 10