

EECE 238 Exam II

Name:

Problem 1 /30

Problem 2 /30

Problem 3 /15

Problem 4 /25

Total: /100

Good Luck!

Problem 1 (30 points total) Sequence Recognizer Design.

Design a digital circuit to recognize the occurrence of the input sequence 1001. The circuit will output a 1 when the previous inputs were 100 and the current input is 1. Note that since the output depends on the input (as well as the current state), you need a *Mealy* solution to this problem.

- 1 (a) (12 points) Derive the state transition diagram.
- 1 (b) (10 points) Derive the state table and Flip-Flop inputs for J-K Flip-Flops.
- 1 (c) (5 points) Use Karnaugh maps to minimize the equations for the Flip-Flop inputs, and the output.
- 1 (d) (3 points) Draw the final circuit.

Problem 2 (30 points total) Synchronous Counter Design.

Design a binary counter that counts through the 3-bit binary numbers: 000, 111, 001, 110, 010, 101, and then repeat from 000. For your design, assume that **there is** a reset signal that will force counting to start at 0. Assume that the states codes are assigned unsigned integer representations.

- 2 (a) (10 points)** Draw the state transition diagram.
- 2 (b) (10 points)** Derive the state table for implementing the counter using J-K Flip-Flops.
- 2 (c) (5 points)** Use K-maps to minimize the inputs to the J-K Flip-Flops.
- 2 (d) (5 points)** Indicate the final circuit.

Problem 3 (15 points total) *Sequential Circuit Analysis I*

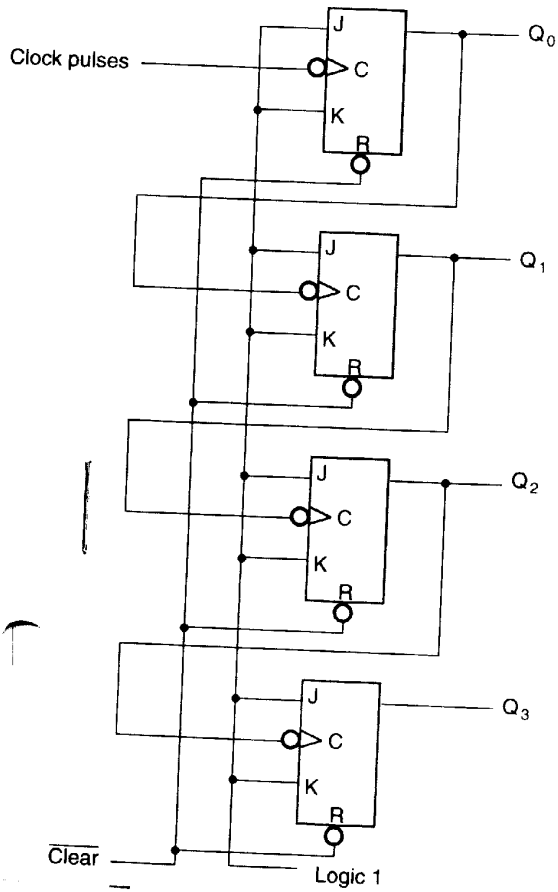
Consider the sequential circuit given below. We would like to analyze the circuit and understand what it does.

- 3 (a) (5 points)** Derive the J-K flip-flop input equations.
- 3 (b) (7 points)** Derive the next-state table based on 3(a).
- 3 (c) (3 points)** Derive the state-diagram based on the next-state table.

Problem 3 (10 points total) *Ripple Counting*

Consider the 4-bit Ripple Counter shown below. Assume that: $Q_0 = 1, Q_1 = 0, Q_2 = 1, Q_3 = 0$.

Clearly indicate how the states of Q_0, Q_1, Q_2, Q_3 change after 4 clock periods.



Problem 4 (25 points total) *Modulo-4 Parity Detector*

Using T Flip-Flops, design an even parity detector that outputs a 1 **after** a multiple of 4 1s have been received. Note that since the output does not depend on the current input, you will need a *Moore* solution to this problem. Also, assume that zero is a multiple of 4 ($0=0*4$).

- 4 (a) (10 points)** Derive the state transition diagram.
- 4 (b) (10 points)** Derive the state table and S-R flip-flop inputs.
- 4 (c) (5 points)** Indicate the final Circuit using S-R flip-flops.