Homework 2 (Due Date: Thursday, Jan 31st In Class)

Sanjay Krishna: University of New Mexico

HW 2, ECE 322L, Spring 2013,

Problem 3.45

Consider the circuit in Figure P3.44. The transistor parameters for M_1 are $V_{TN} = 0.4$ V and $k_n' = 120\,\mu$A/V^2, and for M_2 are $V_{TN} = -0.6$ V, $k_n' = 120\,\mu$A/V^2, and $W/L = 1$. Determine the W/L ratio of M_1 such that $\upsilon_O = 0.025$ V when $\upsilon_I = 3$ V.

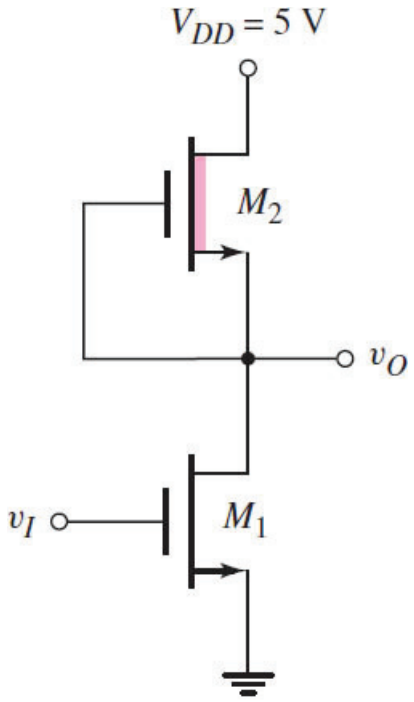

Figure P3.44

Problem 3.47

Consider the circuit in Figure P3.47. (a) The nominal transistor parameters are $V_{TN} = 0.6$ V and $k_n' = 120\,\mu$A/V^2. Design the width-to-length ratio required in each transistor such that $I_{DQ} = 0.8$ mA, $V_1 = 2.5$ V, and $V_2 = 6$ V. (b) Determine the change in the values of V_1 and V_2 if the k_n' parameter in each transistor changes by (i) +5 percent and (ii) -5 percent. (c) Determine the values of V_1 and V_2 if the k_n' parameter of M_1 decreases by 5 percent and the k_n' parameter of M_2 and M_3 increases by 5 percent.

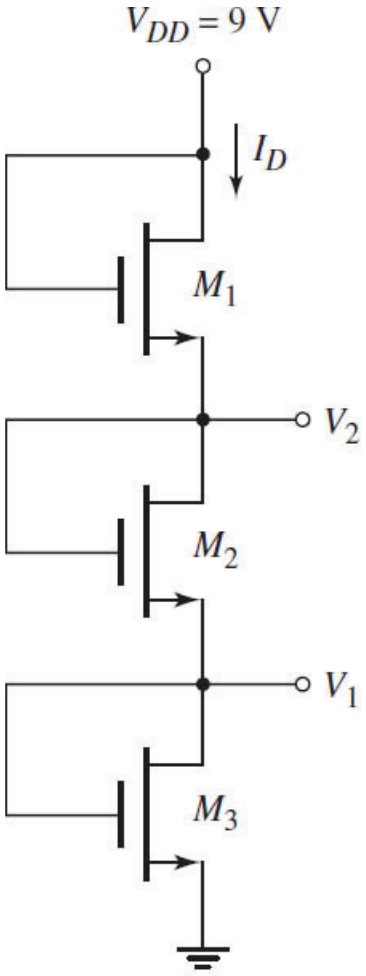

Figure P3.47

Problem 3.53

For the two-input NMOS NOR logic gate in Figure 3.46 in the text, the transistor parameters are $V_{TN1} = V_{TN2} = 0.6$ V, $\lambda_1 = \lambda_2 = 0$, and $k'_{n1} = k'_{n2} = 120\,\mu$A/V^2. The drain resistor is $R_D = 50$ kΩ. (a) Determine the width-to-length ratios of the transistors so that $V_O = 0.15$ V when $V_1 = V_2 = 5$ V. Assume that $(W/L)_1 = (W/L_2)$. (b) Using the results of part (a), find V_O when $V_1 = 5$ V and $V_2 = 0.2$ V.

Problem 3.65

The transistor in the circuit in Figure P3.65 has parameters $I_{DSS} = 8$ mA and $V_P = 4$ V. Design the circuit such that $I_D = 5$ mA. Assume $R_{in} = 100$ k Ω. Determine V_{GS} and V_{SD}.

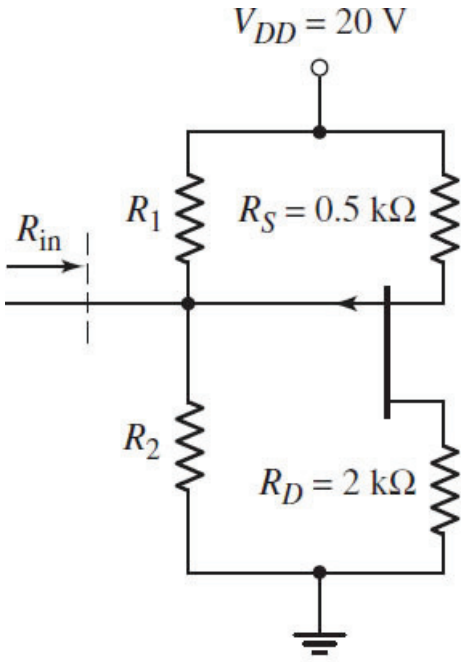

Figure P3.65

Problem 3.71

The GaAs MESFET in the circuit in Figure P3.71 has parameters $k = 250\ \mu A/V^2$ and $V_{TN} = 0.20$ V. Let $R_1 + R_2 = 150$ k Ω. Design the circuit such that $I_D = 40\ \mu A$ and $V_{DS} = 2$ V.

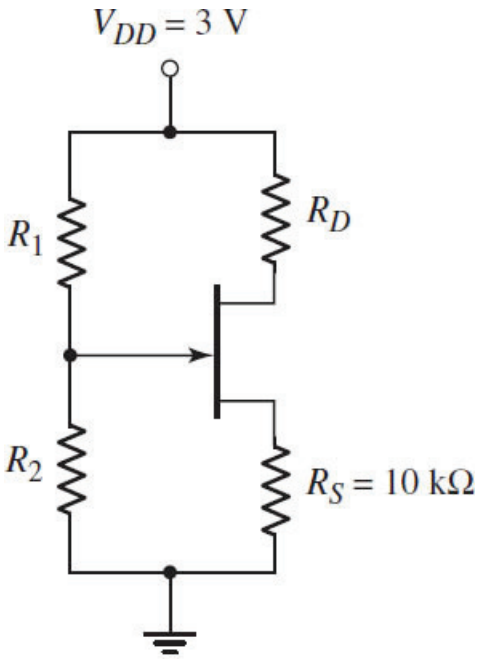

Figure P3.71