

ECE 338 – Advanced Logic Design

Assignment 1

Due Date: February 18, 2011

Design an adder for IEEE 32 bit floating point numbers. That is, design an adder system that will accept two values expressed in the IEEE 32 bit floating point number system, perform the addition, and generate an output that also conforms to the floating point format. All of the activity must take place without the use of clocks or clocked shifting. The one area that will be relaxed is the creation of answers that are un-normalized. When an answer is un-normalized, or when overflow/underflow occurs, create a value that is $\pm\infty$.

The inputs to the system are:

| | |
|-------|-----------------------------|
| A_VAL | 32 bit floating point value |
| B_VAL | 32 bit floating point value |

The output is:

| | |
|-------|-----------------------------|
| F_VAL | 32 bit floating point value |
|-------|-----------------------------|

Do the design in a top-down fashion. That is, start with a simple block diagram, then create a more detailed version, and finally implement the blocks in VHDL. This system is to be implemented in a structural fashion, and each gate level costs one nanosecond.

A test bench will be provided. The entity statement for the unit should be:

```
entity FP_ADDER is
  port (
    A_VAL : in  STD_LOGIC_VECTOR (31 downto 0 );
    B_VAL : in  STD_LOGIC_VECTOR (31 downto 0 );
    F_VAL : out STD_LOGIC_VECTOR (31 downto 0 )
  );
end entity FP_ADDER;
```