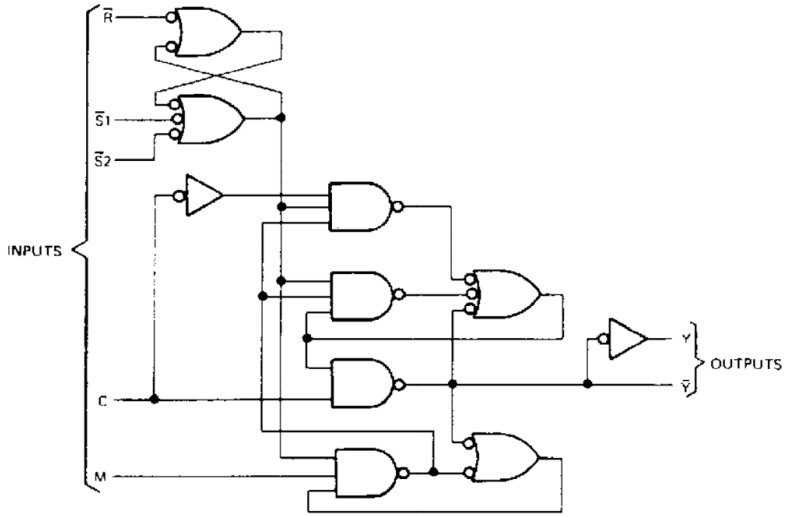
Asynchronous Design Technique in Reverse ➔ Analysis

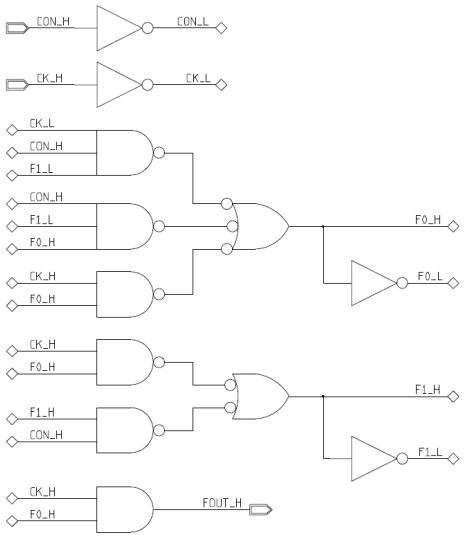
Analysis Technique

- Reverse order for analysis
- Start with logic diagram
- Generate equations
- Put equations in K-Map (Final State Table)
- Determine stable, unstable states
- Generate State Diagram
- Determine behavior

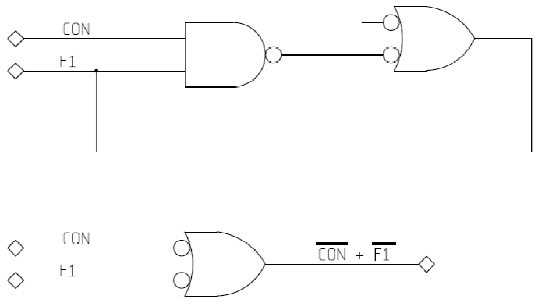
SN74120 – Pulse Synchronizer



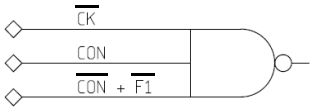
Cleaned Up Schematic



Start with Simplest Feedback



Now Work on Three Input NAND

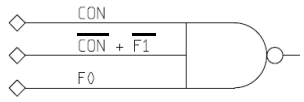


$$\overline{CK} \bullet CON \bullet (\overline{CON} + \overline{F1})$$

$$\overline{CK} \bullet CON \bullet \overline{CON} + \overline{CK} \bullet CON \bullet \overline{F1}$$

$$\overline{CK} \bullet CON \bullet \overline{F1}$$

Now Work on Second Three Input NAND

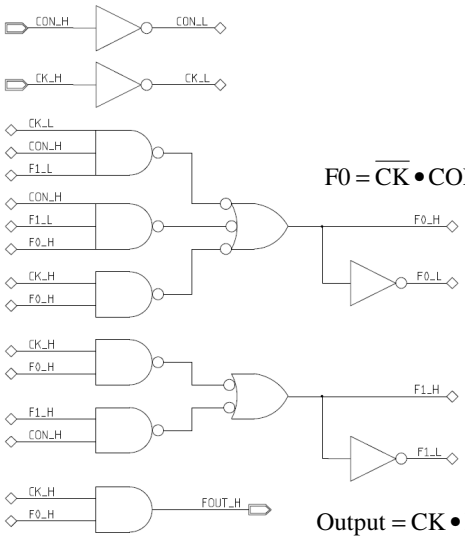


$$CON \bullet (\overline{\overline{CON}} + \overline{F1}) \bullet F0$$

$$CON \bullet \overline{\overline{CON}} \bullet F0 + CON \bullet \overline{F1} \bullet F0$$

$$CON \bullet \overline{F1} \bullet F0$$

And Finally, Generate Equations

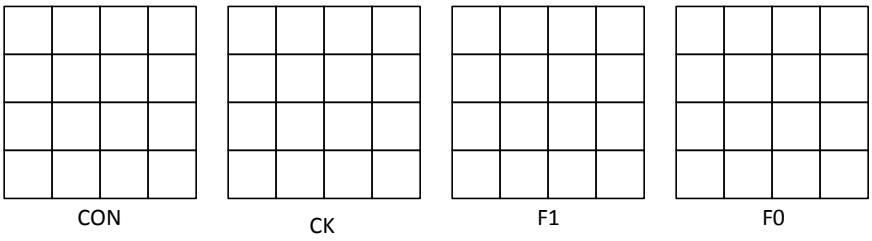


$$F0 = \overline{CK} \bullet CON \bullet \overline{F1} + CON \bullet \overline{F1} \bullet F0 + CK \bullet F0$$

$$F1 = CK \bullet F0 + F1 \bullet CON$$

$$Output = CK \bullet F0$$

From Equations – K-Maps



From Equations – K-Maps

F1: CON \ CK	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	1	1	1
10	0	0	1	1

F1

F0: CON \ CK	00	01	11	10
00	0	0	0	1
01	0	1	1	1
11	0	1	1	0
10	0	0	0	0

F0

Put Maps Together for Final State Table

F1 \ CON CK / F0	00	01	11	10
00	0 0	0 0	0 0	0 1
01	0 0	1 1	1 1	0 1
11	0 0	1 1	1 1	1 0
10	0 0	0 0	1 0	1 0

Identify States in Final State Table

F1 \ CON CK / F0	00	01	11	10
00	A: 0 0	B: 0 0	C: 0 0	0 1
01	0 0	1 1	1 1	D: 0 1
11	0 0	F: 1 1	E: 1 1	1 0
10	0 0	0 0	H: 1 0	G: 1 0

Finish Table with Stable, Unstable States

F1 F0 \ CON CK	00	01	11	10
00	(A)	(B)	(C)	D
01	A		E	(D)
11	A	(F)	(E)	G
10	A	B	(H)	(G)

And Make State Diagram