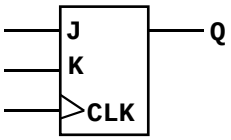
EECE 338 - Fall 2011
Assignment 3
Due at beginning of Final

Consider the following block diagram for a JK flipflop:



Design a gating system that will produce the behavior of a positive edge-triggered JK Flip Flop. That is, the unit should respond according to the JK characteristic table:

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	not Q_n

Changes in the output (Q) should occur only on the rising edge of the clock input. Please follow the following output convention:

$$\frac{J\ K\ CLK}{Q}$$

Your solution should contain whatever definition information you find necessary, a state diagram, a primitive state table, a merge diagram, a final state table, a K-map, the two-level equations, a logic diagram of the final result, and a simulation of the final system.