ECE 322L Spring 2013

Final Lab: Experiment 6

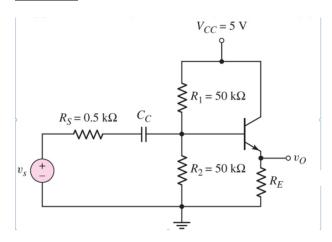
Two stage BJT Amplifier

<u>Purpose:</u> In this Lab we will explorer characteristics of the two stage BJT amplifier. The main purpose of this lab is to see Loading Effect, and how it impacts your circuits gain. Last week we built two different types of BJT amplifiers, this week we will combine the two into a two stage amplifier and explorer how it behaves.

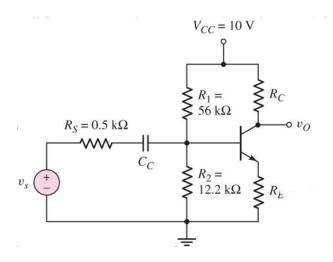
Materials:

Various resistors 2x 2N2222 NPN BJT transistor 2x 0.33 µF capacitors Breadboard

Procedure:



Input Stage



ECE 322L Spring 2013

Gain/Output Stage

• Using the 3-wire curve tracer on your ELVIS boards, find beta for both transistors you are using

- Design the input stage such that Vs = 10 mVpp, R1 = R2 = 50k, Vbe(on) = 0.7V, Icq = .793ma
- Design the output stage such that R1=56k, R2=12.2k , Va = inf, Vbe(on) = 0.7V, Icq = 2.16ma, Vce = 4.81V
- Build the circuit using the common collector amplifier to feed the input of the common emitter, using a .33uF capacitor between the two to isolate DC characteristics from each other. (This means the output of the input stage is the input directly to the gate of the second stage, DO NOT include an RS inbetween the two stages)
- Calculate Av for both stages individually.
- Multiply Av1 and Av2
- Calculate total gain for entire circuit
- Measure AC voltage gain
- Simulate the circuit

Conclusion

- Does Av1 * Av2 match the theoretical voltage gain when both stages are connected together? If not why might this be (hint: I mentioned this in the "Purpose" section
- How does the base current contribute to why Av1 * Av2 does not equate to the overall gain
- What is one way to reduce the Loading Effect?