ECE-344 Final Exam Solutions

1.

Two's Complement Pattern	10011000.10010000	-103.34375
Unsigned Binary Pattern	10011000.10010000	152.5625
Two's Complement Pattern	1011101110000000	24,000
Bit Two's Complement	11111000.10101000	-7.34375
Bit Two's Complement	11010010.01111000	-45 17/32
Unsigned Binary	10101010.10101010	170.664063

2.

a) fundamental principle on which stored program computers are based:

Fetch, decode, execute

b) how is Memory Mapped I/O implemented?

I/O activity is carried out by writing and reading locations in memory.

I/O elements are assigned addresses in the memory space of the processor

c) what instructions move multiple register values to and from memory?

lmw, stmw

d) vector table starts at 0x00100000, ISR is created to handle privilege violations,

where should the ISR be located?

0x00100700

e) give a two instruction sequence to look for the third legal location of interrupt table

lis r3, 0x0002

mtevpr r3

f) why does PowerPC have both a user mode and a privilege mode?

for protection and to manage the resources in the operating system

g) how does the system enter user mode?

Setting PR bit to 1, in the MSR

li r2 0x00010000 mtspr msr r2

h) how far can a branch-to-subroutine go? Assume instruction is at 0x00010000.

0x07fffffc + 0x00010000 = 0x0800fffc

3. registers changed:

r1 = 0x11111118

r2 = 0x00000008

r7 = 0xFFFFFFFF

r9 = 0xBBBBBBBB

r10 = 0x12345678

LR = 0x3008

4. registers changed:

r0 = 0xDDDDDDDD

r3 = 0x54321065

r4 = 0xFFFFFFFF

r13 = 0xFFCCCCCC

r14 = 0x40000400

r15 = 0x0000EFFE

memory changed:

address: 0x4000042c → 99 99 99 99

address: 0x40000432 → 88

5. Interrupt Question #1: Provide code to configure the ML403 as we had in the lab, but fixed so that the only active interrupt is from the UART.

lis r1, 0x83e0

lis r2, 0x80

stw r2, 0x100C(r1) #LCR

li r3, 0x45

```
stw r3, 0x1000(r1) #DLL

li r3, 0x01

stw r3, 0x1004(r1) #DLM

li r3, 0x7

stw r3, 0x100C(r1)

li r3, 0x8

stw r3, 0x1004(r1)

lis r4, 0x8140

li r0, 0

stw r0, 4(r4)

lis r6, 0x8141

stw r0, 4(r6)

lis r7, 0x8142

stw r0, 4(r7)

lis r8, 0x8143

stw r0, 0(r8)

lis r10, 0x8180 #INTC

li r1, 0x3

stw r1, 0xC(r10) #MER

li r1, 0x8

stw r1, 0xC(r10) #IER

li r9, 0xF

stw r9, 0(r10) #ISR

lis r22, 0020

mtevpr r22
```

wrteei 1

b here

6. Interrupt Question #2: deals with steady state activities from Question 5; give code for the ISR for the UART

lis r6, 0x8180 #INTC

lis r5, 0x83e0 #UART

.org 0x500

lwz r1, 0x1000(r5) #load from RBR

lis r2, 0xffff

ori r2, r2, 0x0100

stw r1, 0(r2)

li r3, 0x60

stw r3, 0x1014 #LSR

li r3, 0x8

stw r3, 0xC(r6) #IAR

rfi

7. Provide two sets of instructions, one for the “push” operation and one for the “pop” operation

Push:

.org 0xhe11 (for Mike)

lis r1, 0x2000

stw r3, 0x10(r1)

stw r8, c(r1)

stw r14, 8(r1)

stw r22, 4(r1)

stw r25, 0(r1)

Pop:

```
.org 0x0200
lwz r25, 0(r1)
addi r1, r1, 4
lwz r22, 4(r1)
addi r1, r1, 4
lwz r14, 8(r1)
addi r1, r1, 4
lwz r8, c(r1)
addi r1, r1, 4
lwz r3, 0x10(r1)
```

8.

a) What is the instruction represented by the bit pattern 0x38857342?

addi r4, r5, 0x7342

b) what is the instruction represented by 0x48001511 located at 00004000?

bl 0x1510

0x1510 away from 0x00004000

c) give the coding for the instruction xor. r3, r4, r5

0x7C832A79