Exam 2 - 2

EECE 344

Spring 2010

 Information representation. We gotta have some question about number representation. Consider number system(s) that utilize a single byte - 8 bits, with the radix point right in the middle (xxxx.xxxx). For that arrangement of bits, fill in the missing elements of the following table. (Remember that Maximum is right-most on the number line; minimum is left-most on the number line.)

Value	Unsigned binary bit pattern	Twos-complement bit pattern	0000.101/
Maximum	1111.1111	0111.1111	
Minimum	0000,0000	1000.0000	
11/16	0000.1011	11thator-2	
- <sup>5</sup> / <sub>8</sub>	N/A 0000. [0]0	1111,0110	
123/8	1000:1010	N/A	

77 710

2. General information question:

a) When an interrupt occurs, what happens to the MSR[EE] bit?

b) The EVPR register holds 32 bits. What is the restriction on the contents of this register for normal interrupt operation?

c) Suppose that register R10 contains the value 0x00100000. Is it possible to use this register as a pointer to access the word address 0x000F 88742. If not, why not? If so, what is the offset value used in the load instruction to reach the address?

used in the load instruction to reach the address?

2 No it can't. To offset apointer the max it can offset is extist and exception is forture than on the fram revise valve, yes, 00005786 is there offset.

d) Suppose R10 is as defined in part c, and R11 contains 0x00123456. Give the bit pattern found in the most significant 4 bits of the Condition Register after a cmp 0,0,r10,r11 instruction.

e) The counter register (CTR) is automatically decremented by some conditional branch instructions. However, the user can purposely increment or decrement the value in CTR. What steps need to be taken in order to increment CTR by 0x0100?

mf ctr [3] addi (3), (3), 0x0100 addi (3), (3) Exam 2 - 3

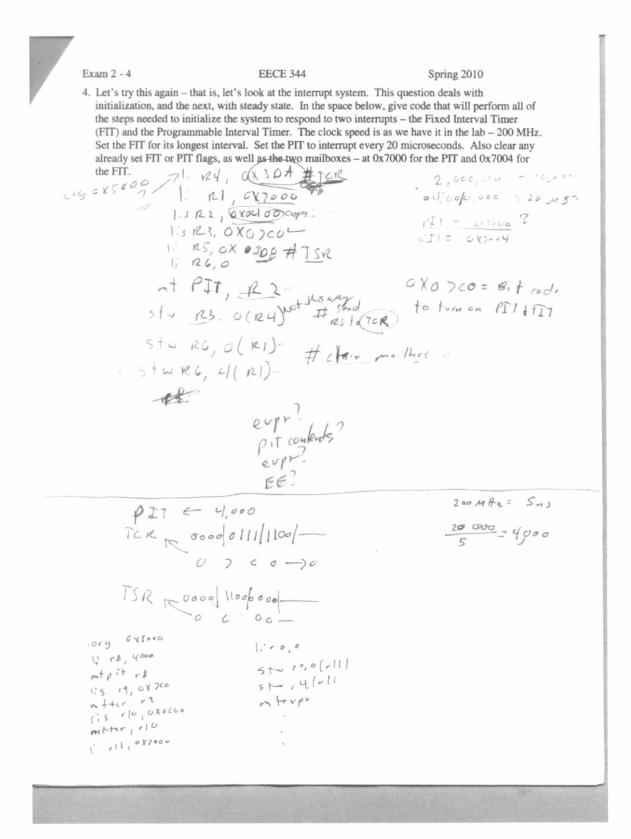
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3. A stack question. Most PPC systems utilize R1 as the stack pointer. And stacks are an accepted method for doing subroutine linkage. In the space provided below, provide code for subroutine linkage using a stack. Be careful with the division of responsibility between calling routines and called routines. Make sure that the method is capable of recursion. Use R31 as the place to locate the return address. Make sure that you use a minimal number of instructions, and that the instruction order is correct.

FML: 6 FML

1000 0x3000	stnu r28,0(1)
hop	bl subrin
nop	1mm 28,0(11)
nop	m flr #31, Ls
melr -31	200
add; 11,-1,-16	n-b
	n i po



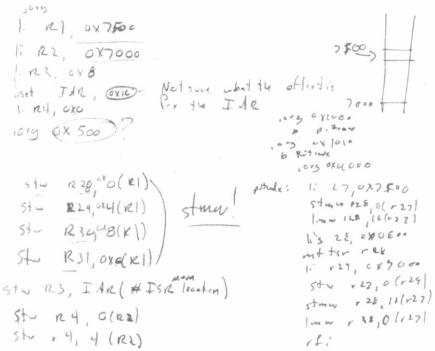
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5. This question is a follow-on to the previous question. The intent is to provide the necessary interrupt service activity to service the two interrupts. The activity is to be the simple model that we used in class. Save current values of R28-R31 going into the ISR and restore at the end of the ISR. The register storage area starts at location 0x7F00. And the activity of the ISR is to reset the appropriate interrupt flag and also set a non-zero mailbox flag. Flag mailboxes are stored in the area starting at 0x7000. The PIT flag is located at 0x7000 and the FIT flag is located at 0x7004.

FIS



sto , 4, 4 (RE)

twe R31, 0xc(R1)

twe R30, 0xe(R1)

twe R20, 0x4(R1)

twe R20, 0x4(R1)

twe R20, 0x4(R1)

fitale: 1: r21, 0 &2 FOO

5tm w r28, 0 (r27)

1mw r28, 0 x0400

nt tor r28

1: r29, 4(r29) 0x 700

5tm r27, 4(r29)

5tm r28, 32(r27)

1mw r28, 32(r27)

1mw r28, 0 (r27)