Homework 3 (Due Date: Thursday, Feb 7th In Class)

An n-channel MOSFET is biased in the saturation region at a constant V_{GS} . (a) The drain current is $I_D=0.250$ mA at $V_{DS}=1.5$ V and $I_D=0.258$ mA at $V_{DS}=3.3$ V. Determine the value of λ and r_o . (b) Using the results of part (a), determine I_D at $V_{DS}=5$ V.

$$I_{D} = K_{\Lambda} (V_{65} - V_{7\Lambda})^{2} (1 + \lambda V_{D5}) \Rightarrow K_{\Lambda} = \frac{I_{D}}{(V_{65} - V_{7\Lambda})^{2} (1 + \lambda V_{D5})}$$

$$0.25 \text{ mA}(1+\lambda(3.3 \text{ V})) = 0.258 \text{ mA}(1+\lambda(1.5 \text{ V}))$$

$$0.25 \text{ mA} + 1825 \text{ m} = 0.258 \text{ mA} + \lambda(387 \text{ M}) = 78 \text{ Bm} = 14138 \text{ M}$$

$$1 = \frac{8 \text{ M}}{438 \text{ m}} = 7 \text{ M} = 0.0183 \text{ V}$$

$$\Gamma_0 = \frac{\Delta U}{\Delta T} \Rightarrow \frac{3.3v - 1.5v}{0.258 \text{ mA} - 0.25 \text{ mA}} \Rightarrow \frac{1.8}{3u} \Rightarrow \Gamma_0 = 225 \text{ KJZ}$$

$$\begin{array}{lll} (1) & 0.258 \text{ mA} = \text{Kn} \left(\text{VGS} - \text{VTN} \right)^2 \left(1 + \lambda \text{ VPS} \right) = \text{Kn} \left(\text{VGS} - \text{VTN} \right)^2 = \frac{0.258 \text{mA}}{1 + 3.3 \left(0.0183 \right)} \\ = \text{70.243 m} = \text{Kn} \left(\text{VGS} - \text{VTN} \right)^2 \end{array}$$

The circuit shown in Figure 4.1 has parameters $V_{DD}=2.5~{\rm V}$ and $R_D=10~{\rm k}\,\Omega$. The transistor is biased at $I_{DQ}=0.12~{\rm mA}$. The transistor parameters are $V_{TN}=0.3~{\rm V}$, $k_n'=100~\mu~{\rm A/V}^2$, and $\lambda=0$. (a) Design the W/L ratio of the transistor such that the small-signal voltage gain is $A_\nu=-3.8$. (b) Repeat part (a) for $A_\nu=-5.0$.

a)
$$V_0 = 2.5V - 0.12 \text{ A}(10K) =) V_0 = 1.3V$$

$$A_V = -3.8 = V_0$$

$$1.3 \boxed{)} -0.342 \cdot -0.3V \qquad \underline{sat}$$

$$0.12 \text{ A} = \frac{100 \text{ A}}{100 \text{ A}} \left(\frac{100}{2}\right) \left(-0.342 - 0.3V\right)^2$$

$$\frac{100 \text{ A}}{100 \text{ A}} \left(\frac{100}{2}\right) \left(-0.042\right)^2 \Rightarrow \boxed{\frac{1000 \text{ A}}{1000 \text{ A}} \left(\frac{100}{2}\right)}$$

b)

$$A_{V} = -5.0 = \frac{V_{0}}{V_{0}^{2}} \Rightarrow V_{0} = \frac{1.3V}{-5} \Rightarrow V_{0} = -0.26 = V_{05}$$

$$1.3 \left[\sum_{i=0.26} -0.26 - 0.3 \right] = 5at$$

$$0.12mA = 100mt (12) (0.26 - 0.3)^{2}$$

$$\frac{W}{L} = \frac{0.12mA(2)}{109mt(-0.56)^{2}} \Rightarrow \left[\frac{W}{L} = \frac{7.653}{109mt(-0.56)^{2}} \right]$$

Consider the circuit in Figure 4.14 in the text. The circuit parameters are $V_{DD}=3.3$ V, $R_D=8$ k Ω , $R_1=240$ k Ω , $R_2=60$ k Ω , and $R_{Si}=2$ k Ω . The transistor parameters are $V_{TN}=0.4$ V, $k_n=100$ μ A/V², W/L=80, and $\lambda=0.02$ V⁻¹. (a) Determine the quiescent values I_{DQ} and V_{DSQ} . (b) Find the small-signal parameters g_m and r_o . (c) Determine the small-signal voltage gain.

$$V_{GS} = 3.3 \cdot \left(\frac{V_{GS}}{V_{GN} + 240K}\right) \Rightarrow V_{GS} = 0.660V$$

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$$V_{DG} = \frac{100 \text{ M}}{2} \left(30\right) \left(0.00 - 0.4\right)^2 \Rightarrow \left[\text{Ip}_{Q} = 270.4 \text{ M}\right]$$

$$V_{DG} = 3.3 \cdot -270.4 \text{ M}\left(3k\right) \Rightarrow V_{DSQ} = 1.1363 \text{ V}$$

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$$V_{DS} = 2 \cdot \text{Im} \cdot \text{Ip}_{Q} \qquad K_{N} = \frac{K_{N}^{1}}{2} \left(\frac{8k}{k}\right) = \frac{100 \text{ M}}{2} \left(\frac{90}{2}\right) = K_{N} = 4M$$

$$g_{M} = 2 \cdot \text{Im} \cdot \left(\frac{270.4 \text{ M}}{2}\right) = \frac{3m}{2} \cdot \frac{2.03 \text{ m} \text{ My}}{2}$$

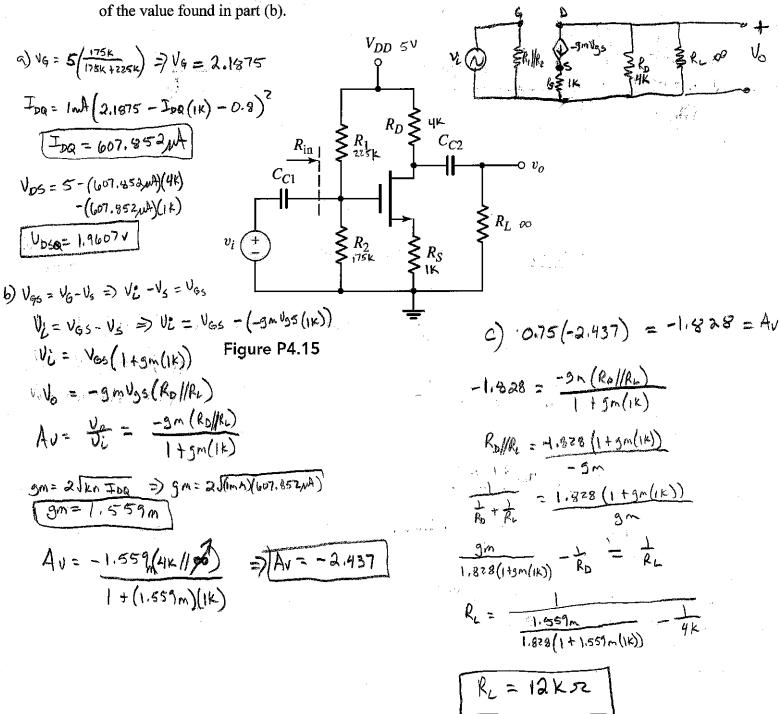
$$f_{0} = \frac{1}{\lambda} \frac{1}{100} \Rightarrow \frac{3}{0.005} \left(\frac{270.4 \text{ M}}{2}\right) \Rightarrow \frac{7}{0.005} \left(\frac{81/182}{86k + 81/182}\right)$$

$$V_{0} = -9 \text{ m} \cdot V_{0} \cdot \left(\frac{81/182}{8k + 81/182}\right) \left(\frac{80/182}{8k + 81/182}\right) \left(\frac{80$$

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For the NMOS common-source amplifier in Figure P4.15, the transistor parameters are: $V_{TN}=0.8~\rm{V},~K_n=1~\rm{mA/V}^2$, and $\lambda=0$. The circuit parameters are $V_{DD}=5~\rm{V},~R_S=1~\rm{k}\Omega$, $R_D=4~\rm{k}\Omega$, $R_1=225~\rm{k}\Omega$, and $R_2=175~\rm{k}\Omega$. (a) Calculate the quiescent values I_{DQ} and V_{DSQ} . (b) Determine the small-signal voltage gain for $R_L=\infty$.

(c) Determine the value of R_L that will reduce the small-signal voltage gain to 75 percent of the value found in part (b).



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Consider the ac equivalent circuit shown in Figure P4.18. Assume $r_o = \infty$ for the transistor. The small-signal voltage gain is $A_v = -8$ for the case when $R_S = 1$ k Ω .

(a) When R_S is shorted ($R_S = 0$), the magnitude of the voltage gain doubles. Assuming the small-signal transistor parameters do not change, what are the values of g_m and R_D ? (b) A new value of R_S is inserted into the circuit and the voltage gain becomes $A_v = -10$. Using the results of part (a), determine the value of R_S .

