EECE 238 Exam II

Name: Solutions

Problem 1	30 /30
Problem 2	30 /30
Problem 3	15 /15
Problem 4	25 /25
Total:	100 /100

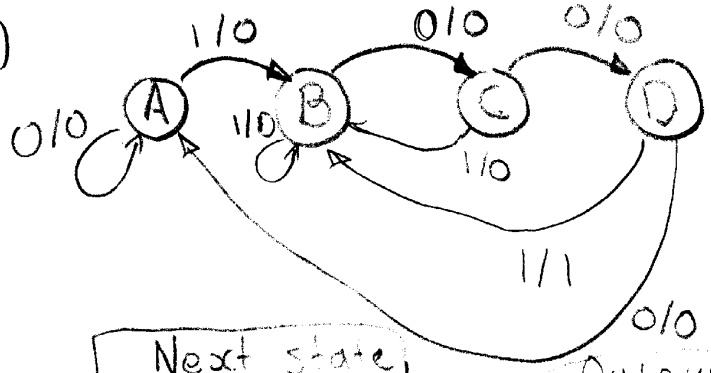
Good Luck!

Problem 1 (30 points total) *Sequence Recognizer Design.*

Design a digital circuit to recognize the occurrence of the input sequence 1001. The circuit will output a 1 when the previous inputs were 100 and the current input is 1. Note that since the output depends on the input (as well as the current state), you need a ***Mealy*** solution to this problem.

1 (a) (12 points) Derive the state transition diagram.
1 (b) (10 points) Derive the state table and Flip-Flop inputs for J-K Flip-Flops.
1 (c) (5 points) Use Karnaugh maps to minimize the equations for the Flip-Flop inputs, and the output.
1 (d) (3 points) Draw the final circuit.

1(a)



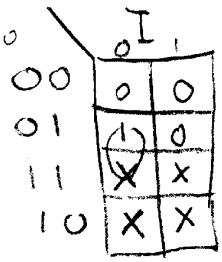
A: no is received
B: ending in 1
C: ending in 10
D: ending in 100

1(b)

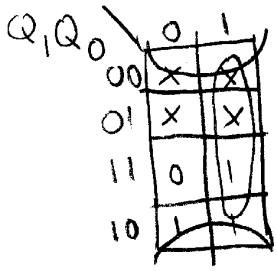
current	Next state I=0	Next state I=1	Output I=0	Output I=1	I=0 J_1K_1	I=0 J_0K_0	I=1 J_1K_1	I=1 J_0K_0
A: 00	A:00	B:01	0	0	0X	0X	0X	1X
B: 01	C:11	B:01	0	0	1X	X0	0X	X0
C: 11	D:10	B:01	0	0	X0	X1	X1	X0
D: 10	A:00	B:01	0	1	X1	0X	X1	1X

Q(t)	Q(t+1)	J K
0	0	0 X
0	1	1 X
1	0	X 1
1	1	X 0

1(c)

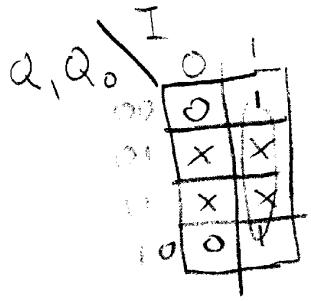


$J_1 = I'Q_0$

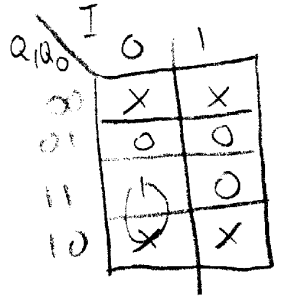


$K_1 = I + Q_0'$

Output $= Q_1Q_0'I$

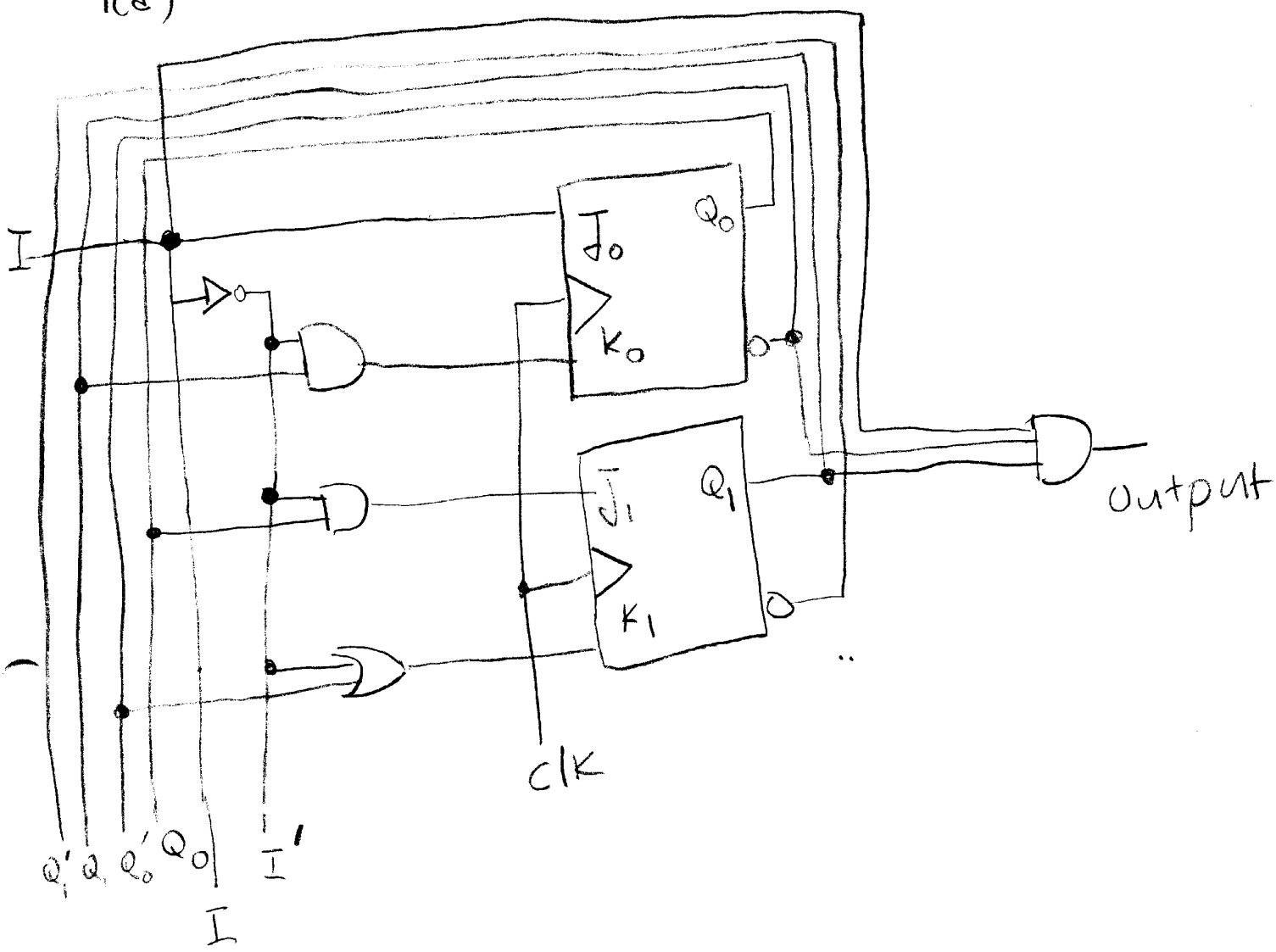


$J_0 = I$



$K_0 = I'Q_1$

1(d)

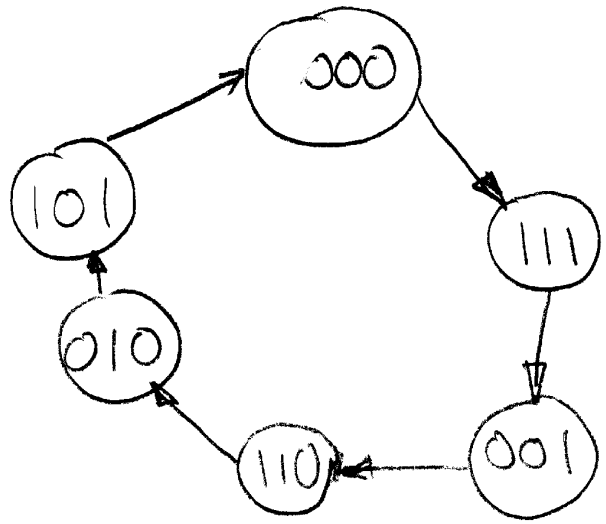


Problem 2 (30 points total) *Synchronous Counter Design.*

Design a binary counter that counts through the 3-bit binary numbers: 000, 111, 001, 110, 010, 101, and then repeat from 000. For your design, assume that **there is** a reset signal that will force counting to start at 0. Assume that the states codes are assigned unsigned integer representations.

2 (a) (10 points) Draw the state transition diagram.
2 (b) (10 points) Derive the state table for implementing the counter using J-K Flip-Flops.
2 (c) (5 points) Use K-maps to minimize the inputs to the J-K Flip-Flops.
2 (d) (5 points) Indicate the final circuit.

2(a)



Q(t)	Q(t+1)	J K
0	0	0X
0	1	1X
1	0	X1
1	1	X0

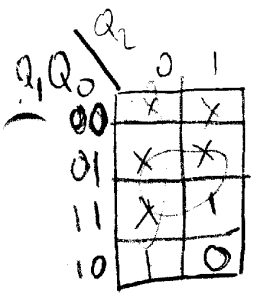
2(b)

$Q_2Q_1Q_0$ Present state	Next state	J_2K_2	J_1K_1	J_0K_0
000	111	1X	1X	1X
001	110	1X	1X	X1
010	101	1X	X1	1X
011	XXX	XX	XX	XX
100	XXX	XX	XX	XX
101	000	X1	0X	X1
110	010	X1	X0	0X
111	001	X1	X1	X0

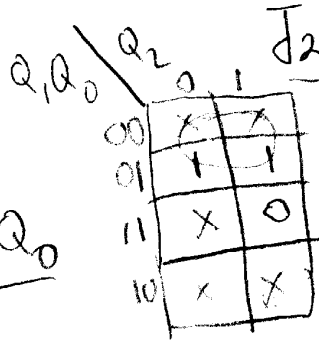
$J_2 = K_2 = 1$

$J_1 = Q_2'$

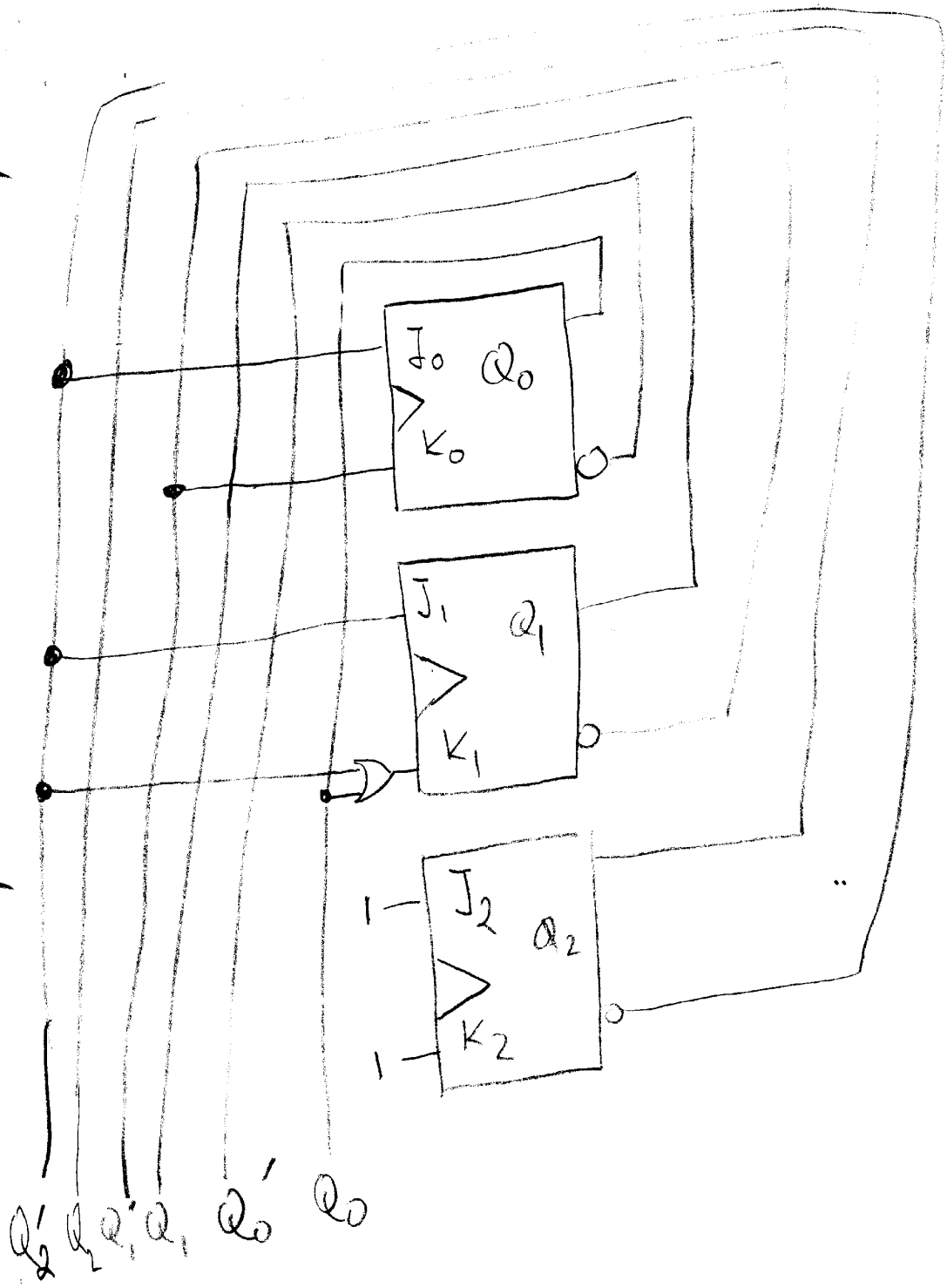
$J_0 = Q_2'$



$K_1 = Q_2' + Q_0$



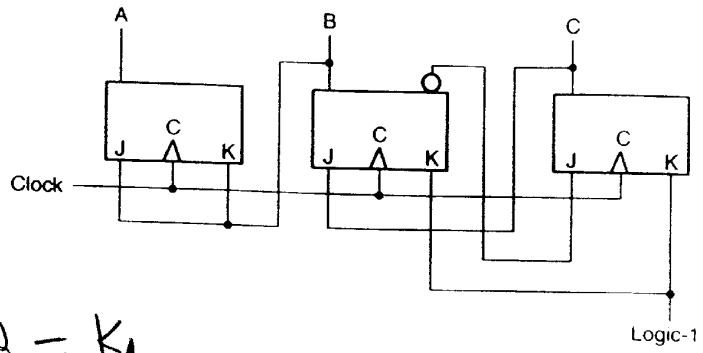
$K_0 = Q_1'$


J_0 Q_0
K_0
J_1 Q_1
K_1
1
J_2 Q_2
K_2
1
Q_2' Q_2 Q_1' Q_1 Q_0' Q_0

Problem 3 (15 points total) *Sequential Circuit Analysis I*

Consider the sequential circuit given below. We would like to analyze the circuit and understand what it does.

3 (a) (5 points) Derive the J-K flip-flop input equations.
3 (b) (7 points) Derive the next-state table based on 3(a).
3 (c) (3 points) Derive the state-diagram based on the next-state table.



3(a) $J_A = B = K_A$

$J_B = C$

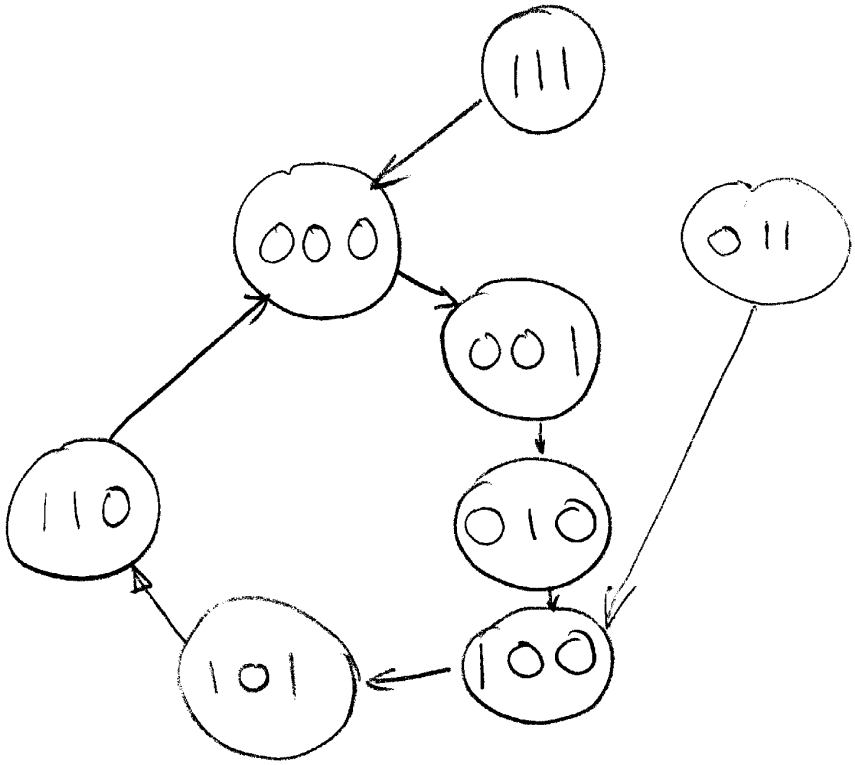
$K_B = 1$

$J_C = B'$

$K_C = 1$

3(b)

Present state ABC	J_A K_A	J_B K_B	J_C K_C	Next state
000	0 0	0 1	1 1	0 0 1
001	0 0	1 1	1 1	0 1 0
010	1 1	0 1	0 1	0 1 1
011	1 1	1 1	0 1	1 0 0
100	0 0	0 1	1 1	1 0 1
101	0 0	1 1	1 1	1 1 0
110	1 1	0 1	0 1	0 0 0
111	1 1	1 1	0 1	0 0 0

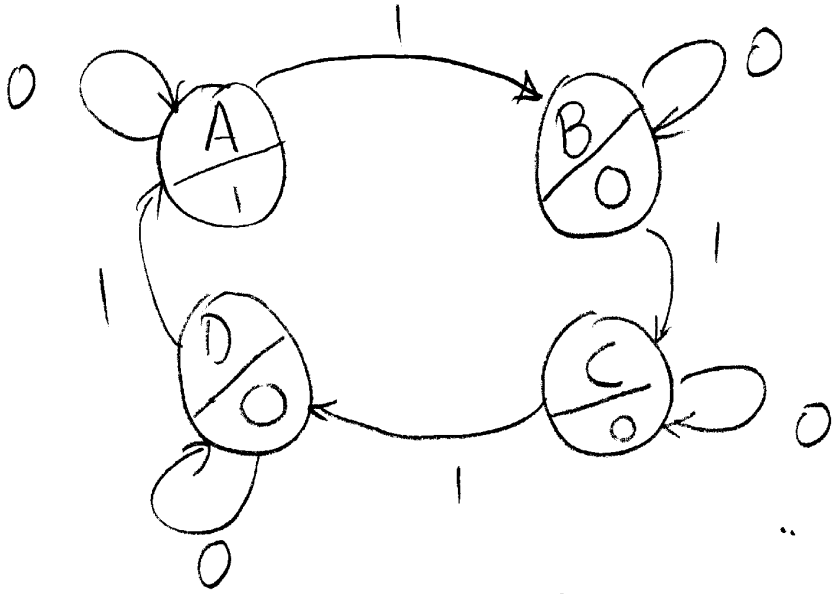

111
000
011
001
110
010
101
100

Problem 4 (25 points total) *Modulo-4 Parity Detector*

Using T Flip-Flops, design an even parity detector that outputs a 1 **after** a multiple of 4 1s have been received. Note that since the output does not depend on the current input, you will need a ***Moore*** solution to this problem. Also, assume that zero is a multiple of 4 (0=0*4).

4 (a) (10 points) Derive the state transition diagram.
4 (b) (10 points) Derive the state table and S-R flip-flop inputs.
4 (c) (5 points) Indicate the final Circuit using S-R flip-flops.

4(a)

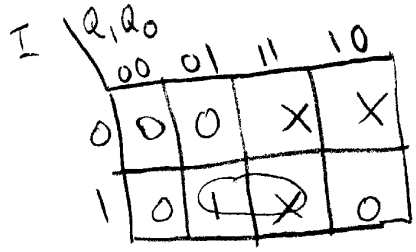


4(b) For S-R F.F.:

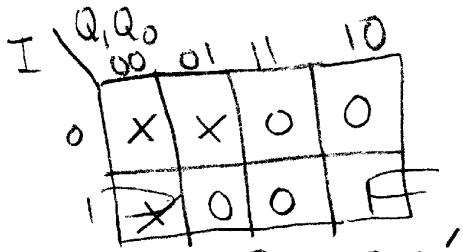
Q(t) → Q(t+1)		S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$O = Q_1' Q_0'$

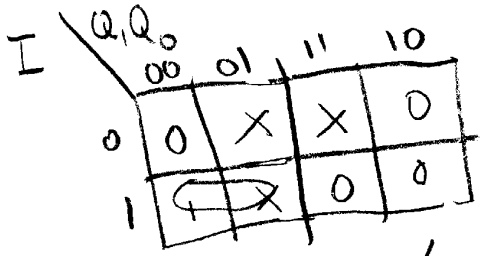
Present State (Q_1Q_0)	I	Next State	S_1R_1	S_0R_0
A 00	0	A 00	0X	0X
00	1	B 01	0X	10
B 01	0	B 01	0X	X0
01	1	C 11	10	X0
C 11	0	C 11	X0	X0
11	1	D 10	X0	01
D 10	0	D 10	X0	0X
10	1	A 00	01	0X



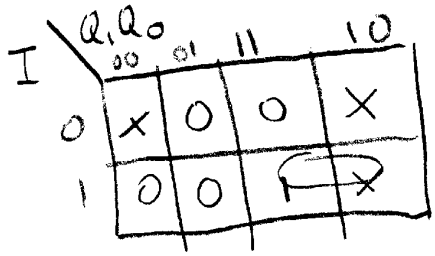
$S_1 = I Q_0$



$R_1 = I Q_0'$

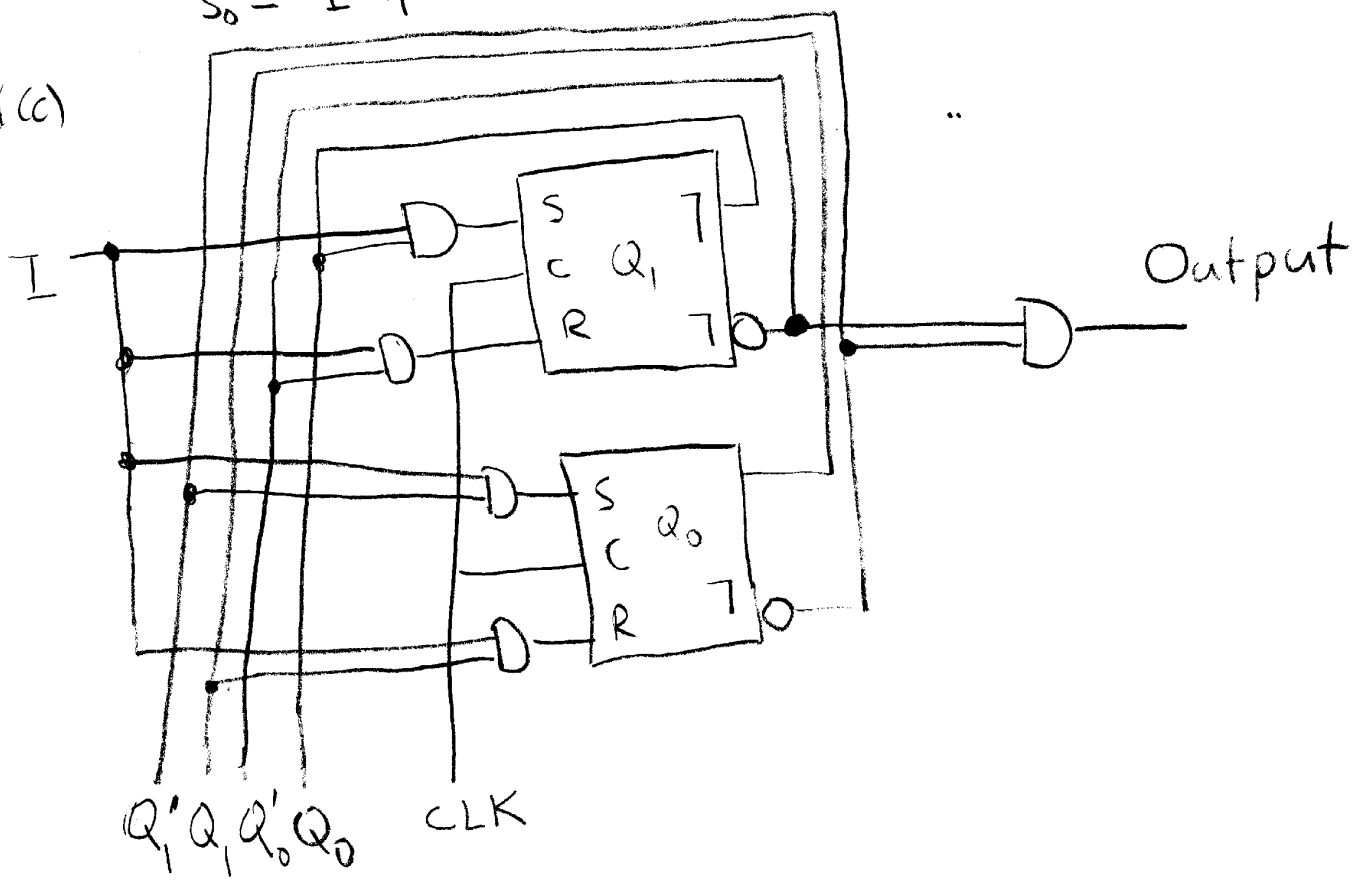


$S_0 = I Q_1'$



$R_0 = I Q_1$

4(c)



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Name:

Problem 1	**_____/25**
Problem 2	**_____/25**
Problem 3	**_____/30**
Problem 4	**_____/20**
Total:	**_____/100**

Good Luck!

Problem 1 (25 points total) *Counter with Parallel Load*

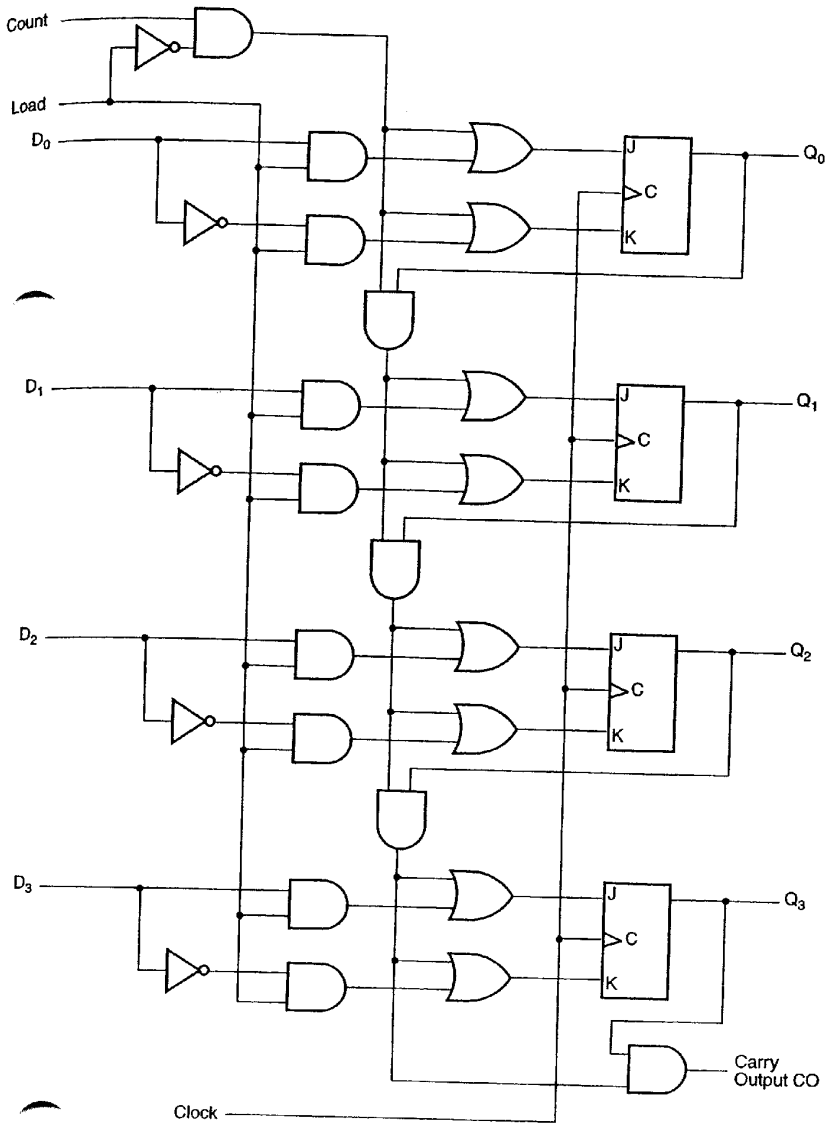
The digital logic circuit below represents a 4-Bit Binary Counter with Parallel Load. Assume that originally, all the D Flip-Flops store 0: $D_3D_2D_1D_0 = 0000$.

1(a) (5 points) Indicate how to make the counter count. How should you connect the inputs?

The following steps are used to make the counter count from 2 to 5. ***For full-credit in parts 1(b) and 1(c),, you must show the clock input, all the affected inputs (possible inputs are:*** D_0, D_1, D_2, D_3, Load, and Count***), and all the outputs:*** Q_0, Q_1, Q_2, Q_3.

1(b) (5 points) Indicate how to load 2 into the counter.

1(c) (15 points) Show how to make the counter count to 5, and **then stop**.



Problem 2 (25 points total) *Synchronous Counter Design.*

Design a binary counter that counts through the 3-bit binary numbers: 000, 001, 010, 100, and then repeat from 000. For your design, assume that **there is** a reset signal that will force counting to start at 000. Assume that the states codes are assigned unsigned integer representations.

2 (a) (5 points) Draw the state transition diagram.
2 (b) (10 points) Derive the state table for implementing the counter using S-R Flip-Flops.
2 (c) (5 points) Use K-maps to minimize the inputs to the S-R Flip-Flops.
2 (d) (5 points) Indicate the final circuit.

Problem 3 (30 points total) Sequential Circuit Design

Design a digital circuit to recognize the occurrence of the input sequence 0110. The circuit will output a 1 when the previous inputs were 011 and the current input is 0. Note that since the output depends on the input (as well as the current state), you need a ***Mealy*** solution to this problem.

3 (a) (10 points) Derive the state transition diagram.
3 (b) (10 points) Derive the state table and Flip-Flop inputs for J-K Flip-Flops.
3 (c) (5 points) Use Karnaugh maps to minimize the equations for the Flip-Flop inputs, and the output.
3 (d) (5 point) Draw the final circuit.

Problem 4 (20 points total) *Sequential Circuit Analysis*

Consider the sequential circuit given below. We would like to analyze the circuit and understand what it does.

4 (a) (5 points) Derive the T flip-flop input equations.
4 (b) (5 points) Derive the next-state table based on (a).
4 (c) (5 points) Derive the state-diagram based on the next-state table.
4 (d) (5 points) What does this circuit do?