

Power and Delay Analysis of a 2-to-1 Multiplexer Implemented in Multiple Logic Styles for Multiplexer-Based Decoder in Flash ADC

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Abstract— Thermometer - to - Binary decoders has become bottleneck in the ultra-high speed flash ADCs. Among various types of decoders available multiplexer-based decoder requires less hardware, has more regular structure and shorter critical path. A 2-to-1 multiplexer is the leaf cell in the decoder. In this paper the authors have analyzed a 2-to-1 multiplexer circuit using complementary CMOS, dynamic and pass-transistor logic styles. The power consumption, delay, area and power-delay product of various logic styles are compared. This paper shows that 2T multiplexer is an optimum device level design which has characteristics of high speed with minimum power compared with other realizations.

Index Terms— Thermometer code, Flash ADC, CPL, EEPL, LEAP.

I. INTRODUCTION.

Flash Analog-to-Digital Converter (ADC) architecture is mainly known for its high-speed conversion rate. It consumes more power and occupies large chip area when compared with other types of ADCs [1]. In Flash ADC the input signal is applied to the inputs of 2^N-1 comparators, where N is the number of bits. Each comparator is connected to a reference voltage commonly generated by a resistive ladder. The output of comparator is high if the input voltage is larger than the reference voltage at the input of the comparator, otherwise the output is low. Hence the output pattern corresponds to thermometer code. This code is generally decoded to binary code by using (2^N-1) -to-N Decoder. A variety of decoders have been reported in literature [2] [3] [4]. Among them multiplexer-based decoder has regular structure requires less hardware and has a shorter critical path than any other decoder and gives bubble error suppression. It consists entirely of 2-to-1 multiplexers.

Thus this paper analyzes 2-to-1 multiplexer using complementary CMOS, dynamic and pass-transistor logic styles. These implementations are compared based on transistor count, power dissipation, delay and power-delay product.

The rest of the paper is organized as follows: In section II, we present the architecture of multiplexer-based thermometer code to binary code (TC-to-BC) decoder and basic idea of a 2-to-1 multiplexer. Section III gives the design of 2-to-1 multiplexer using complementary CMOS, dynamic and pass-transistor logic style. Results of quantitative comparisons based on simulations of different logic styles are given in section IV. Some conclusions are drawn in section V.

II. ARCHITECTURE OF MULTIPLEXER-BASED TC-to-BC DECODER

Multiplexer-based TC-to-BC decoder is based on 2-to-1 multiplexers connected as a tree. Each level of the tree divides the input thermometer scale into two and calculates one of the bits in the binary output. The most significant bit (MSB) of the decoder output is equal to the middle digit in the thermometer code [4]. The second highest bit is found in the same way, but only considering a part of the whole thermometer code. The lower half if the middle digit is zero, otherwise the upper half. This is continued until all output bits are found. The 3-bit multiplexer-based decoder scheme is illustrated in Fig.1. Due to its regular structure it can easily be expanded to operate in a system of higher resolution than 3-bits. The amount of hardware is also reduced, which will translate to power saving, compared with all other decoders.

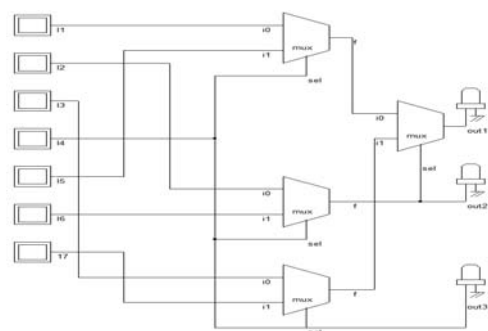


Fig.1. Multiplexer-based decoder for N=3 bits

MULTIPLEXER CIRCUIT:

A circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of one or more control inputs is called “multiplexer”. A multiplexer with two data inputs is referred as “2-to-1 or 2:1” multiplexer. Commonly used circuit and graphical symbol for 2:1 multiplexer is shown in Fig.2.

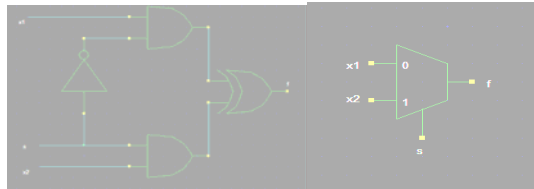


Fig.2. Circuit and Graphical symbol of 2:1 Multiplexer

Logic expression for multiplexer output is given below.

$$F = \bar{S} x_1 + S x_2 \quad (1)$$

III. LOGIC STYLES

A logic style is the way how a logic function is constructed from a set of transistors. It influences the speed, size, power dissipation and wiring complexity of a circuit. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.

A. Complementary CMOS Logic style: Any logic function in complementary CMOS is realized by NMOS pull-down and PMOS pull-up networks connected between gate, output and power lines [5]. Input signals are connected to transistor gates only. Pseudo nMOS and Cascode Voltage Switch Logic (CVSL) fall under CMOS ratioed logic family.

B. Dynamic Logic style: The operation of dynamic logic is based on storage of charge on capacitive node [6]. These are fastest, have zero static power dissipation and are sensitive to noise. Domino logic and Dual rail Domino fall under this category.

C. Pass-transistor Logic style: The pass-transistor logic reduces the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation. Several pass-transistor logic styles [6] Complementary Pass Transistor Logic (CPL)[6], Energy Economized Pass Transistor Logic (EEPL)[6], Differential Cascode Voltage Switch logic with Pass gate (DCVSPG), Swing restored pass-transistor logic (SRPL)[6], Double pass-transistor logic (DPL), CMOS Transmission gate[6], Push-pull Pass Transistor Logic (PPL), LEAN Integrated pass gate logic (LEAP) and 2T Multiplexer are considered to implement 2-to-1 multiplexer.

Among all these 2T Multiplexer is optimal. It uses one pMOS and one nMOS transistor and these two-pass transistors at the input select which signal to propagate. The logic levels will be deteriorated by the pass

transistor. The threshold voltage of both pass-transistors should be identical for accurate operation. Fig.3 represents implementation of 2-to-1 multiplexer using several logic styles.

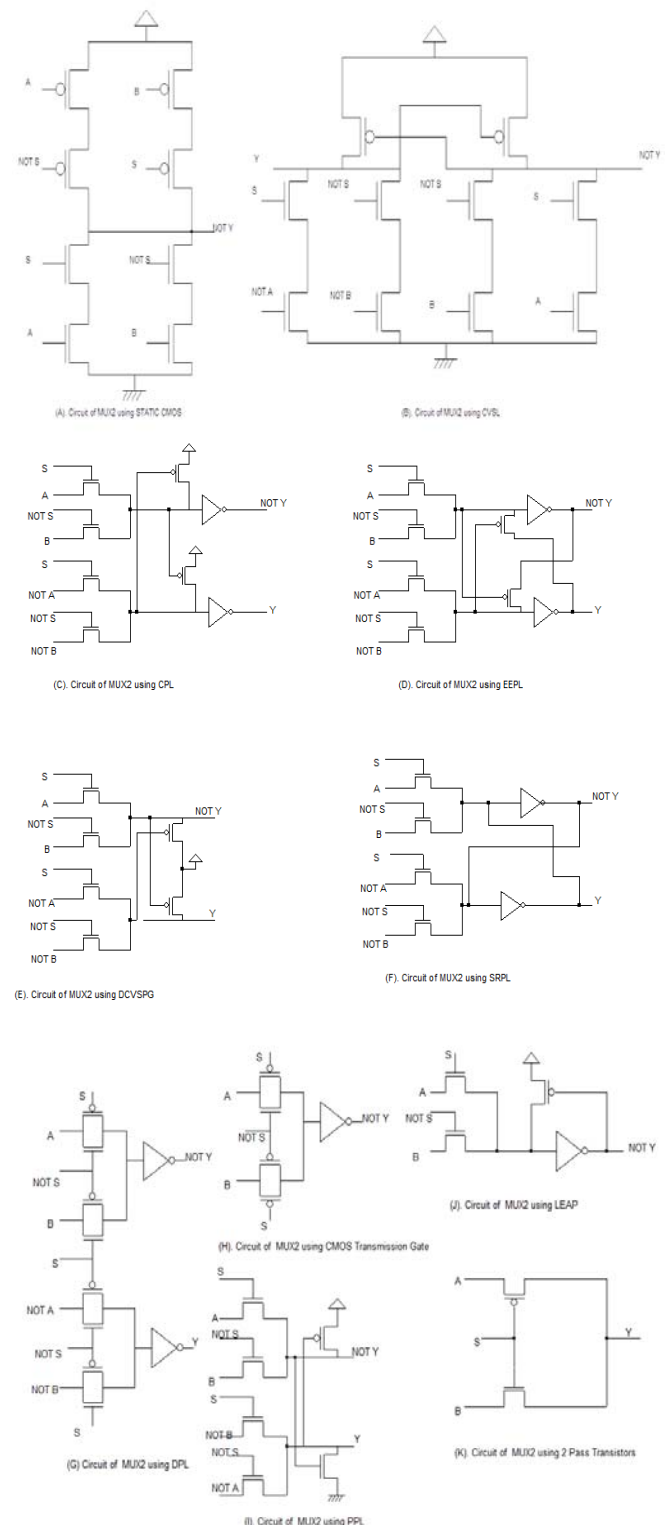


Fig.3. 2-to-1 multiplexer in (a) Static CMOS. (b) CVSL (c) CPL. (d) EEPL. (e) DCVSPG. (f) SRPL (g) DPL. (h) CMOS TG. (i) PPL. (j) LEAP. (k) 2T MUX

IV. SIMULATION

All the simulations have been done using Tanner tools. All the schematics are drawn using 0.18- μ m technology with a 1.8V supply voltage. The calculation of power, delay and power-delay product are carried out for 2-to-1 multiplexer in Static CMOS, CVSL, 2TMux (pass-transistors), CMOS transmission gate, CPL, DCVSPG, DPL, EEPL, PPL, SRPL and LEAP logic styles.

To establish an impartial testing environment, simulations have been carried out using a comprehensive input signal pattern which covers every transition possible for a multiplexer. The domino logic, dual rail domino and pseudo nMOS logic style realizations are done but they are not included in plots because they span in large magnitudes. Frequencies have been chosen in the range from 50 to 200MHz. The power dissipated by multiplexer at various frequencies is plotted in Fig.4.

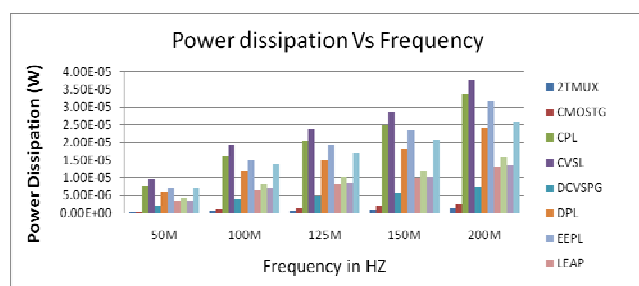


Fig.4. Power dissipation Vs Frequency plot for 2-to-1 multiplexer in multiple logic styles

Also, five different loads (300fF, 250 fF, 150 fF, 100 fF and 50 fF) have been inserted to the output port. The delay at these loads is plotted in Fig.5. Power-delay product for various loads is computed and is plotted in Fig.6. Logic styles based on count of transistors needed to implement 2-to-1 multiplexer are plotted in Fig.7.

V.CONCLUSION

Static CMOS performs much better than pass-transistor logic styles if low power is of concern. Pass-transistor logic has proved to be an attractive alternative to static CMOS design with respect to area, performance and power consumption. Among all pass-transistor logic styles considered 2T multiplexer is having few transistor counts. The advantage of having the same functionality with very few transistors and of small input capacitance in 2T pass-transistor logic will be beneficial in multiplexer realization for TC-to-BC decoder. The pass-transistor has loss of logic level but it can be compensated by using buffers at intermediate places in decoder stages. Thus 2T multiplexer is suitable for multiplexer-based decoder implementation which is characterized by high speed with minimum power compared with all other realizations. As the logic in Flash ADC is complex, by using this multiplexer we can compensate the area on the chip and simultaneously achieving the speed.

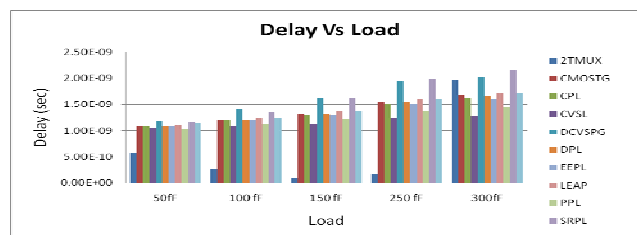


Fig.5. Delay Vs Load plot for 2-to-1 multiplexer in multiple logic styles

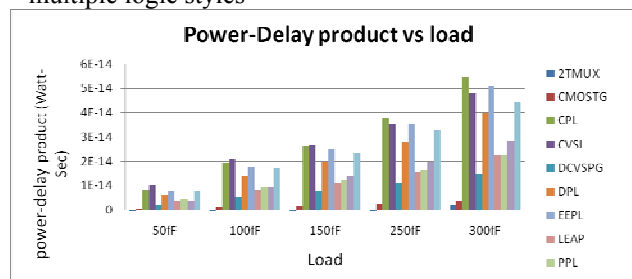


Fig.6. Power-delay product Vs. Load plot for 2-to-1 multiplexer in multiple logic styles

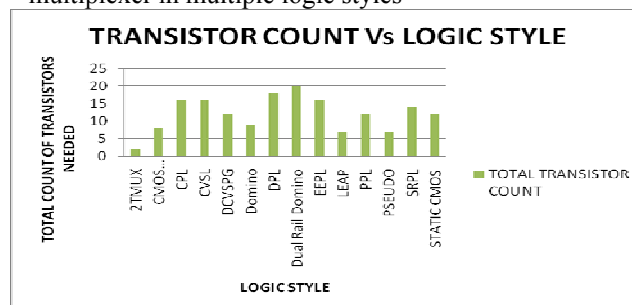


Fig.7. Logic style Vs Total count of transistors needed for 2-to-1 multiplexer

REFERENCES

- [1] R. J. Van de Plassche, *Integrated Analog- to- Digital and Digital- to-Analog Converters*, Kluwer Academic Publishers, 1994.
- [2] F. Kaess, R. Kanan, B. Hochet and M. Declercq, "New encoding scheme for high-speed flash ADC's," *IEEE Proc. Circuits and Syst.*, vol. 1, pp. 5-8, June 1997.
- [3] E. Säll, M. Vesterbacka and K.O. Andersson, "A study of digital decoders in flash analog-to-digital converters," *IEEE Int. Symp. Circuits Syst.*, Vancouver, Canada, May 23-26, 2004.
- [4] E.Sall and M.Vesterbacka, "Comparison of two thermometer-to-binary decoders for high-performance flash ADCs," *Proceedings of IEEE Norchip Conference*, Nov. 2005.
- [5] Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design perspective," 2nd Edition, Prentice-Hall, Inc.
- [6] Neil H.E. Weste, David Harris and Ayan Banerjee, *CMOS VLSI Design, A circuits and system perspective*, 3rd Edition, Pearson Education, 2005.