University of New Mexico
Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2012) Exam 2

Name: Answers Date: Nov. 12, 2012

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) True or false:

(a) It is always desirable to have a small noise margin. (F)

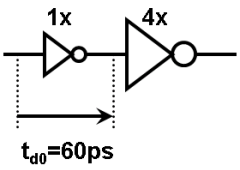
(b) To decrease t_{pHL}, the NMOS threshold voltage must be decreases. (T)

(c) When the input of a CMOS inverter is low, the leakage current will be determined by I_{OFF} of PMOS. (F)

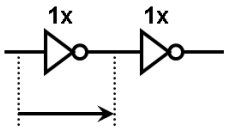
(d) In a CMOS inverter, the slower input rise time results in lower short-circuit power. (F)

(e) A 10% reduction in power supply voltage reduces the dynamic power dissipation by about 20%. (T)

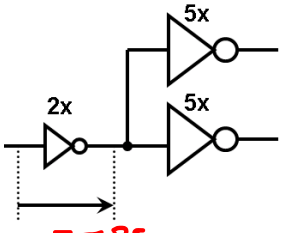
2. (15 points) Given the delay of a standard fanout-4 delay is 50ps (i.e. 1x inverter driving a 4x inverter), determine the delay in each of the following cases:



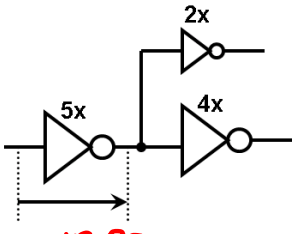
t_{d0}=60ps



t_{d0}= 15 ps



t_{d0}=75 ps



t_{d0}=18 ps

3. (10 points) Determine the $(W/L)_p$ of the PMOS transistor in a CMOS inverter such that the switching threshold voltage, V_M, becomes exactly $V_{DD}/2$. Assume that $K'_n=120uA/V^2$, $Vt_n=0.3V$, $\lambda_n=0.01V^{-1}$, $(W/L)_n=10$, $K'_p=50uA/V^2$, $Vt_p=-0.4V$, $\lambda_p=-0.02V^{-1}$ and $V_{DD}=1.2V$. Include the channel length modulation effect into your calculation.

$$\left(\frac{W}{L}\right)_p = 53.68$$

4. (10 points) Calculate the short circuit current, I_{DDMax}, in the CMOS inverter of problem 3. Again, include the channel length modulation effect into your calculation.

$$I_{DDmax} = 54.324\ ^{MA}$$

5. (10 points) Using the slope of VTC curve (equation g below) determine V_{IL} and V_{IH} of the CMOS inverter in problem 3.

$$g = \frac{-2}{\lambda_n + |\lambda_p|}\left(\frac{1}{V_M - V_{Tn}} + \frac{1}{V_{DD} - V_M - |V_{Tp}|}\right)$$

$g = -555.55$

$V_{IL} = 0.5989$ V

$V_{IH} = 0.601$ V

6. (10 points) From the V_{IL} and V_{IH} found in Problem 5, determine the low and high noise margin of the CMOS inverter.

$NML = NMH = 0.5989$ V

7. (15 points) The output of the CMOS inverter in problem 3 is connected to a 100fF load capacitor. Use the average current technique to find high-to-low propagation delay, t_{pHL}. Include the channel length modulation effect only in saturation region, not in linear region.

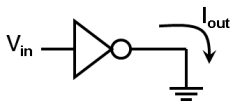
$I_{av} = 461.916\ \mu A$

$t_{PHL} = 129.89\ PF$

8. (10 points) Determine the dynamic power consumption in the CMOS inverter of problem 7, if a square wave pulse running at 1GHz frequency is applied to its input.

$P_D = 144\ \mu W$

9. (10 points) The output of the CMOS inverter in problem 3 has been connected to a defective load which is a short circuit to GND (see figure below). Determine the output current, I_{out}, when the input voltage, V_{in}, is zero and V_{DD}.



$V_{in} = 0 \Rightarrow I_{out} = 879.5\ \mu A$

$V_{in} = V_{DD} \Rightarrow I_{out} = 0$