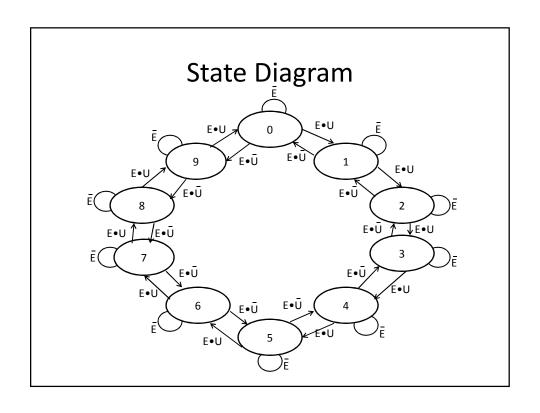
# Design of an Up/Down Decade Counter



Enable	Up	Count	Next
0	0	0000	0000
0	0	0001	0001
0	0	0010	0010
0	0	0011	0011
0	0	0100	0100
0	0	0101	0101
0	0	0110	0110
0	0	0111	0111
0	0	1000	1000
0	0	1001	1001
0	0	1010	XXXX
0	0	1011	XXXX
0	0	1100	XXXX
0	0	1101	XXXX
0	0	1110	XXXX
0	0	1111	XXXX

Enable	Up	Count	Next
0	1	0000	0000
0	1	0001	0001
0	1	0010	0010
0	1	0011	0011
0	1	0100	0100
0	1	0101	0101
0	1	0110	0110
0	1	0111	0111
0	1	1000	1000
0	1	1001	1001
0	1	1010	XXXX
0	1	1011	XXXX
0	1	1100	XXXX
0	1	1101	XXXX
0	1	1110	XXXX
0	1	1111	XXXX

Enable	Up	Count	Next
1	0	0000	1001
1	0	0001	0000
1	0	0010	0001
1	0	0011	0010
1	0	0100	0011
1	0	0101	0100
1	0	0110	0101
1	0	0111	0110
1	0	1000	0111
1	0	1001	1000
1	0	1010	XXXX
1	0	1011	XXXX
1	0	1100	XXXX
1	0	1101	XXXX
1	0	1110	XXXX
1	0	1111	XXXX

Enable	Up	Count	Next
1	1	0000	0001
1	1	0001	0010
1	1	0010	0011
1	1	0011	0100
1	1	0100	0101
1	1	0101	0110
1	1	0110	0111
1	1	0111	1000
1	1	1000	1001
1	1	1001	0000
1	1	1010	XXXX
1	1	1011	XXXX
1	1	1100	XXXX
1	1	1101	XXXX
1	1	1110	XXXX
1	1	1111	XXXX

### These locations for A asserted

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
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 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

### These locations for B asserted

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

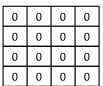
 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0



 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

### These locations for C asserted

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0

 0
 0
 0

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 0
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 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

### These locations for D asserted

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

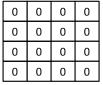
 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0

 0
 0
 0
 0



 0
 0
 0
 0

 0
 0
 0
 0

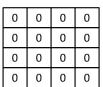
 0
 0
 0
 0

 0
 0
 0
 0

These locations for Up asserted

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

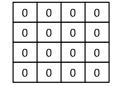


These locations for Enable asserted

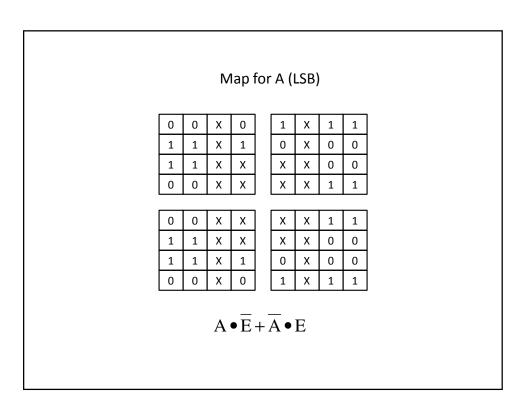
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0



0	4	12	8	40	44	36	32
1	5	13	9	41	45	37	33
3	7	15	11	43	47	39	35
2	6	14	10	42	46	38	34
18	22	30	26	58	62	54	50
19	23	31	27	59	63	55	51
17	21	29	25	57	61	53	49
16	20	28	24	56	60	52	48



Map for B

0	0	Х	0	1	Х	1	
0	0	Х	0	0	Х	0	
1	1	Х	Х	Х	Х	1	
1	1	Х	Х	Х	Х	0	

1	1	Х	Х
1	1	Х	Χ
0	0	Χ	0
0	0	Χ	0

Х	Х	1	1
Χ	Χ	0	0
0	Χ	1	1
0	Χ	0	0

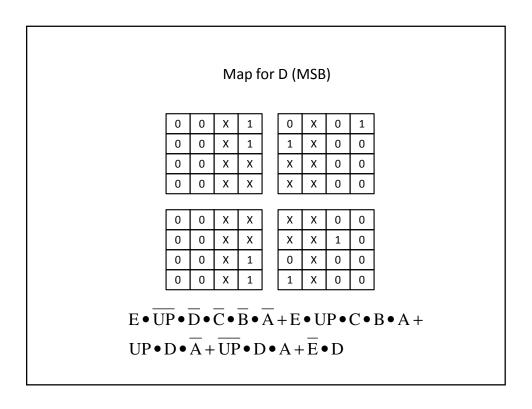
 $E \bullet UP \bullet \overline{D} \bullet \overline{B} \bullet A + E \bullet \overline{UP} \bullet C \bullet \overline{B} \bullet \overline{A} + E \bullet \overline{UP} \bullet D \bullet \overline{A} + UP \bullet B \bullet \overline{A} + \overline{UP} \bullet B \bullet A + \overline{E} \bullet B$ 

Map for C

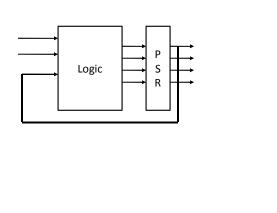
1	Х	0	0
0	Χ	1	0
Χ	Х	1	0
Χ	Χ	1	0

0	1	Х	Х
0	1	Χ	Х
0	1	Χ	0
0	1	Х	0

 $E \bullet \overline{UP} \bullet D \bullet \overline{B} \bullet \overline{A} + E \bullet UP \bullet \overline{C} \bullet B \bullet A + C \bullet B \bullet \overline{A} + \overline{UP} \bullet C \bullet A + \overline{E} \bullet \overline{D} \bullet C + UP \bullet C \bullet \overline{B}$ 



## Implementation Method for Clocked Sequential System



# Another Implementation Method for Clocked Sequential System State Logic R Decode Logic Logic

