EECE 338 - Spring 2011
Assignment 2 – CORDIC System with Bus Interface
Due Date: April 4, 2011

Design a CORDIC System (CORDIC) to be attached to a bus structure that will provide data and accept results. The data provided will be a single number, which is a value represented as a 32 bit fixed point value, scaled to be a number between +/- 1. Answers will be available in three registers. These answers are the terminal Z value, the final X value, and the final Y value, according to the CORDIC mechanism as presented in class.

The CORDIC System accepts a single value, then, before it responds to the bus communication protocol by asserting the acknowledge line, it will calculate the three new values. The CORDIC equations to be used with this assignment are:

$$Z_{i+1} = Z_i \pm \alpha_i \qquad (\alpha_i = \arctan(2^{-i}))$$
$$X_{i+1} = X_i \pm Y_i \times 2^{-i}$$
$$Y_{i+1} = Y_i \mp X_i \times 2^{-i}$$

The answers to be supplied by the CORDIC system when interrogated are the final Zi, Yi, and Xi. Transfers to and from the CORDIC system will take place on a 32 bit bus system that operates according to the four-event protocol. Thus, there are control lines writing to and reading from the registers of the CORDIC system. That is, the bus structure and protocol will be used to both fill and read the registers of the CORDIC system. When a value is written to the Z register, the CORDIC system performs the necessary work, then responds with the appropriate ACK activity. The user is then free to use read operations to read the final X, Y, and Z values.

The signals utilized by this project are:

Signal	Activity/Action
ADDR	Address bus – 32 lines identifying the address
DBUS	Data bus – 32 bit bidirectional data transfers
SYS_CLK_H	System clock – all activity synchronous with clock
SYS_RST_H	System reset – force sanity (to idle state)
REQ_H	Request line – to request activity on bus
ACK_H	Acknowledge line – slave's acknowledge to REQ_H
READ_H	Direction control – identifies direction of transfer

The addresses of interest for this project are:

Address	Activity/Action
0xFFFF_1040	Read/Write activity for Z value
0xFFFF_1044	Read activity for X value
0xFFFF_1048	Read activity for Y value

Your job is to design the CORDIC System. The design will be done with modules described in VHDL and combined appropriately. Your activities should include:

- Develop an algorithm that implements the CORDIC, and utilizes *buildable* constructs.
- Determine a data path block diagram. Again, you must use buildable constructs in the modules that you develop. Then utilizing those capabilities determine how to put together the system according to your algorithm.
- Identify the control points of your data path. Determine how the control points should be used to implement the algorithm on the data path. Represent this method with a state-diagram.
- Design a control system that operates according to your state-diagram. For this implementation, use a case construct with appropriate VHDL data types.

You are to supply the following items:

- A brief write-up describing your device. Include any state diagrams for sequential control systems or other pertinent design information. Include any flow diagrams, word descriptions, or other information that you feel will help your reviewer comprehend your brilliant design.
- VHDL as appropriate (be sure to comment extensively).
- Simulations of the system (a test bench will be provided).