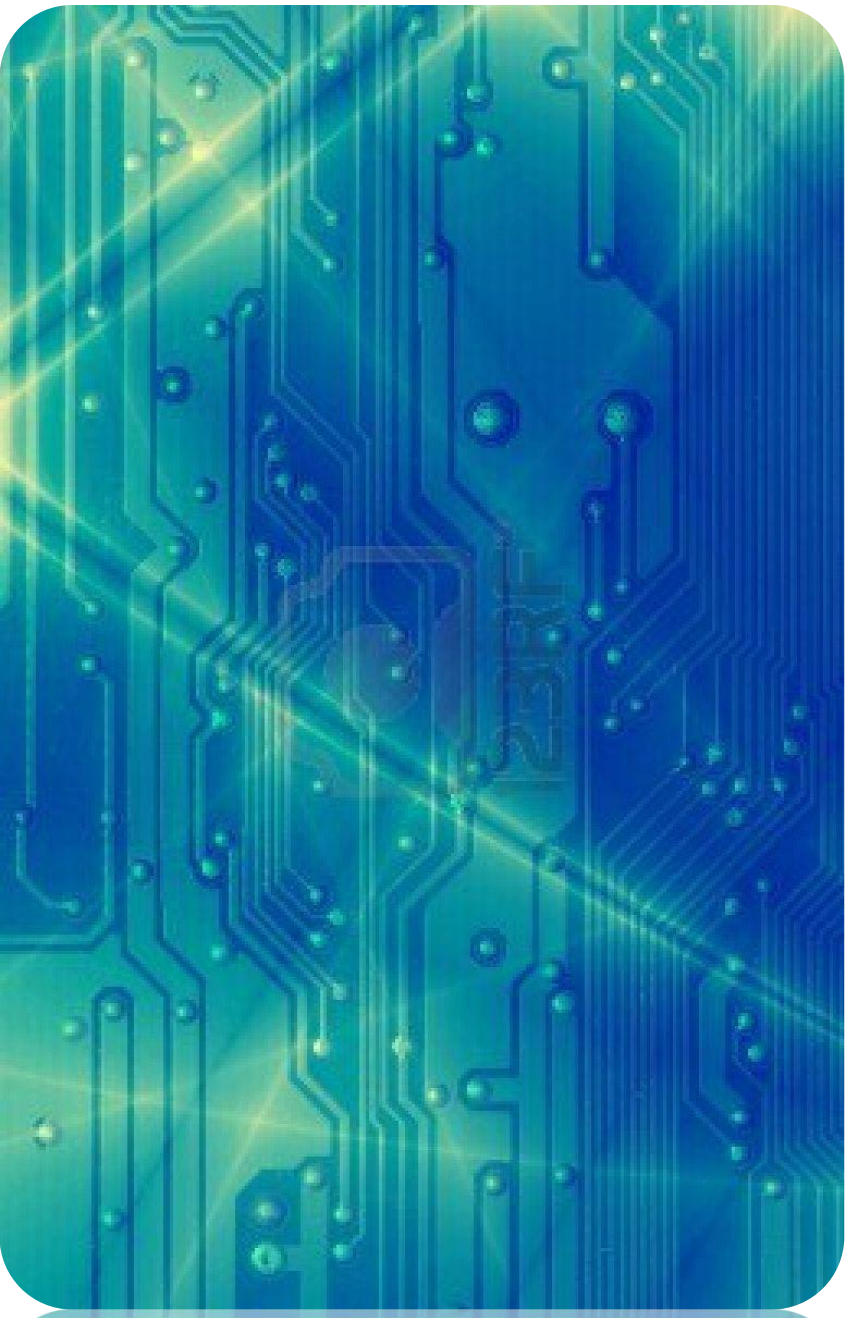

ECE 321

Term Project

2-1 Multiplexer

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I. INTRODUCTION

The ECE 321 Fall 2012 2-1 multiplexer project is intended to provide students with exposure to and hands-on practice in design, manufacturing-layout, PSPICE implementation, and analysis of a semiconductor circuit. Design of the circuit will be accomplished in LEDIT using MOSIS 2 μm Process (SCMOS) technology, and the LEDIT layout will be extracted to a PSPICE file for implementation and characterization. Analysis performed will include verification of circuit operation, worst case switching delay, worst case switching energy, input capacitances, and output resistance. Design considerations, implementation notes, results, and conclusions will be presented in this report.

II. DESIGN

1. Design Choice:

Many configurations of the 2-1 multiplexer have been developed. The performance of different options varies in size, power efficiency, speed, and cost. After experimentation with several designs our team chose to use CMOS transmission gates with the following considerations:

- Simplicity of design.
- Smallest number of components to assure logic integrity.
- Reasonable performance in speed and power consumption.

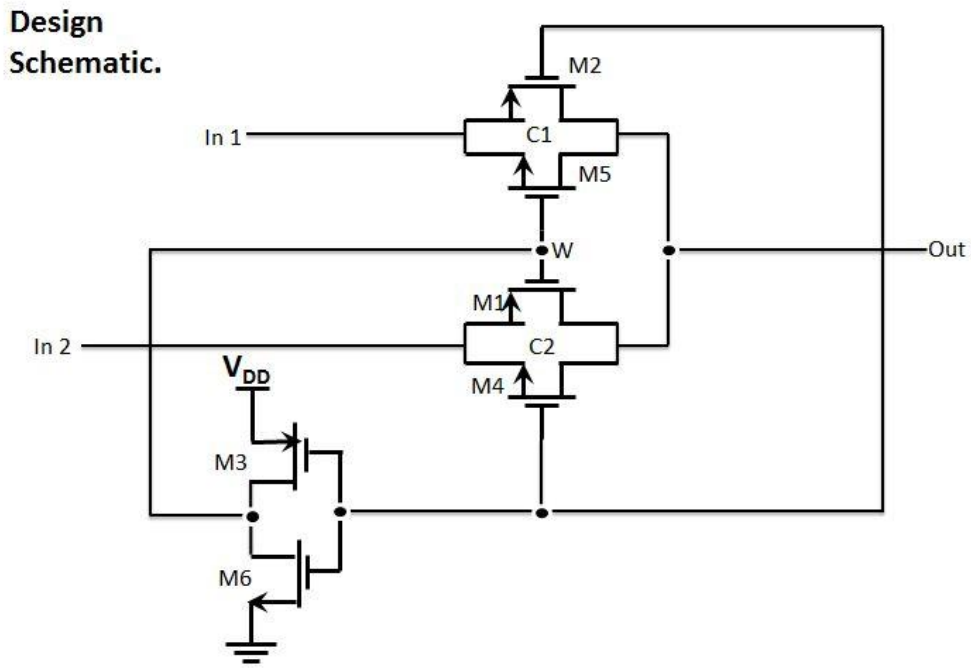

Figure 1

2. Layout: (total area = **5193 μm^2)**

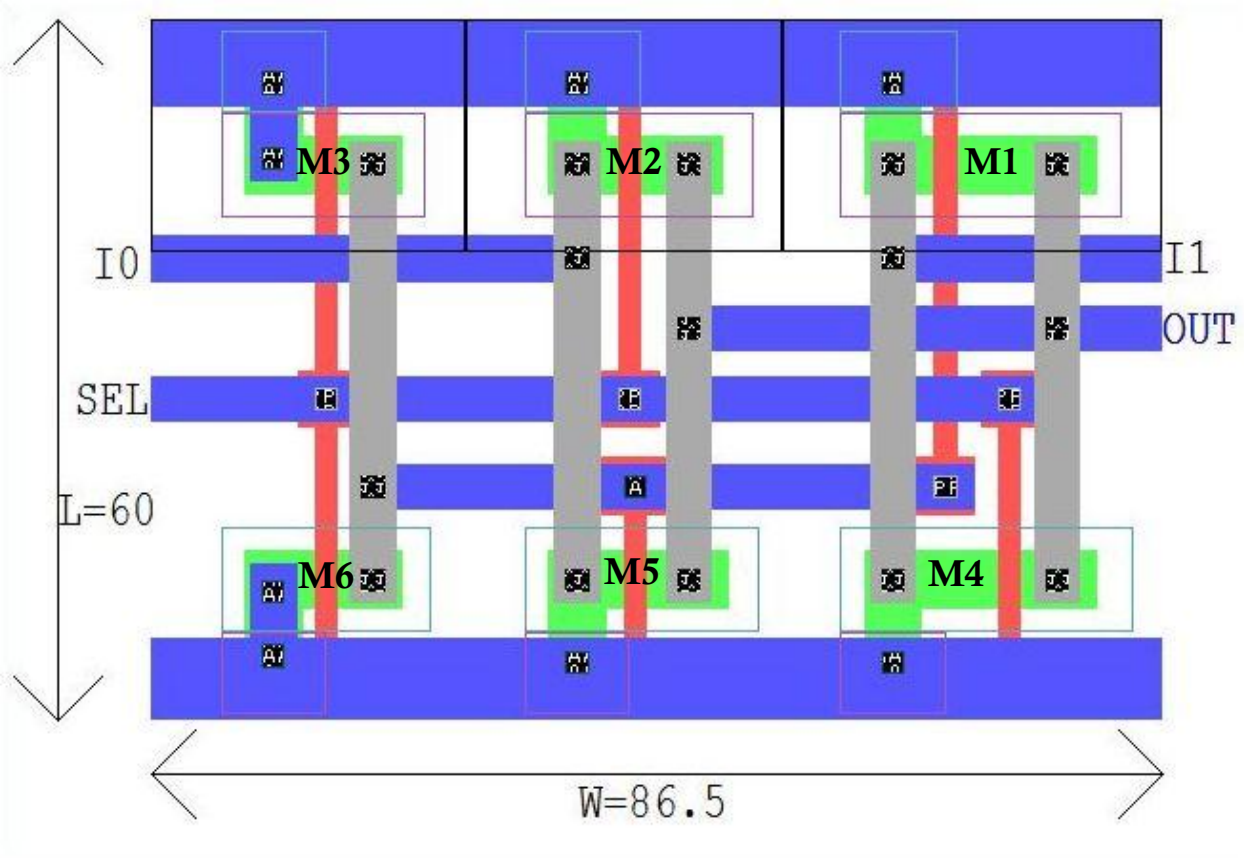

Figure 2: LEDIT Layout with dimensions.

Extraction from LEDIT to PSPICE produced a netlist that was edited for node numbering and to add power supply, ground, inputs, and output components. The extracted and adjusted code, listed below, was used to verify integrity of the circuit:

```
* Circuit Extracted by Tanner Research's L-Edit V7.12 / Extract V4.00 ;
* TDB File:  C:\Users\Tony\Desktop\321_Project\RunFrom\spread3_2dec1, Cell:  Cell0
* Extract Definition File:  C:\Users\Tony\Desktop\321_Project\RunFrom\template.ext
* Extract Date and Time:  12/02/2012 - 19:36

.include 2um_CMOS.modlib


* NODE NAME ALIASES

VDD 1 0 dc 5v
V_SEL 6 0 dc  0v pulse(0 5 0ps 1ps 1ps 10ns 20s)
V_IN_0 4 0 dc 5v pulse(0 5 10ps 1ps 1ps 30ns 60ns)
V_IN_1 3 0 dc 5v pulse(0 5 5ps 1ps 1ps 20ns 40ns)
CL 2 0 100ff

M1 2 5 3 1 cmosp L=2u W=5u AD=95p PD=58u AS=40p PS=26u
* M1 DRAIN GATE SOURCE BULK (200.5 -82.5 202.5 -77.5)
M2 2 6 4 1 cmosp L=2u W=5u AD=95p PD=58u AS=40p PS=26u
* M2 DRAIN GATE SOURCE BULK (173.5 -82.5 175.5 -77.5)
M3 5 6 1 1 cmosp L=2u W=5u AD=27.5p PD=21u AS=40p PS=26u
* M3 DRAIN GATE SOURCE BULK (147.5 -82.5 149.5 -77.5)
M4 2 6 3 0 cmosn L=2u W=5u AD=67.5p PD=47u AS=67.5p PS=37u
* M4 DRAIN GATE SOURCE BULK (206 -118 208 -113)
M5 2 5 4 0 cmosn L=2u W=5u AD=67.5p PD=47u AS=42.5p PS=27u
* M5 DRAIN GATE SOURCE BULK (174 -118 176 -113)
M6 5 6 0 0 cmosn L=2u W=5u AD=27.5p PD=21u AS=40p PS=26u
* M6 DRAIN GATE SOURCE BULK (147.5 -118 149.5 -113)

.op
.probe
.tran 100ps 300ns

* Total Nodes: 8
* Total Elements: 6
* Extract Elapsed Time: 0 seconds
.END
```

III. IMPLEMENTATION / RESULTS

Operation of the circuit was verified in PSPICE by applying pulses to each input in a sequence that allowed each data input to pulse one at a time while the select line was held in each select state for each pair of data pulses. The output followed each data input as expected and the sequence is shown in Figure 3.

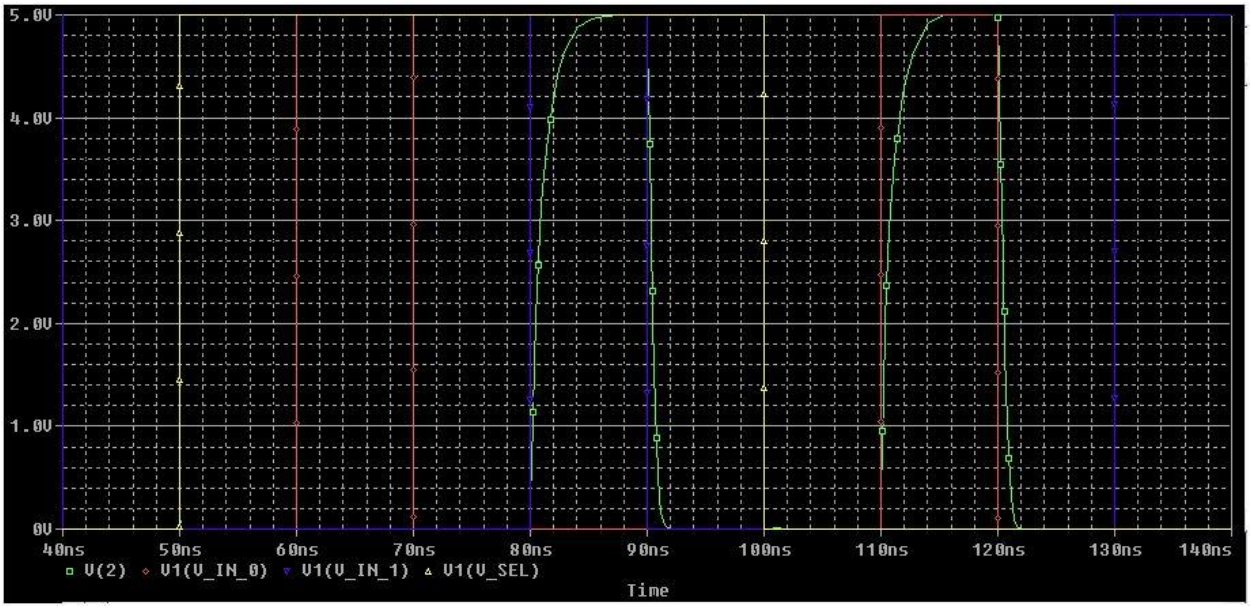

Figure 3: Verification of operation.

Transistor states were evaluated in a truth table to determine which state would apply the worst case delay and worst case switching energy. It was determined that two identically sized NMOS transistors on at the same time would carry the lowest drive current and would therefore cause the maximum delay. The truth table and possible worst case delay states are listed in Table 1.

SEL	I0	I1	OUT	M1	M2	M3	M4	M5	M6
0	0	0	0	0	0	1	0	1	0
0	0	1	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	0	0
0	1	1	1	0	1	1	0	0	0
1	0	0	0	0	0	0	1	0	1
1	0	1	1	1	0	0	0	0	1
1	1	0	0	0	0	0	1	0	1
1	1	1	1	1	0	0	0	0	1

Worst case delay (during transition to this state)

Worst case switching energy

Table 1: Transistor states per multiplexer state.

Worst case output delay was measured in PSPICE and was found to be 593ps. This measurement is shown in Figure 4 below.

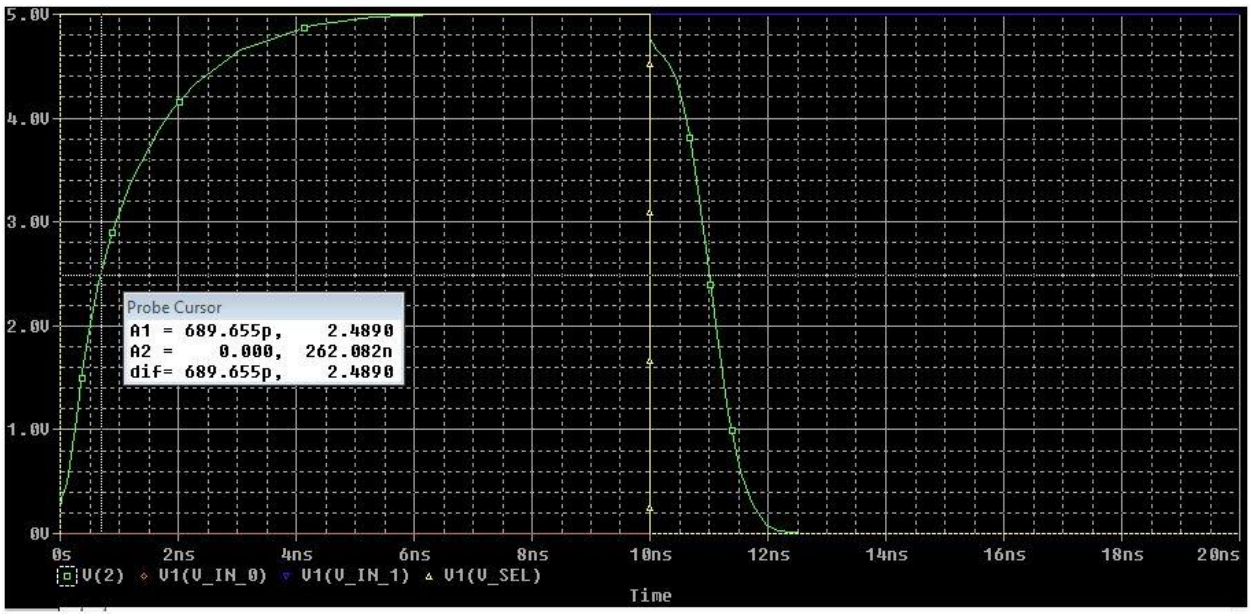

Figure 4: Worst case delay measurement.

Worst case switching energy was measured by first multiplying the total power dissipation listed at the end of the output file by the total transient interval in the simulation then dividing by the number of transitions in the interval:

$$\frac{(P_{total})(t_{transient\_interval})}{\#\ of\ transitions} = \text{Switching Energy}$$

$$\frac{(\mathbf{2.13}nW)(\mathbf{100}ns)}{\mathbf{3}} = \mathbf{71\ x\ 10^{-18}}J$$

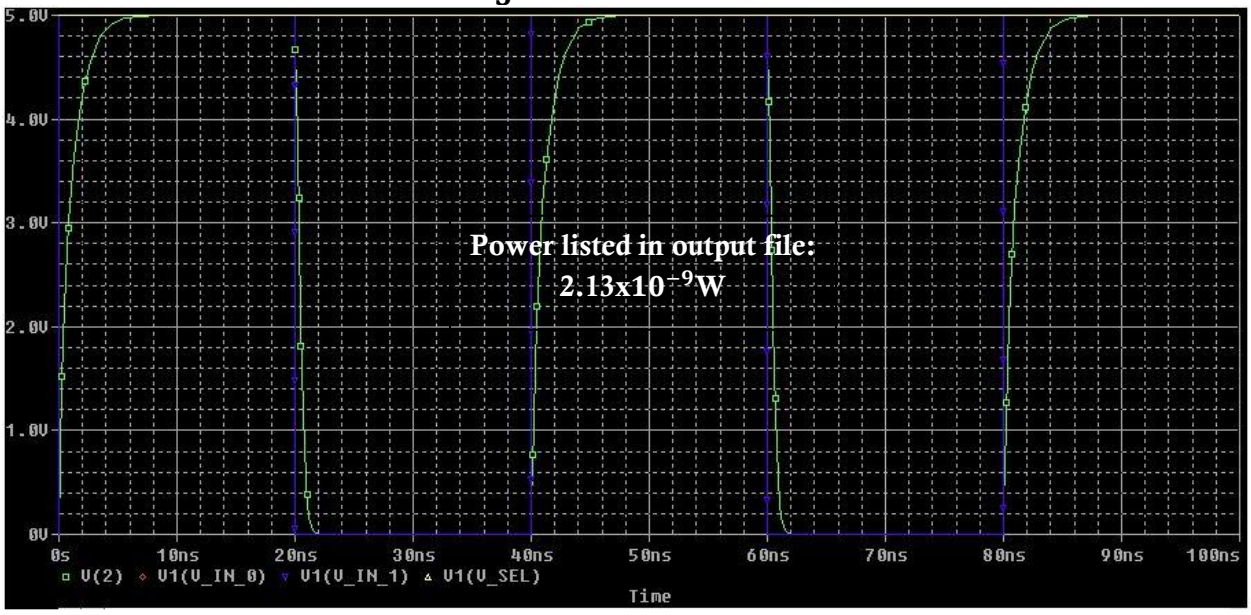

Figure 5: Worst case delay measurement.

R_{OUT} was calculated by adding a 1pF capacitor to the output while creating an output low to high transition then using equation $t_{pLH} = 0.69RC$ to solve for R.

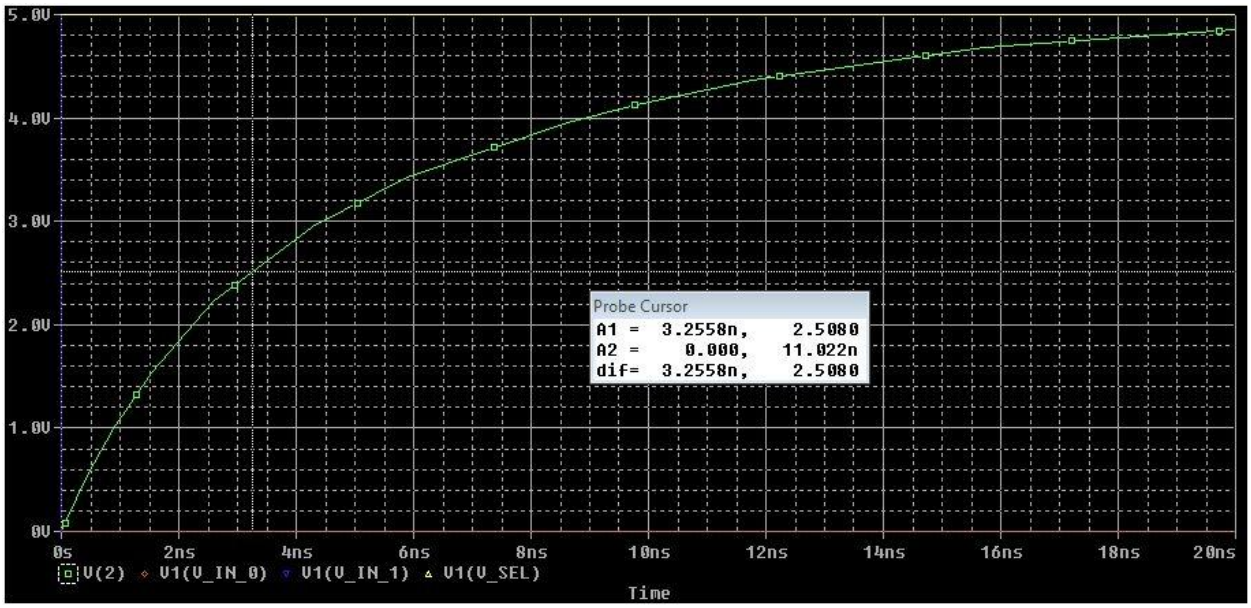

Figure 6: R_{OUT} delay measurement.

Capacitances of each input cell were calculated by finding the output delay t_{pLH} for a transition of each input then using equation: $t_{pLH} = 0.69RC$ to solve for each capacitance.

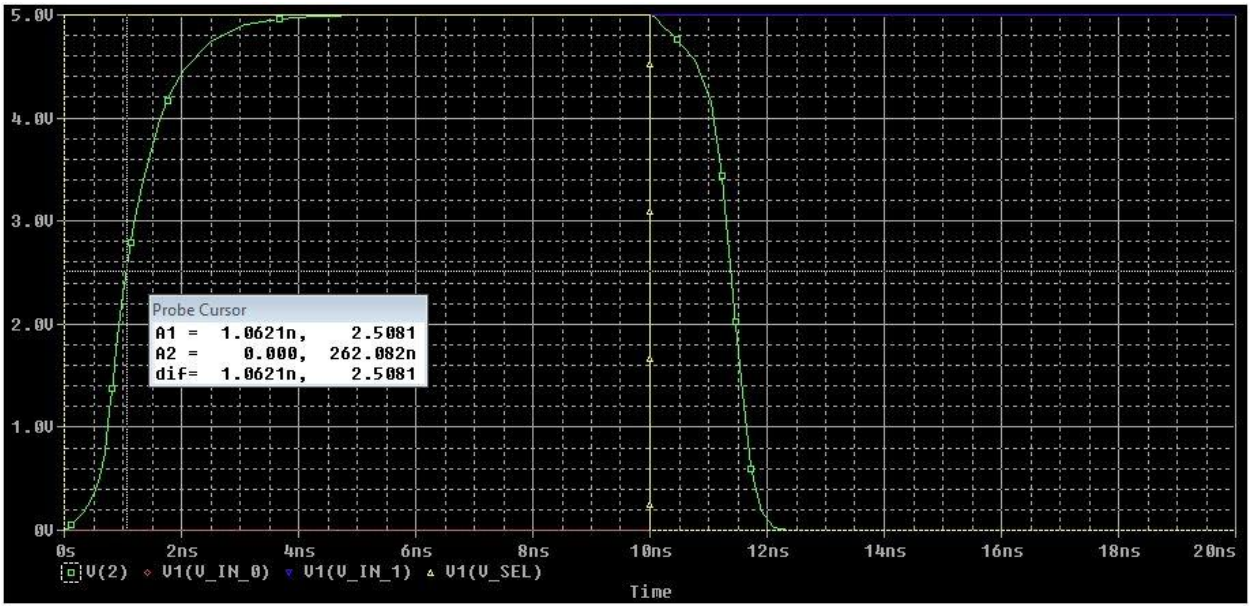

Figure 7: C_{IN-SEL} delay measurement.

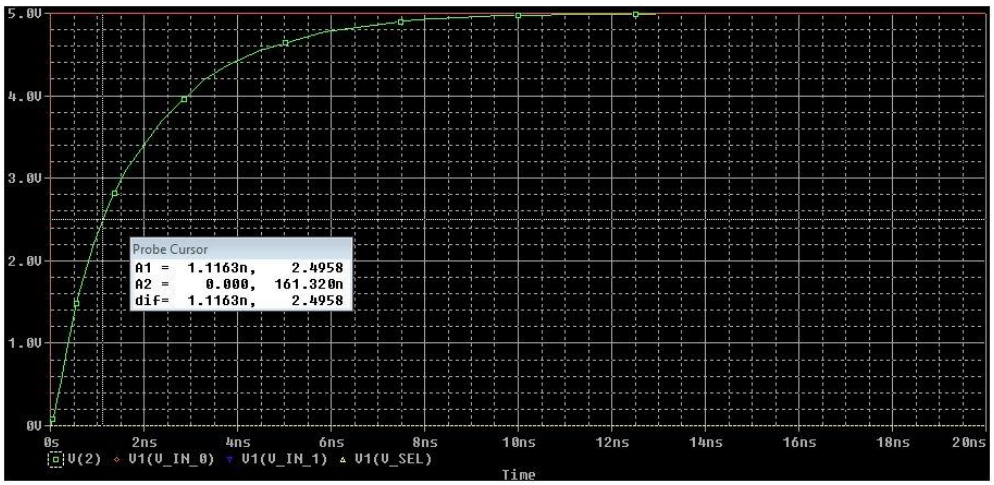

Figure 8: C_{IN-SEL} delay measurement.

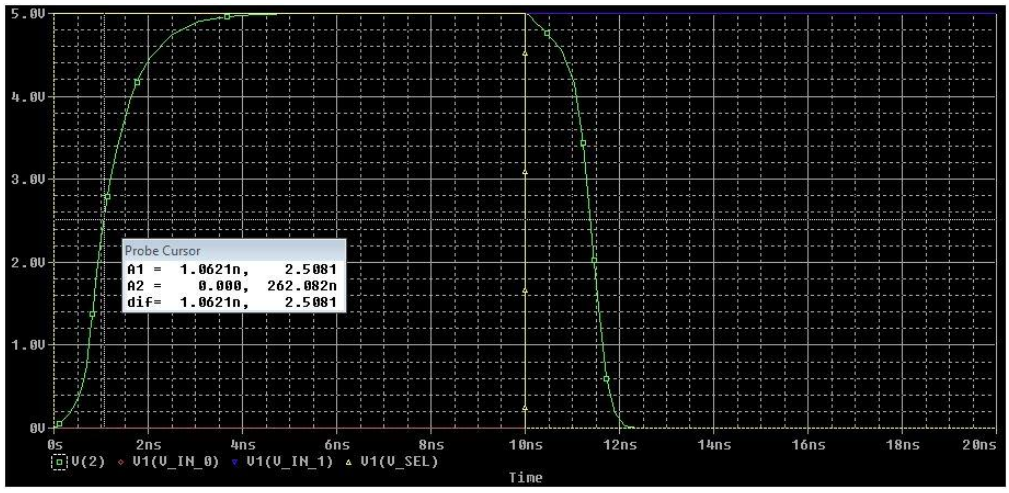

Figure 9: C_{IN-I0} delay measurement.

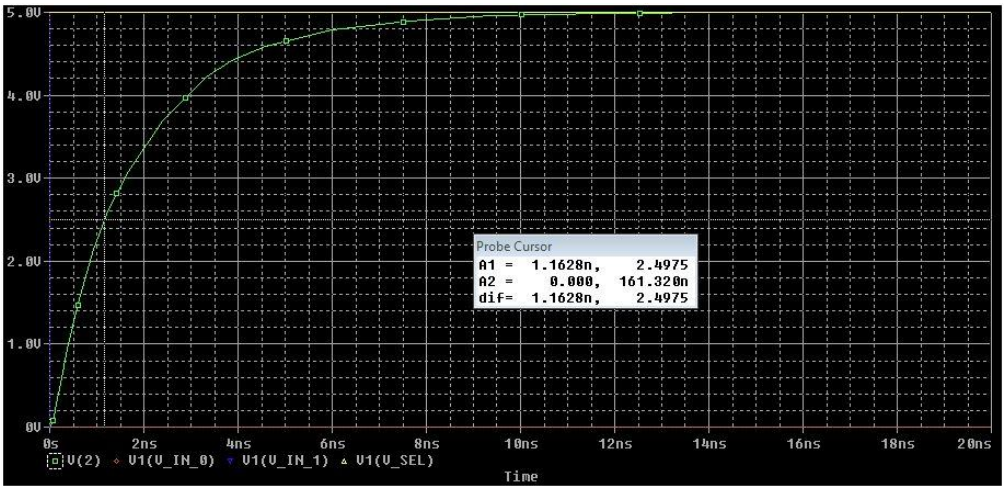

Figure 10: C_{IN-I1} delay measurement.

R_{OUT}	**4.718kΩ**
C_{IN-SEL}	**153.92fF**
C_{IN-I0}	**161.78fF**
C_{IN-I1}	**168.52fF**

Table 2: Cell characterization values.

Task	Becker	Mancuso	McConaha
Design Choice	3	3	3
LEDIT Layout	3	6	5
LEDIT Extract	3	1	3
PSPICE Configuration	2	2	3
Operation Verification	1	1	1
Adjustments	1	1	1
Characterization	3	6	3
Report	4	4	1
Total Hours	**20**	**24**	**20**

Table 3: Member participation.

IV. CONCLUSION

This project was a good introduction to the basic design process for a digital logic circuit. The 2-1 multiplexer is a very simple circuit that requires no extensive effort to understand and evaluate and the project therefore allowed for extensive focus on operations in LEDIT and PSPICE. Lecture notes and slides allowed for quick development of skills in the use of LEDIT and the application was found to be effective for the purpose of this project. PSPICE skills were improved for the team members due to the redundant effort required to get just the right combination of input pulses and output simulation results. Determination of switching energy was a difficult task. The final result was a reasonable value, but the

method used to obtain the data is not yet clear to the team. More work will be required to confirm the best approach to calculating energy consumption.

Our work with LEDIT revealed that there are many ways that a circuit can be laid out and different performance enhancements that can be applied, depending on the desired outcome. Our first design consisted of four transistors and scored well in the size department, however it came with a cost in efficiency. Testing and analysis of the chosen circuit in PSPICE proved that the circuit operated as intended, and the performance of the circuit seemed to be a good combination of short design and implementation time and reasonable speed and power consumption. It was determined as the project moved forward that there were opportunities to improve size and speed quite easily, however there was insufficient time to implement those improvements at the time of discovery.

In summary, the project provided good exposure to transistor logic design and all team members gained valuable practice in design, implementation, and analysis of digital electronic circuits.