ECE 321

Lab 8: CMOS Inverter Design

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(Tuesday)

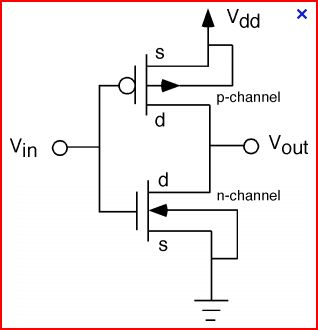
October 23, 2012

**Purpose:**

This laboratory exercise is intended to provide students with experience in the design, construction, and analysis of CMOS transistor discrete and packaged inverters.

**Procedure:**

1. Provide CMOS inverter schematic diagram.
2. List logic inverter truth table.
3. Construct single inverter circuit using:
   1. BS170 n-channel and BS250 p-channel MOSFETs.
   2. 7404 six-inverter integrated circuit.
4. Measure propagation delay for each circuit and record results.



**BS170**

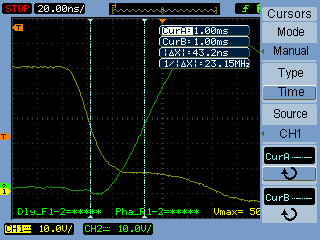
**BS250**

*Figure 1: CMOS Inverter.*

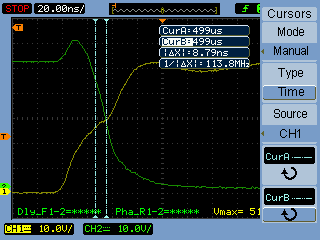
|  |  |
| --- | --- |
| **Vin** | **Vout** |
| 0 | 1 |
| 1 | 0 |

*Table 1: CMOS Inverter*

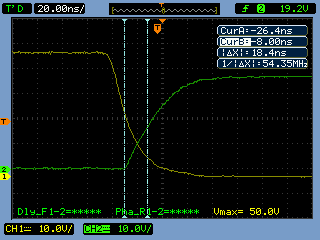
**Results:**

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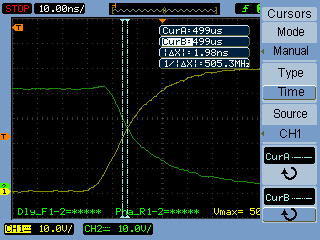
*Figure 2: Discrete transistor inverter .*

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*Figure 3: Discrete transistor inverter .*

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*Figure 4: 7404 packaged inverter .*

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*Figure 4: 7404 packaged inverter .*

|  |  |  |
| --- | --- | --- |
| **Circuit** |  |  |
| Discrete | 43.2ns | 8.79ns |
| 7404 | 18.4ns | 1.98ns |

*Table 2: Propagation Delays.*

**Conclusion:**

The propagation delays of the IC inverter were much lower than the delays of the discrete inverter. We noted during the experiment that the current flow in the discrete inverter was much lower than the current flow in the IC inverter circuit (about 50mA in the IC inverter and about 1mA in the discrete inverter). Delay in a CMOS inverter is proportional to the total circuit capacitance and inversely proportional to the circuit current. Since the differences in delay times were from 2 to 4 times greater in the discrete inverter and the current in the discrete inverter was lower, we conclude that the total capacitance in the discrete inverter was much larger than the total capacitance in the IC inverter.

The inverter has many practical uses, the most simple being that of a switch control. Inverters are used in NAND and NOR circuits, provide very low power requirements, and are most likely the most common form of transistor configuration used in all digital electronics.

We found that the datasheets we referenced for the BS250 p-channel transistor had erroneous pin-out information. The diagrams of transistor pin configurations in multiple documents indicated the opposite drain-gate-source locations than we found to be the actual case.

This lab provided a good introduction to CMOS inverter design, construction, and analysis.