ECE 321L

Lab 9: CMOS NAND Gate Design

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(Tuesday)

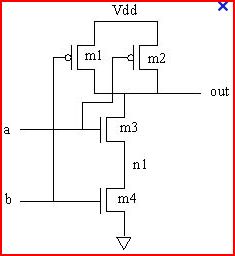
October 30, 2012

**Purpose:**

This laboratory exercise is intended to provide students with experience in the design, construction, and analysis of CMOS NAND gate operations.

**Procedure:**

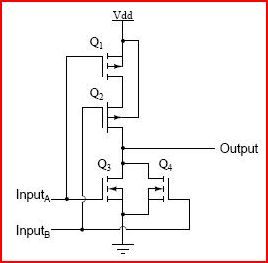
1. Provide NAND inverter schematic diagram.
2. List NAND truth table.
3. Construct NAND circuit using:
   1. BS170 n-channel and BS250 p-channel MOSFETs.
   2. 7400 quad-NAND integrated circuit.
4. Measure propagation delay for discrete and IC NAND circuits and record results.
5. Provide NOR inverter schematic diagram.
6. List NOR truth table.
7. Construct NOR circuit using:
   1. BS170 n-channel and BS250 p-channel MOSFETs.
   2. 7402 quad-NOR integrated circuit.
8. Measure propagation delay for discrete and IC NOR circuits and record results.



*Figure 1: Discrete NAND Gate.*

|  |  |
| --- | --- |
| **ab** | **out** |
| 00 | 1 |
| 01 | 1 |
| 10  11 | 1  0 |

*Table 1: NAND Truth Table*

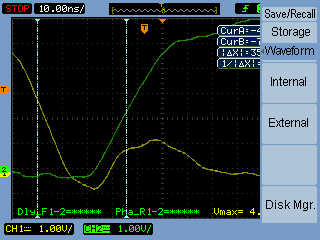
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*Figure 2: Discrete NOR Gate.*

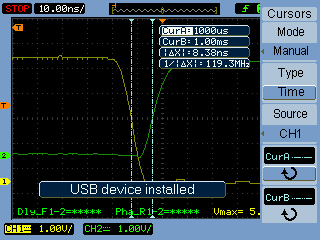
|  |  |
| --- | --- |
| **ab** | **out** |
| 00 | 1 |
| 01 | 0 |
| 10  11 | 0  0 |

*Table 2: NOR Truth Table*

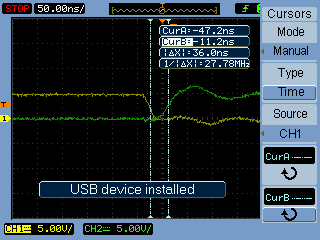
**Results:**

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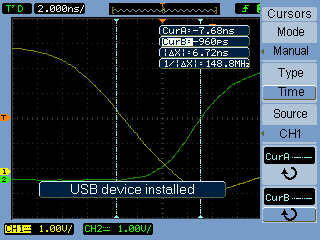
*Figure 2: NAND discrete transistor inverter .*

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*Figure 3: NAND 7400 IC inverter .*

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*Figure 4: NOR discrete inverter .*

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*Figure 5: 7404 IC packaged inverter .*

|  |  |
| --- | --- |
| **Circuit** |  |
| Discrete NAND | 35.6ns |
| 7400 NAND | 8.38ns |
| Discrete NOR | 36ns |
| 7402 NOR | 6.72ns |

*Table 2: Propagation Delays.*

**Conclusion:**

Propagation delays of the IC NAND and NOR circuits were much lower than the delays of the discrete circuits. Delay in a CMOS inverter is proportional to the total circuit capacitance and inversely proportional to the circuit current. Since the differences in delay times were from 4 to 6 times greater in the discrete circuits we conclude that the total capacitance in each of the discrete circuits was much larger than the total capacitance in the corresponding IC circuits.

This lab provided a good introduction to CMOS NAND and NOR design, construction, and analysis.