

Assignment 4 – NAND3 Layout & Logic Functions

ELEC 402

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1.0 Project Description

This project consisted in using the Cadence Design tools to layout and characterize a NAND3 circuit. First, the sizing of the transistors of the NAND3 gate are calculated using theoretical inverter sizing. A layout is then created, verifying the design using DRC, LVS, then extracting the parasitic components from the layout. The layout was designed with the aim of reducing the time delay and area as much as possible. Next, a logic circuit is analyzed and simulated to find its worst case rising and falling delays. Finally, the RC and Elmore delays for a transmission gates circuit are calculated, and optimized by deriving an optimal output inverter size.

2.0 NAND3 Simulation & Layout

A symmetrical NAND3 gate is designed on Cadence with equal tpLH and tpHL delays, measured from 50% to 50%. The aim of this simulation is to obtain a time difference within 5ps. We use an input clock slew rate of 10ps, with a 10fF load capacitance, and a VDD of 1V. The goal of this assignment is to design the smallest and fastest NAND3 gate meeting the above requirements.

2.1 NAND3 Schematics and Sizing

Using the standard sizing for an inverter of 2W for PMOS and 1W for NMOS, we design and calculate the theoretical widths for the NMOS and PMOS transistors. The PMOS width is calculated to be 2W each, and the NMOS are 3W. However, as these sizes do not meet the symmetric time requirements when simulated later, the widths are doubled in simulation, therefore PMOS are 4W, and NMOS are 8W. A stick diagram such as in Figure 2.1 was designed to get an overview of the gate layout.

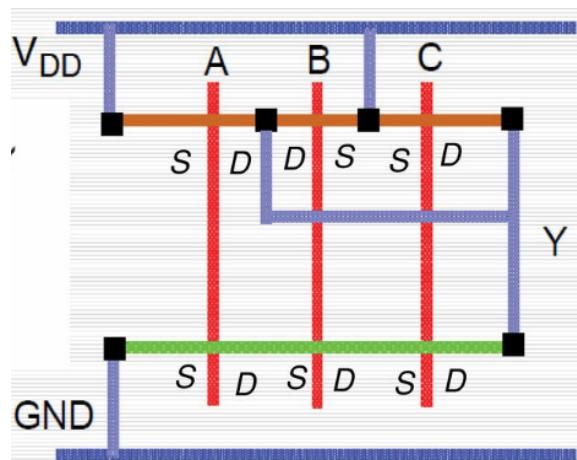


Figure 2.1: NAND3 Stick Diagram

We design the NAND3 Schematics that we will use for Layout comparison on Cadence. The following schematics in Figure 2.2 is created.

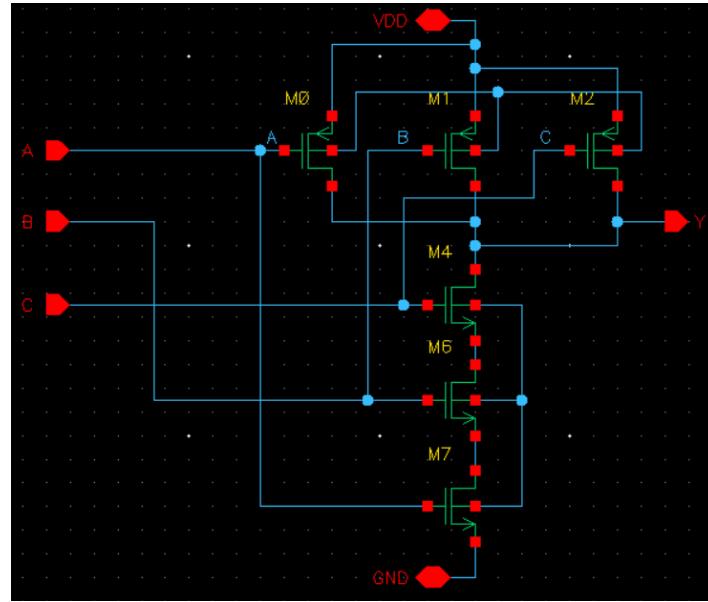


Figure 2.2: NAND3 Cadence Schematics

2.2 NAND3 Layout and Pain

The layout diagram shown in Figure 2.3 was created using 3 NMOS pCells and 3 PMOS pCells, with 4 fin NMOS and 8 fin PMOS. Note that certain details such as labels may not be fully observable when zoomed out of the layout in this figure.

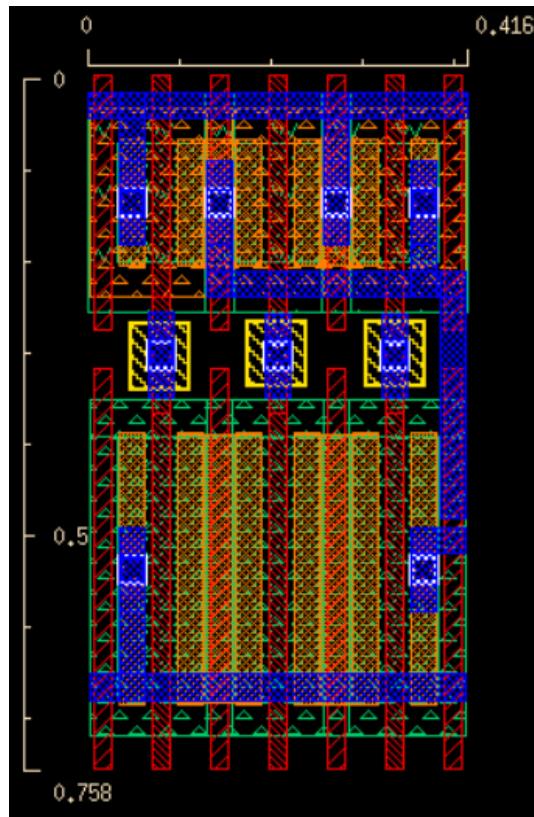


Figure 2.3: Full NAND3 Gate Layout View

The following materials in Table 2.1 were added to the schematics and pCells to form connections.

NMOS pCell Connections	PMOS pCell Connections	Gates	Gate Interconnect	Metal Connections	Contacts
PIM	NIM	GATEA	GIL	M1A	Vo

Table 2.1: Used Design Materials List

A closer snapshot of the NAND3 gate layout is included showing labels and more detail as shown in Figure 2.4. Adding rulers to measure the width and length of the layout, we see an approximate length of 0.758 um and width of 0.416 um. Using the built in Cadence function to calculate Area and Density of layout, an area of $0.375678 \mu\text{m}^2$ is obtained as shown in Appendix D.

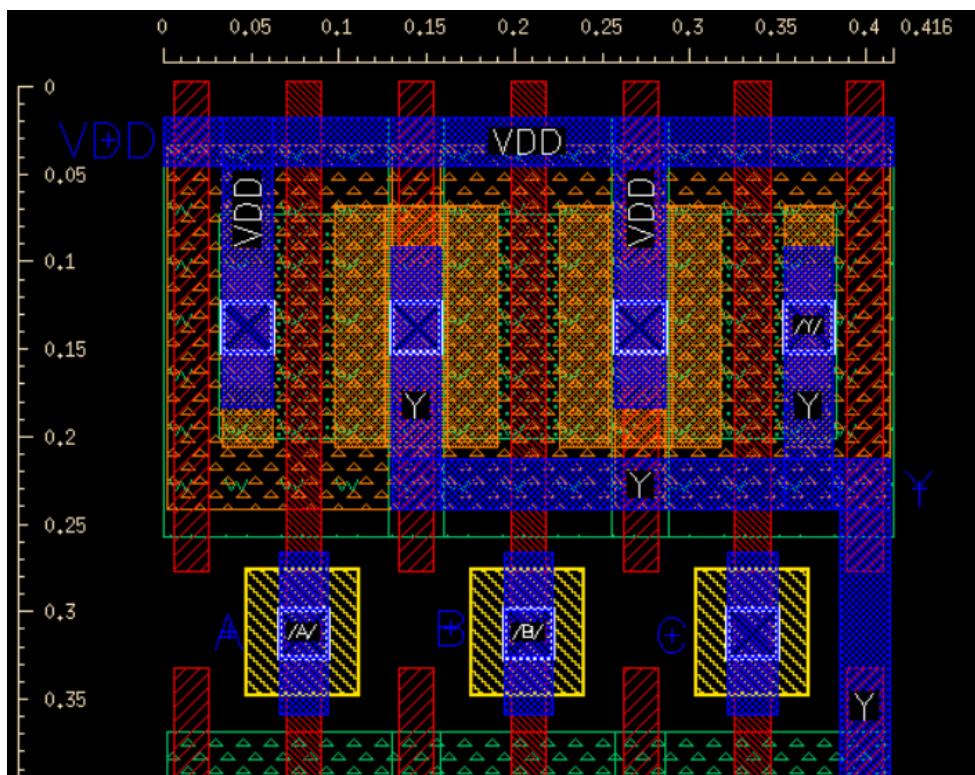


Figure 2.4: NAND3 Layout PMOS pCells and Connections

Each input pin A, B, and C are distanced 0.128 um from each other as measured from the center of their contact point and pin. The nearest pin C, is positioned a horizontal distance of 0.03 um, and 0.17 um vertically from the output pin Y. Further dimensioning and measured distance between pins of the layout are shown in Table 2.2.

	A - B - C	VDD - Y	C - Y	Y - GND
Horizontal Distance (um)	0.128	0.32	0.03	0.32
Vertical Distance (um)	0	0	0.17	0.341

Table 2.2: Horizontal and Vertical Distances of Layout Pins

Over the development of the gate, the Design Rule Check (DRC) is used repeatedly to ensure that material geometries do not violate manufacturing capabilities for a valid design. The final DRC summary can be found in Appendix A.

Next, we use Layout vs Schematic (LVS) to check for connectivity differences between layout and our schematic previously designed. The LVS report can be found in Appendix B.

Once the design is confirmed to be correct, we extract all parasitic resistances, capacitances, and inductances from the layout through Parasitic Extraction (PEX). The Netlist shown in Appendix C is extracted, and a circuit block is obtained for our NAND3 layout. Using this block, the testbench shown in Figure 2.5 is created. For the worst-case delay, inputs A and B are connected to VDD, and pulsing input is applied to input C with a clock skew rate of 10ps, therefore switching between ABC = 000 -> 001.

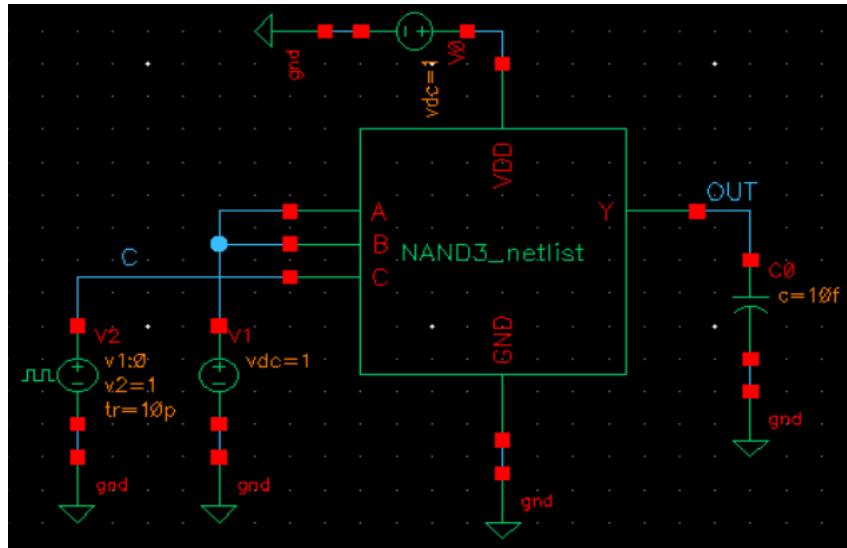


Figure 2.5: NAND3 Layout Testbench

The waveform shown in Figure 2.6 is simulated, resulting in a time difference between tpHL and tpLH of 0.929ps, as shown in Table 2.3, meeting design restrictions. Total time delay is obtained using:

$$t_d = \frac{tpHL + tpLH}{2}$$

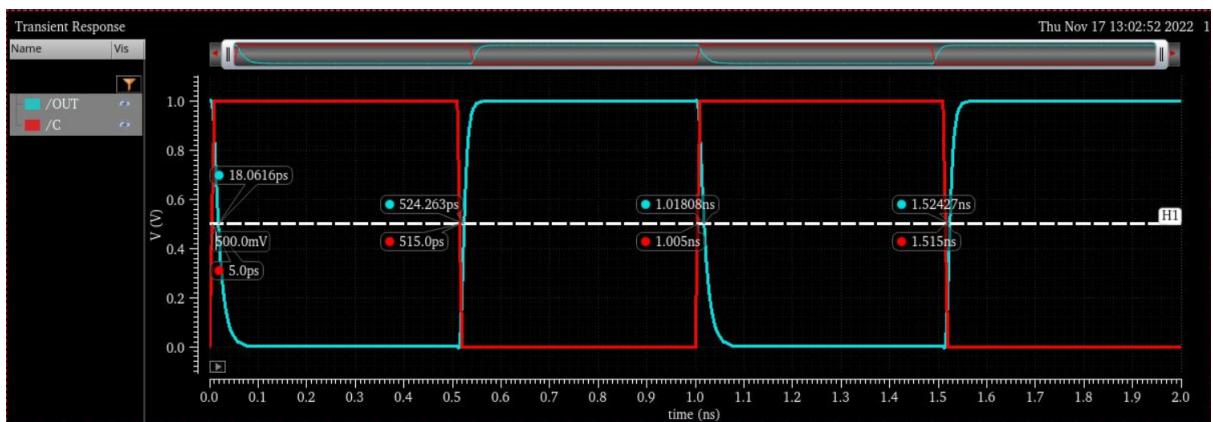


Figure 2.6: NAND3 Layout Testbench Waveform

tpHL (ps)	tpLH (ps)	Time Difference (ps)	Delay (ps)
9.431	10.36	0.929	9.8955

Table 2.3: Simulated Delays and Calculations

Finally, the area x delay is calculated using the layout area obtained above using the Cadence tool as shown in Table 2.4.

Measured Length (μm)	Measured Width (μm)	Computed Area (μm^2)	Delay (ps)	Area x Delay ($\mu m^2 \times ps$)
0.758	0.416	0.375678	9.8955	3.71752

Table 2.4: Area x Delay Calculations

3.0 Logic Function and Gate Sizing

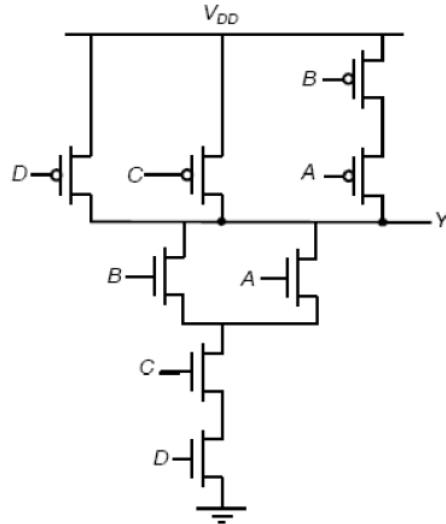


Figure 3.1: Logic Circuit

3.1 Logic Function as Boolean Expression

The Boolean expression of the circuit in Figure 3.1 can be found by analyzing the pull-down section of this transistor circuit. Taking Y as the output, we see B and A in parallel, then in series with C and D. Therefore, the pull-down expression can be written as:

$$\bar{Y} = (A + B) * C * D$$

Therefore, the Boolean expression for the circuit is:

$$Y = \bar{A}\bar{B} + \bar{C} + \bar{D}$$

3.2 Gate Sizing and Output Resistance

Next, the NMOS and PMOS gates are sized such that the output resistance is the same as that of an inverter with NMOS W/L = 4λ and PMOS W/L = 8λ .

Comparing the circuit in Figure 3.1 to a standard inverter with PMOS width 2W and NMOS width W with equivalent output resistance, transistor widths are allocated as shown in Figure 3.2.

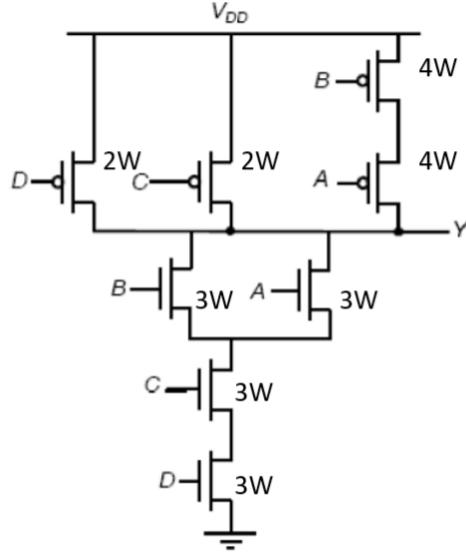


Figure 3.2: Logic Circuit Gate Widths

Taking the worst case into account for the pull-up circuit, the path taken would be the A-B PMOS branch, as more resistance is seen from the output due to more transistors.

In the pull-up circuit, PMOS sized 4W are equivalent to a width of 16λ while PMOS sized 2W are equivalent to 8λ . In the pull-down circuit, all NMOS have a width of 3W, resulting in a width of 12λ .

3.2 Worst Case Delays and Simulation

High to Low (tpHL)

Next, we find the worst case input patterns for A, B, C, and D inputs resulting in the worst case tpLH and tpHL. In the case of High to Low delay tpHL, we consider the NMOS portion of the circuit. To charge as many nodes as possible before the transition, all inputs could be on to the exception of D to prevent discharging to GND, for example ABCD = 1110 || 1010 || 0110.

During discharge, we want to provide the least amount of paths available to ground while turning on D to discharge. Therefore, the worst case High to Low transition can be ABCD = 1010 -> 1011 || 0110 -> 0111.

Low to High (tpLH)

To find the worst case Low to High delay, we consider the PMOS portion of the circuit. To keep as many nodes connected to GND initially, we keep transistor A off while the rest are on, therefore ABCD = 0111.

While transitioning, we turn on the least number of PMOS possible to drive the output Y to VDD. Therefore the worst case path from Low to High is **ABCD = 0111 -> 0011**.

Cadence Simulation

The following schematics shown in Figure 3.3 was created in Cadence to simulate the logic circuit in Figure 3.2 with the calculated widths. Figure 3.4 a) shows the testbench simulating the worst case High to Low tpHL delay case where ABCD = 1010 -> 1011. Input A and C are on while input B is grounded, and input D is connected to a step function, simulating the switching transition. Figure 3.4 b) shows the testbench simulating the worst case Low to High tpLH delay case where ABCD = 0111 -> 0011.

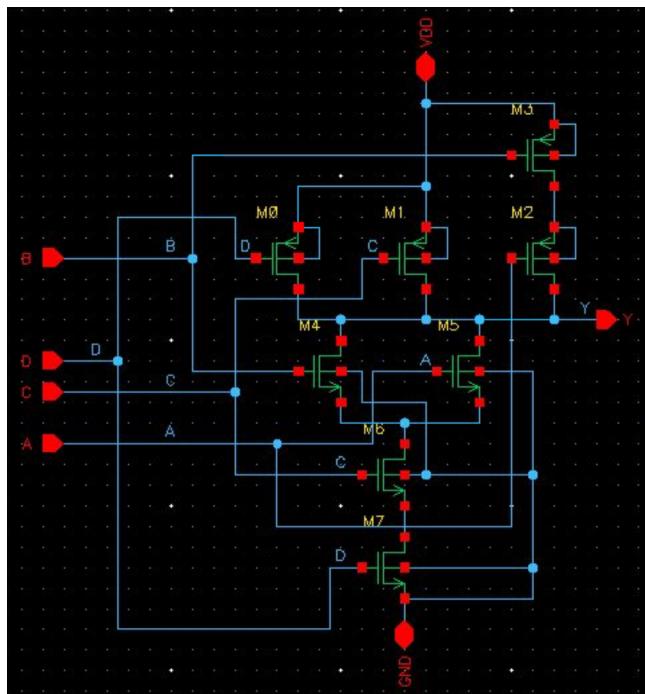


Figure 3.3: Cadence Logic Circuit Schematics

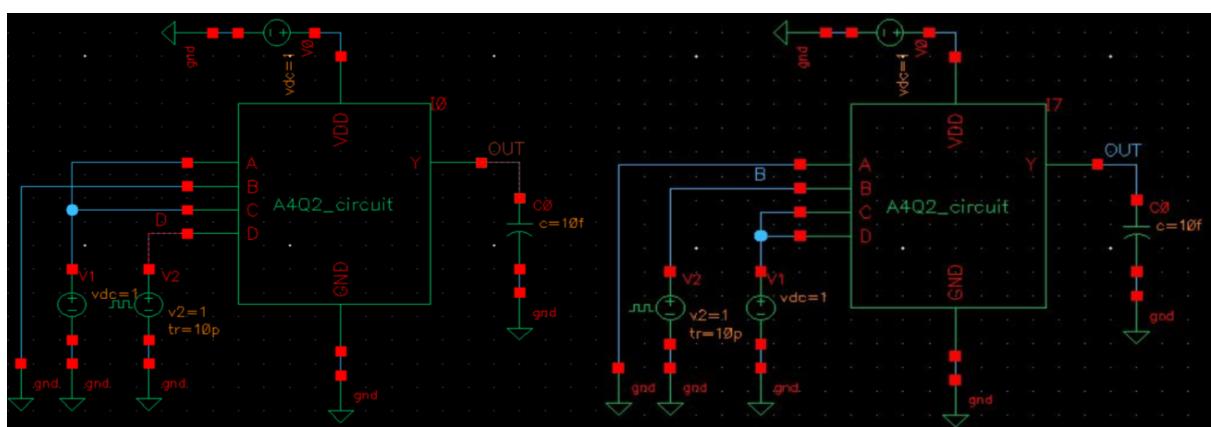


Figure 3.4: Testbench for Worst Case a) High to Low Delay, b) Low to High Delay

Taking the 50% rising point of input D and 50% falling point from the testbench simulation in Figure 3.5, the worst case tpHL delay is found to be $39.55 - 5.0 = 34.55$ ps.

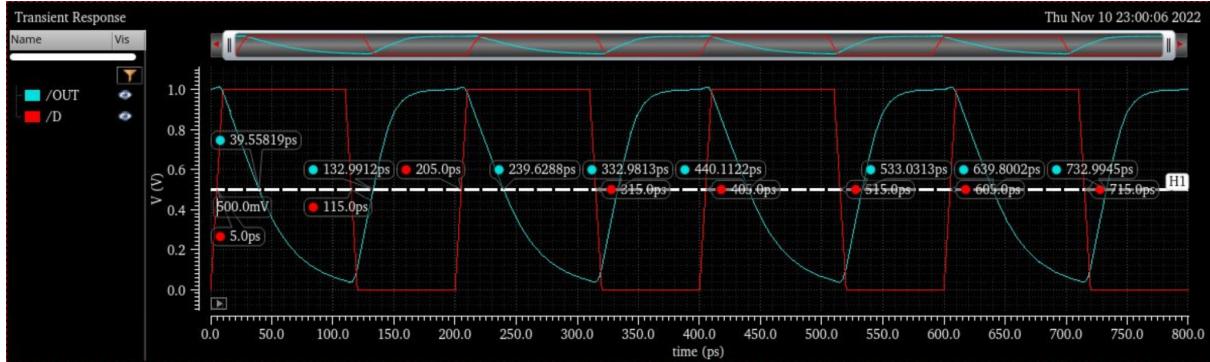


Figure 3.5: Worst Case High To Low Delay Simulation

Taking the 50% falling point of input D and 50% rising point, the worst case tpLH delay is found to be $140.05 - 115.0 = 125.05$ ps.

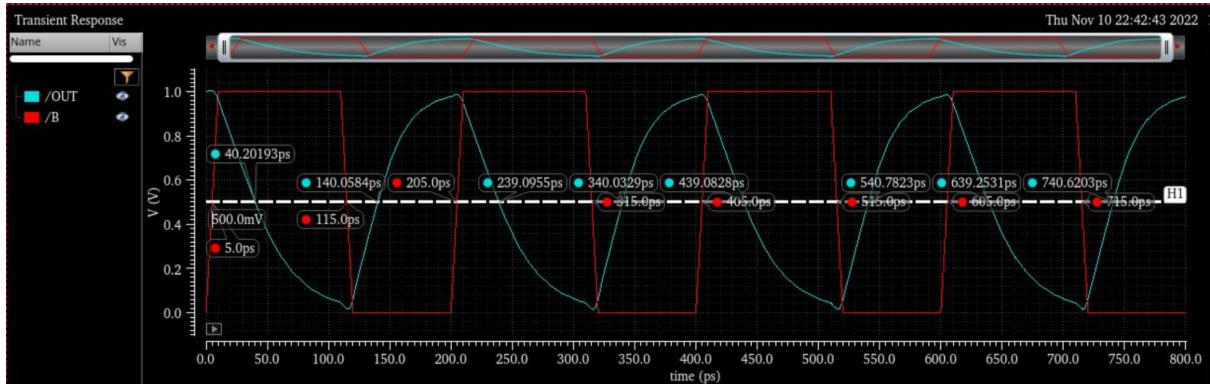


Figure 3.6: Worst Case Low to High Delay Simulation

The worst case tpLH and tpHL delay schematics netlists are included in Appendix E and Appendix F respectively.

4.0 Transmission Gates Circuit Analysis

The transmission Gates circuit shown in Figure 4.1 shows two transmission gates sized $4\lambda: 2\lambda$ with inverters driving the transmission gates constructed of PMOS sized $8\lambda: 2\lambda$ and NMOS sized $4\lambda: 2\lambda$, where $\lambda = 0.1 \mu m$. The output inverter drives a 50 fF load, and is f times larger than the input inverters.

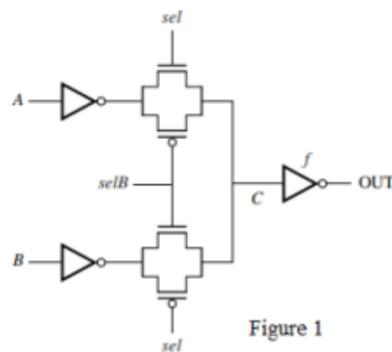


Figure 1

Figure 4.1: Transmission Gates and Inverter Circuit

4.1 Boolean Expression

The expression for the output function in terms of A, B, sel, and selB can be derived by observing the circuit. the combination of the two transmission gates form an OR operation. To select \bar{A} , the top TG activates using the sel signal. to select \bar{B} , the bottom TG activates using the selB signal. Therefore, the boolean expression for this circuit is found to be:

$$OUT = \bar{C} = (\bar{A} * sel) + (\bar{B} * selB)$$

$$OUT = C = (A + \bar{sel}) * (B + \bar{selB})$$

4.2 Equivalent RC Circuit of A-C Path

An equivalent RC circuit model for the path from A to C is created, assuming that the sel signal is high. Following the path from input A to output C as shown in Figure 4.2, we pass through resistance resulting from the inverter, capacitance at the node between the inverter and TG, TG resistance, and more capacitance at the node between the TG and output inverter.

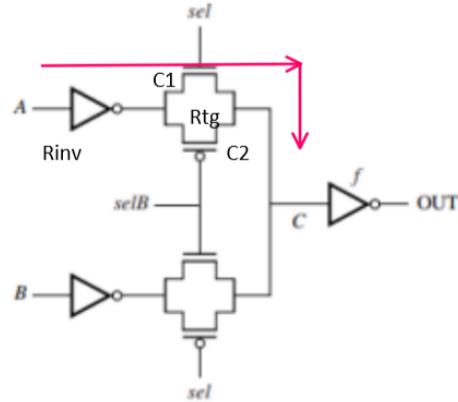


Figure 4.2: Path from A-C with Resistance and Capacitance

The equivalent RC circuit is shown in Figure 4.3. The TG resistance Rtg can be approximated to be $R_{TG} = R_{eqn}(L/W)$ and Rinv to be $R_{inv} = R_{TG}$. Therefore,

$$R_{Inv} = R_{TG} = 12.5k * (2/4) = 6.25 k\Omega$$

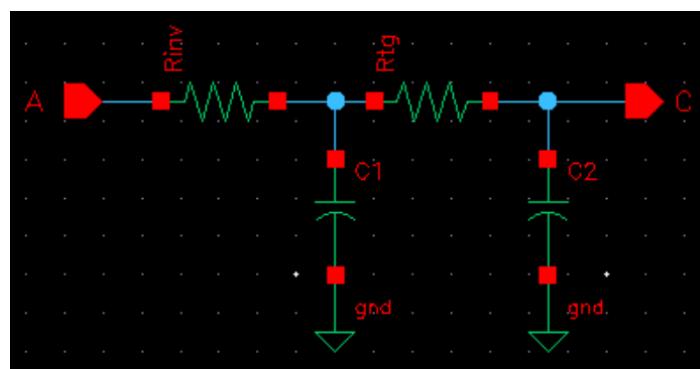


Figure 4.3: RC Circuit of Path from A-C

To find C₁, we consider both the inverter and TG capacitance. The inverter has capacitance $C_{inv} = C_{eff} * (4\lambda + 8\lambda)$ while the TG has a capacitance of $C_{TG} = C_{eff} * 2(4\lambda) + C_g(4\lambda)$ when turned on. Therefore:

$$C_1 = C_{inv} + C_{TG} = (4\lambda + 8\lambda)C_{eff} + C_{eff} * 2(4\lambda) + C_g(4\lambda)$$

$$C_1 = 20\lambda C_{eff} + 4\lambda C_g = (20)(0.1)(0.1) + (4)(0.1)(0.2) = 2.4 fF$$

To find C₂, the TG capacitance is obtained in a similar method while taking into account the output inverter, being f times larger than the input inverters. The load inverter capacitance is known to be $C_{li} = fC_g(4\lambda = 8\lambda)$. Therefore:

$$C_2 = f(4\lambda + 8\lambda)C_g + 2(4\lambda)C_{eff} + (4\lambda)C_g$$

$$C_g = 2.4f + 1.6 fF$$

4.3 Elmore Delay

The expression for the elmore delay from A to C can be found for the RC circuit use the following expression:

$$t_D = R_{inv} C_1 + (R_{inv} + R_{TG})C_2 \text{ where } R_{inv} = R_{TG} = 6.25 k\Omega$$

Where C₁ and C₂ are as indicated in Section 4.2

4.4 A-OUT RC Delay

Similarly to Section 4.2, an equivalent RC circuit model for the path from A to OUT shown in Figure 4.4 is created.

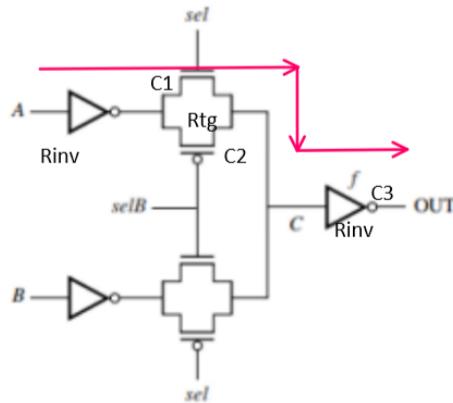


Figure 4.4: Path from A-OUT with Resistance and Capacitance

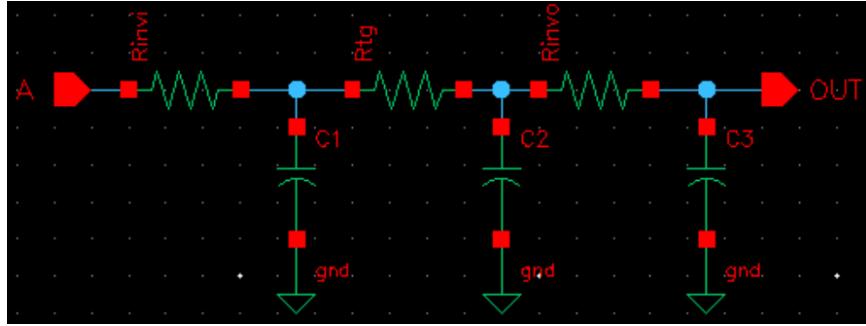


Figure 4.5: RC Circuit of Path from A-OUT

As the only additions to the corresponding RC circuit in Figure 4.5 are Rinvo and C₃, C₁ and C₂, the RC delay can be found similarly to Section 4.2. For C₃ and Rinvo:

$$C_3 = fC_{eff}(4\lambda + 8\lambda) + C_{load} \text{ where } C_{load} = 50 \text{ fF}$$

$$C_3 = 1.2f = 50 \text{ fF}$$

$$R_{invo} = \frac{R_{invi}}{f}$$

To find RC Delay:

$$t_D = R_{invi}C_1 + (R_{invi} + R_{TG})C_2 + (R_{invi} + R_{TG} + \frac{R_{invo}}{f})C_3$$

4.5 Output Inverter Optimal Size

The optimal size of the output inverter can be found such that it minimizes the total delay from A to OUT. Using Elmore delay and $R_{invi} = R_{invo} = R_{TG} = R$ where $R = 6.25 \text{ k}\Omega$

$$t_D = RC_1 + 2RC_2 + (2R + \frac{R}{f})C_3$$

$$t_D = 6.25k * (7.2f + 106.8 + \frac{50}{f})$$

To minimize the delay, we minimize the terms containing f, plotting $y = 7.2f + 50/f$, resulting in the following plot. The minima is found at $f = 2.635$.

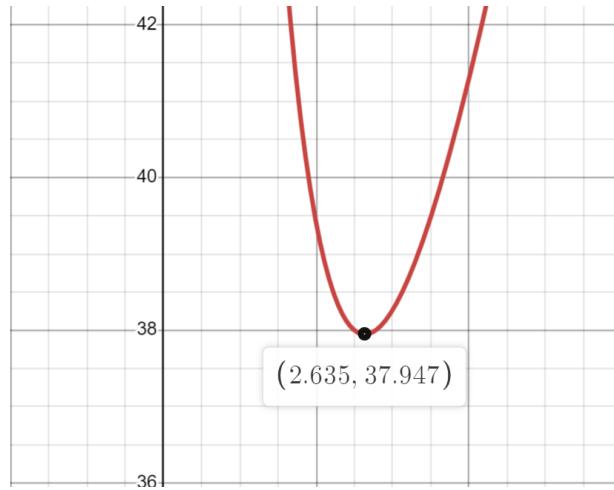


Figure 4.6: Minimized f Value to Minimize Output Delay

Appendix A: DRC Summary

```
=====
== CALIBRE:::DRC-H SUMMARY REPORT
==

Execution Date/Time:      Thu Nov 17 13:18:34 2022
Calibre Version:          v2018.1_36.27      Tue Apr 3 12:54:13 PDT 2018
Rule File Pathname:       /ubc/ece/home/ugrads/a/abeilles/elec402/assignment4/_calibreDRC.rul_
Rule File Title:
Layout System:            GDS
Layout Path(s):           A4Q1_NAND3_circuit.calibre.db
Layout Primary Cell:     A4Q1_NAND3_circuit
Current Directory:        /ubc/ece/home/ugrads/a/abeilles/elec402/assignment4
User Name:                abeilles
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:  4096
DRC Results Database:    A4Q1_NAND3_circuit.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:     A4Q1_NAND3_circuit.drc.summary (REPLACE)
Geometry Flagging:        ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:        COMMENT TEXT + RULE FILE INFORMATION
Layers:                   MEMORY-BASED
Keep Empty Checks:        YES
-----
--- RUNTIME WARNINGS
---
-----
--- ORIGINAL LAYER STATISTICS
---
LAYER NW ..... TOTAL Original Geometry Count = 1  (3)
LAYER ACT ..... TOTAL Original Geometry Count = 2  (6)
LAYER GATEA .... TOTAL Original Geometry Count = 5  (9)
LAYER GATEB .... TOTAL Original Geometry Count = 4  (12)
LAYER GATEAB ... TOTAL Original Geometry Count = 0  (0)
LAYER NIM ..... TOTAL Original Geometry Count = 2  (4)
LAYER PIM ..... TOTAL Original Geometry Count = 2  (4)
LAYER AIL2 ..... TOTAL Original Geometry Count = 1  (9)
```

```

LAYER AIL1 ..... TOTAL Original Geometry Count = 8 (16)
LAYER GATEC ..... TOTAL Original Geometry Count = 0 (0)
LAYER VTH ..... TOTAL Original Geometry Count = 0 (0)
LAYER VTL ..... TOTAL Original Geometry Count = 0 (0)
LAYER GIL ..... TOTAL Original Geometry Count = 3 (3)
LAYER M1A ..... TOTAL Original Geometry Count = 17 (25)
LAYER V0 ..... TOTAL Original Geometry Count = 1 (9)
-----
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
CELL pmos_pcell_CDNS_668719912771 ... TOTAL Result Count = 1 (3)
    RULECHECK RULE_ACT009 ..... TOTAL Result Count = 1 (3)
CELL nmos_pcell_CDNS_668719912770 ... TOTAL Result Count = 1 (3)
    RULECHECK RULE_ACT009 ..... TOTAL Result Count = 1 (3)
CELL A4Q1_NAND3_circuit ..... TOTAL Result Count = 1 (1)
    RULECHECK RULE_NW004A ..... TOTAL Result Count = 1 (1)
-----
--- SUMMARY
---
TOTAL CPU Time:          0
TOTAL REAL Time:         3
TOTAL Original Layer Geometries: 46 (100)
TOTAL DRC RuleChecks Executed: 698
TOTAL DRC Results Generated: 3 (7)

```

Appendix B: LVS Report

```

REPORT FILE NAME:      A4Q1_NAND3_circuit.lvs.report
LAYOUT NAME:
/ubc/ece/home/ugrads/a/abeilles/elec402/assignment4/svdb/A4Q1_NAND3_circuit.sp
('A4Q1_NAND3_circuit')
SOURCE NAME:
/ubc/ece/home/ugrads/a/abeilles/elec402/assignment4/A4Q1_NAND3_circuit.src.net
('A4Q1_NAND3_circuit')
RULE FILE:
/ubc/ece/home/ugrads/a/abeilles/elec402/assignment4/_calibrePEX.rul_
CREATION TIME:        Thu Nov 17 11:06:27 2022
CURRENT DIRECTORY:   /ubc/ece/home/ugrads/a/abeilles/elec402/assignment4
USER NAME:            abeilles
CALIBRE VERSION:     v2018.1_36.27      Tue Apr 3 12:54:13 PDT 2018
***** CELL SUMMARY *****
***** CELL SUMMARY *****


```

Result	Layout	Source
-----	-----	-----
CORRECT	A4Q1_NAND3_circuit	A4Q1_NAND3_circuit

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	10	10	
Instances:	3	3	MN (4 pins)
	3	3	MP (4 pins)
Total Inst:	6	6	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	6	6	
Nets:	8	8	
Instances:	3	3	MP (4 pins)
	1	1	SMN3 (5 pins)
Total Inst:	4	4	

INFORMATION AND WARNINGS

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	6	6	0	0	
Nets:	8	8	0	0	
Instances:	3	3	0	0	MP (PFET)
	1	1	0	0	SMN3
Total Inst:	4	4	0	0	

o Initial Correspondence Points:

Ports: VDD GND A B C Y

SUMMARY

Total CPU Time: 16 sec
 Total Elapsed Time: 20 sec

Appendix C: PEX Netlist

```
* File: A4Q1_NAND3_circuit.pex.netlist
* Created: Wed Nov 16 21:29:29 2022
* Program "Calibre xRC"
* Version "v2018.1_36.27"
*
.include "A4Q1_NAND3_circuit.pex.netlist.pex"
.subckt A4Q1_NAND3_circuit GND A B VDD C Y
*
* Y      Y
* C      C
* VDD    VDD
* B      B
```

```

* A          A
* GND        GND
MM0 N_Y_MM0_d A VDD NET1 PFET L=2e-08 W=1.28e-07 NFIN=4 ADEJ=1.216e-15
+ ASEJ=1.216e-15 PDEJ=3.36e-07 PSEJ=3.36e-07
MM1 N_Y_MM1_d B N_VDD_MM1_s NET1 PFET L=2e-08 W=1.28e-07 NFIN=4 ADEJ=1.216e-15
+ ASEJ=1.216e-15 PDEJ=3.36e-07 PSEJ=3.36e-07
MM2 Y C N_VDD_MM2_s NET1 PFET L=2e-08 W=1.28e-07 NFIN=4 ADEJ=1.216e-15
+ ASEJ=1.216e-15 PDEJ=3.36e-07 PSEJ=3.36e-07
MM5 N_NET4_MM5_d A N_GND_MM5_s NET2 NFET L=2e-08 W=2.08e-07 NFIN=6
+ ADEJ=1.824e-15 ASEJ=1.824e-15 PDEJ=5.04e-07 PSEJ=5.04e-07
MM4 N_NET3_MM4_d B N_NET4_MM4_s NET2 NFET L=2e-08 W=2.08e-07 NFIN=6
+ ADEJ=1.824e-15 ASEJ=1.824e-15 PDEJ=5.04e-07 PSEJ=5.04e-07
MM3 N_Y_MM3_d C N_NET3_MM3_s NET2 NFET L=2e-08 W=2.08e-07 NFIN=6 ADEJ=1.824e-15
+ ASEJ=1.824e-15 PDEJ=5.04e-07 PSEJ=5.04e-07
c_10 A GND 0.01761f
c_17 B GND 0.0140459f
c_32 C GND 0.01761f
*
.includef "A4Q1_NAND3_circuit.pex.netlist.A4Q1_NAND3_CIRCUIT.pxi"
*
.ends
*

```

Appendix D: Area and Density Computation

```

*****
Area and Density
*****
Library      : ELEC402
Cell         : A4Q1_NAND3_circuit
View         : maskLayout
Option        : current to bottom
Stop Level   : 31
Created      : UTC 2022.11.18 05:12:48.719

*****
Region      : ((1.075 -1.775) (1.561 -1.775) (1.561 -1.002) (1.075 -1.002))
TotalArea= 0.375678

Layer        : NW/drawing
TotalArea= 0.099840
Density=    0.265760

```

Appendix E: Schematic Netlist of Worst Case tpLH Circuit

```

// Library name: ELEC402
// Cell name: A4Q2_circuit
// View name: schematic
subckt A4Q2_circuit A B C D GND VDD Y
    M3 (net1 B VDD VDD) pfet w=480n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M2 (Y A net1 VDD) pfet w=480n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M1 (Y C VDD VDD) pfet w=240n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M0 (Y D VDD VDD) pfet w=240n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M7 (net3 D GND GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no

```

```

M6 (net2 C net3 GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
M5 (Y A net2 GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
M4 (Y B net2 GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
ends A4Q2_circuit
// End of subcircuit definition.

// Library name: ELEC402
// Cell name: A4Q2_testbench2
// View name: schematic
I8 (0 B net4 net4 0 net1 OUT) A4Q2_circuit
C0 (OUT 0) capacitor c=10f
V1 (net4 0) vsource dc=1 type=dc
V0 (net1 0) vsource dc=1 type=dc
V2 (B 0) vsource type=pulse val1=0 period=200p delay=0 rise=10p fall=10p width=100p
simulatorOptions options psfversion="1.1.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub

```

Appendix F: Schematic Netlist of Worst Case tpHL Circuit

```

// Library name: ELEC402
// Cell name: A4Q2_circuit
// View name: schematic
subckt A4Q2_circuit A B C D GND VDD Y
    M3 (net1 B VDD VDD) pfet w=480n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M2 (Y A net1 VDD) pfet w=480n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M1 (Y C VDD VDD) pfet w=240n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M0 (Y D VDD VDD) pfet w=240n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M7 (net3 D GND GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M6 (net2 C net3 GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M5 (Y A net2 GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
    M4 (Y B net2 GND) nfet w=360n l=120n as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2
degradation=no
ends A4Q2_circuit
// End of subcircuit definition.

// Library name: ELEC402
// Cell name: A4Q2_testbench
// View name: schematic
I8 (net4 0 net4 D 0 net1 OUT) A4Q2_circuit
C0 (OUT 0) capacitor c=10f
V1 (net4 0) vsource dc=1 type=dc
V0 (net1 0) vsource dc=1 type=dc
V2 (D 0) vsource type=pulse val1=0 vall=1 period=1n delay=0 rise=10p fall=10p width=500p
simulatorOptions options psfversion="1.1.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \

```

```
sensfile="..../psf/sens.output" checklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```