Assignment 2 - Synthesized Verilog Project

ELEC 402

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1.0 Project Description

This project consisted in using Cadence Encounter RTL Compiler to generate a mapped netlist based on a provided library of cells. The same DNS Lookup System Verilog FSM from Assignment 1 was used to create a netlist. The total number of cells and time slack of this FSM was generated by the RTL Compiler, and the generated graphical waves of the mapped Verilog file were compared to the initial waveforms from Assignment 1 to observe timing similarities and functioning.

2.0 Mapped Verilog Generated by RTL Compiler

Once the RTL Compiler had executed the TCL instructions, a *DNSLookup_map.v* file was generated, describing the new gate level description of the synthesized system. Figure 2.1 shows the top level module inside the generated mapped file. The module declaration, inputs, and outputs are identical to that of the declaration from the original *DNSLookup.sv* module.

```
// Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1

// Verification Directory fv/DNSLookup

module DNSLookup(clk, rst, client_req, web_addr, webpage_idx_out,
      tld_addr_out, domain_ip_out, web_ip_out, exec_time, ip_resolved,
      client_res);
  input clk, rst, client_req;
  input [7:0] web_addr;
  output [15:0] webpage_idx_out;
  output [7:0] tld_addr_out, domain_ip_out, web_ip_out, exec_time;
  output ip_resolved, client_res;
```

Figure 2.1: Top Level Module, Inputs, and Outputs of Mapped Verilog of Synthesized Design

Next, we look at a summary of generic gates, including INV, NAND, and NOR gates in the mapped file. As these cells are scattered among others in the code, a list summary of each cell found in the file is included in Appendix A, B, and C for INV, NAND, and NOR gates respectively.

3.0 Mapped Verilog State Transition Waveforms

The generated *DNSLookup_map.v* and *DNSLookup_map.sdf* artifacts are now used to create a ModelSim simulation. The required PDK Verilog file *NanGate_15nm_OCL_functional.v* containing a behavioral description of the standard cells must first be added to the ModelSim project. Then, the SDF entry is added to the simulation.

Once the simulation is run, we compare our results from the original waveforms from Assignment 1 to the waveforms generated from the mapped DNSLookup file. Both waveforms are working similarly. The state transitions of each waveform segment also correspond timing-wise.

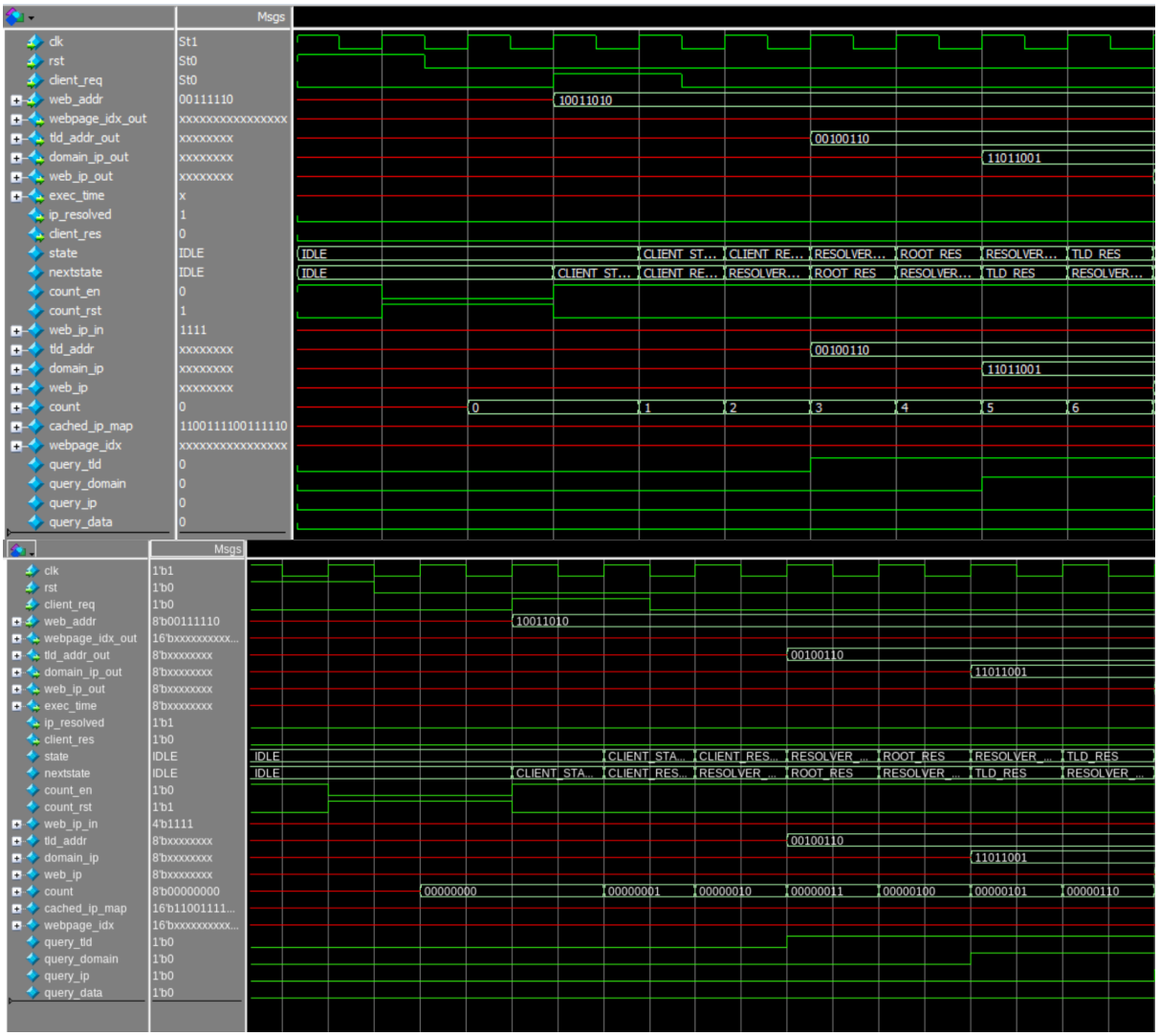

Figure 3.1 a): Comparison of the first client query's original waveforms (top) and the mapped waveform (bottom)

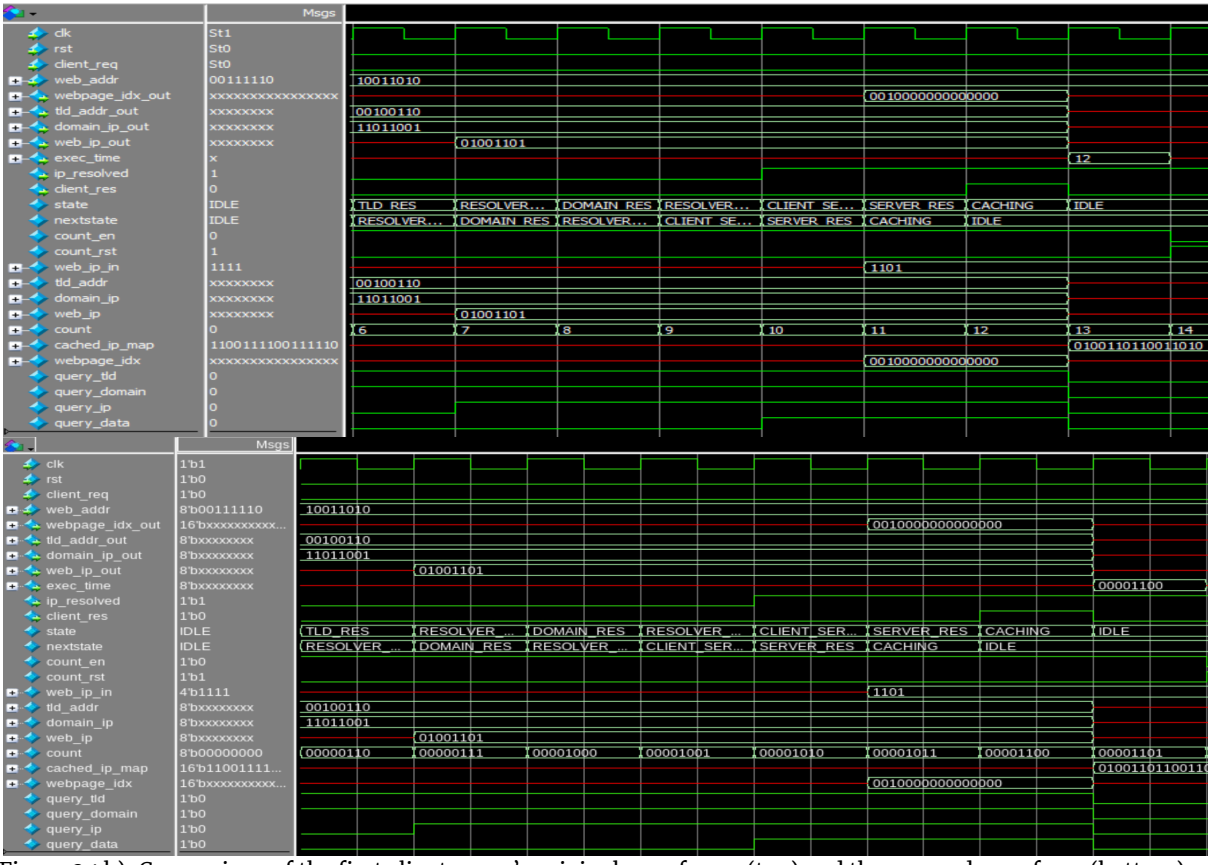

Figure 3.1 b): Comparison of the first client query's original waveforms (top) and the mapped waveform (bottom)

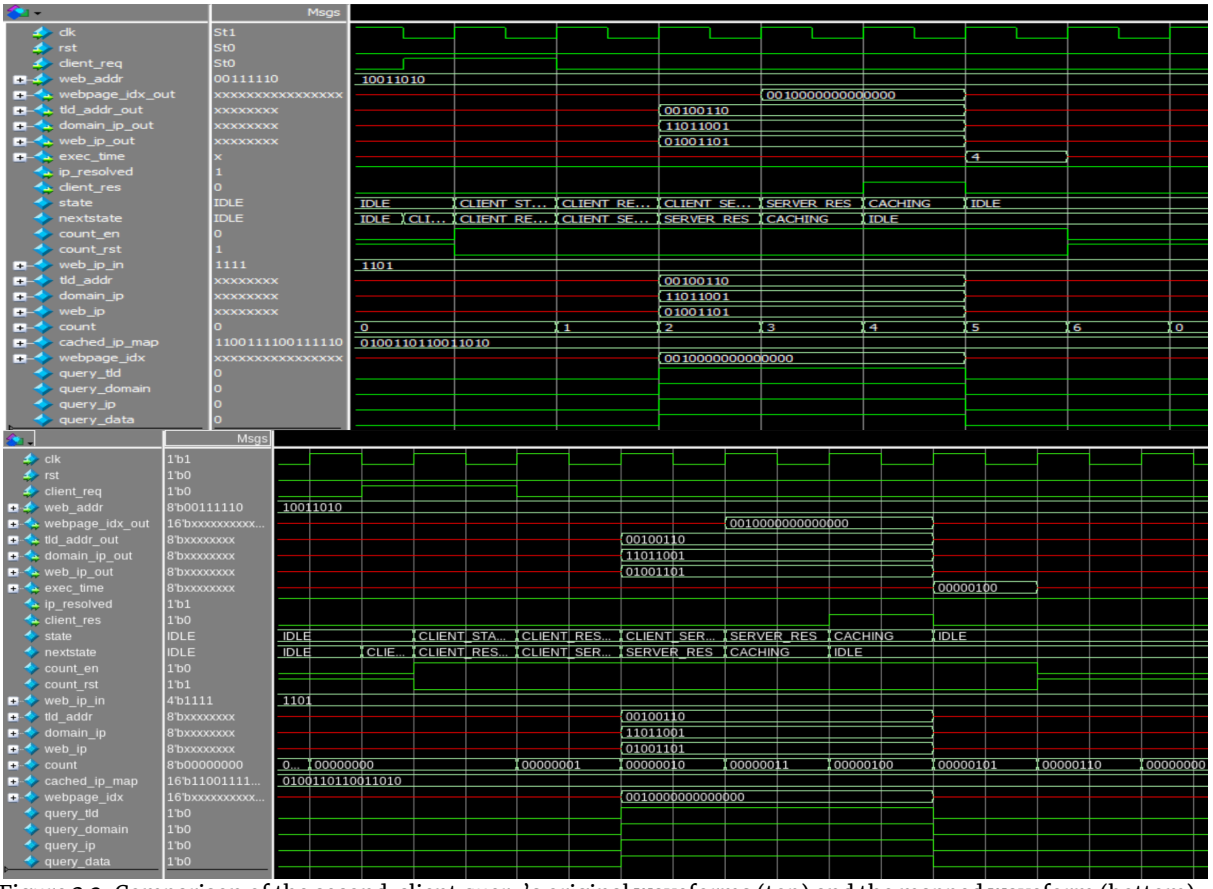

Figure 3.2: Comparison of the second client query's original waveforms (top) and the mapped waveform (bottom)

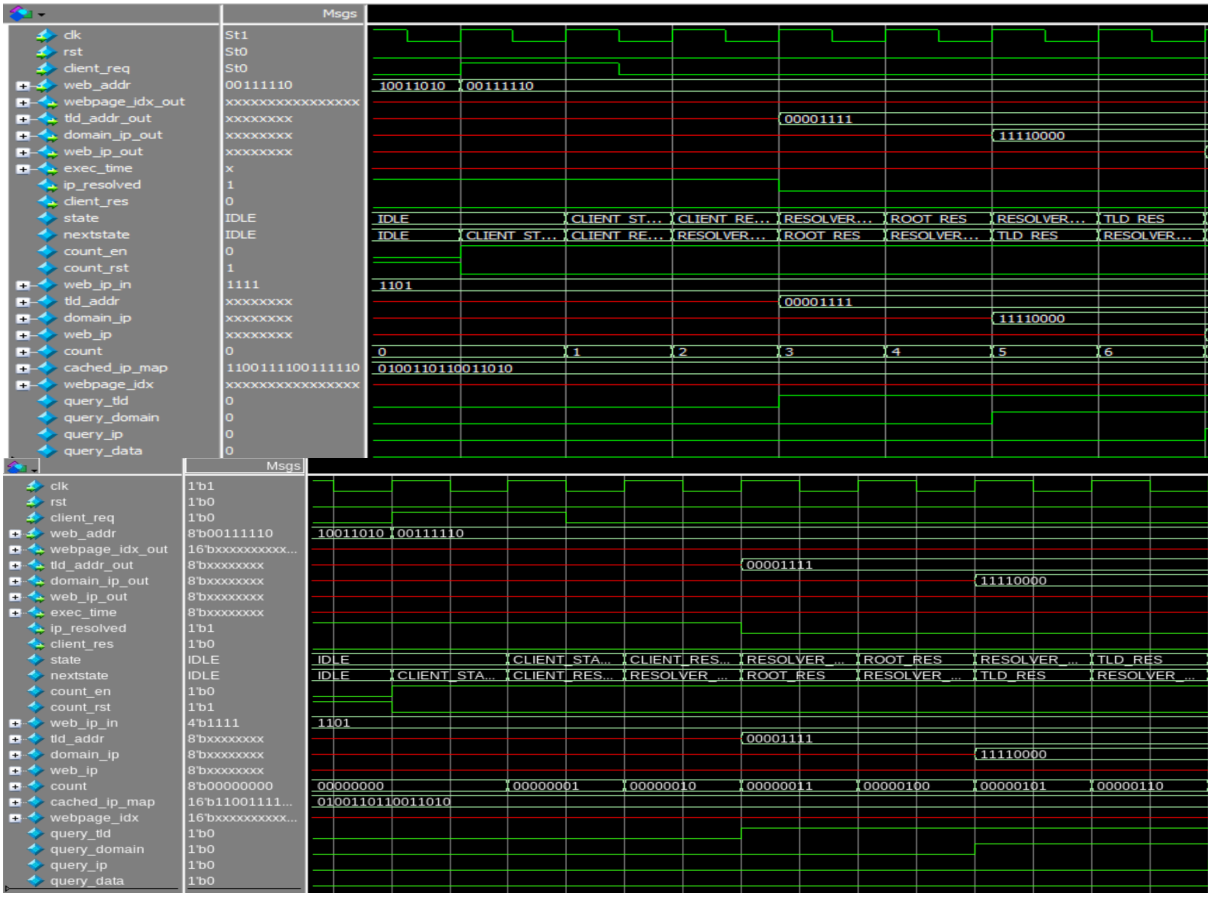

Figure 3.3 a): Comparison of the third client query's original waveforms (top) and the mapped waveform (bottom)

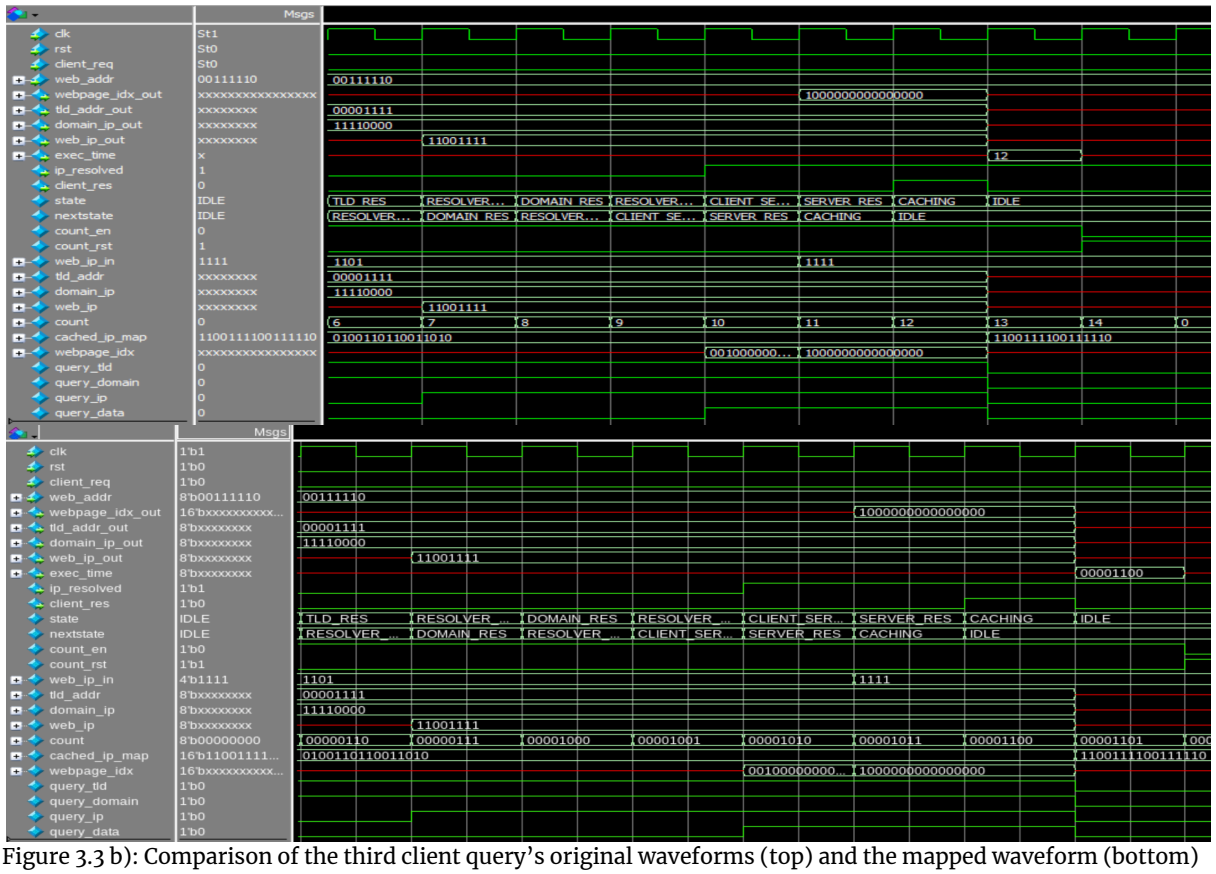

Figure 3.3 b): Comparison of the third client query's original waveforms (top) and the mapped waveform (bottom)

4.0 RTL Compiler Report

When compiled and synthesized by the RTL Compiler, an area report, used cells statistics report, timing report, and power consumption report are generated. Each of these files are important assets to ensure that the system meets the required specifications. For this lab, only the *DNSLookup_area.rpt* report file will be analyzed. As shown in Table 4.1, the total number of cells in the project is 285. The full contents of this file can be found in Appendix D.

Instance	**Cells**	**Cell Area**	**Net Area**	**Total Area**	**Wireload**
DNSLookup	228	92	0	92	<none> (D)
ExecCounter	43	20	0	20	<none> (D)
WebIPToWebData	14	3	0	3	<none> (D)
Total	285	115	0	115	<none> (D)

Table 4.1: Module Area Report Data

Furthermore, the timing slack displayed in the *DNSLookup_timing.rpt* shows a positive time of 19ps, indicating that there are no timing violations.

Appendix A: Mapped Verilog INV Gates

```
INV_X1 g1079(.I (n_473), .ZN (n_72));
INV_X1 g1078(.I (n_474), .ZN (n_69));
INV_X1 g4910(.I (n_248), .ZN (web_ip_in[3]));
INV_X1 g4912(.I (n_247), .ZN (web_ip_in[2]));
INV_X1 g4914(.I (n_246), .ZN (web_ip_in[1]));
INV_X1 g4916(.I (n_245), .ZN (web_ip_in[0]));
INV_X1 g5145(.I (n_454), .ZN (n_4));
INV_X1 g5157(.I (n_70), .ZN (n_1987_BAR));
INV_X1 g5163(.I (n_68), .ZN (n_521));
INV_X1 g5169(.I (n_62), .ZN (n_63));
INV_X1 g5171(.I (n_61), .ZN (n_60));
INV_X1 g5175(.I (state[3]), .ZN (n_57));
INV_X1 g5176(.I (state[1]), .ZN (n_56));
INV_X1 g5177(.I (state[0]), .ZN (n_55));
INV_X1 g1757(.I (nextstate[0]), .ZN (n_51));
INV_X1 g1769(.I (n_40), .ZN (n_41));
INV_X1 g1776(.I (nextstate[1]), .ZN (n_36));
INV_X1 g1815(.I (n_510), .ZN (n_7));
INV_X1 g1816(.I (web_addr[5]), .ZN (n_6));
INV_X1 g1817(.I (web_addr[3]), .ZN (n_5));
INV_X1 g1819(.I (web_addr[1]), .ZN (n_3));
INV_X1 g1820(.I (client_res), .ZN (n_2));
INV_X1 g1821(.I (n_252), .ZN (n_1));
INV_X1 g1779(.I (nextstate[2]), .ZN (n_34));
INV_X1 g1788(.I (n_25), .ZN (n_26));
```

Appendix B: Mapped Verilog NAND Gates

```
NAND3_X1 g4918(.A1 (n_195), .A2 (n_117), .A3 (n_242), .ZN
     (domain_ip_out[0]));
NAND3_X1 g4919(.A1 (n_202), .A2 (n_120), .A3 (n_244), .ZN
     (tld_addr_out[1]));
NAND3_X1 g4920(.A1 (n_193), .A2 (n_116), .A3 (n_241), .ZN
     (tld_addr_out[0]));
NAND3_X1 g4921(.A1 (n_184), .A2 (n_114), .A3 (n_240), .ZN
     (tld_addr_out[6]));
NAND3_X1 g4922(.A1 (n_176), .A2 (n_112), .A3 (n_239), .ZN
     (domain_ip_out[6]));
NAND3_X1 g4923(.A1 (n_156), .A2 (n_84), .A3 (n_235), .ZN
     (domain_ip_out[5]));
NAND3_X1 g4924(.A1 (n_200), .A2 (n_119), .A3 (n_243), .ZN
     (domain_ip_out[4]));
NAND3_X1 g4925(.A1 (n_145), .A2 (n_75), .A3 (n_232), .ZN
     (domain_ip_out[7]));
NAND3_X1 g4926(.A1 (n_168), .A2 (n_97), .A3 (n_238), .ZN
     (domain_ip_out[3]));
NAND3_X1 g4927(.A1 (n_166), .A2 (n_113), .A3 (n_237), .ZN
     (tld_addr_out[7]));
NAND3_X1 g4928(.A1 (n_158), .A2 (n_88), .A3 (n_236), .ZN
     (tld_addr_out[5]));
NAND3_X1 g4929(.A1 (n_151), .A2 (n_83), .A3 (n_234), .ZN
     (domain_ip_out[2]));
NAND3_X1 g4930(.A1 (n_149), .A2 (n_82), .A3 (n_233), .ZN
     (tld_addr_out[4]));
NAND3_X1 g4931(.A1 (n_140), .A2 (n_79), .A3 (n_231), .ZN
     (tld_addr_out[3]));
NAND3_X1 g4932(.A1 (n_133), .A2 (n_76), .A3 (n_230), .ZN
     (domain_ip_out[1]));
NAND3_X1 g4933(.A1 (n_131), .A2 (n_74), .A3 (n_229), .ZN
     (tld_addr_out[2]));
NAND2_X1 g4944(.A1 (n_71), .A2 (n_226), .ZN (n_251));
NAND2_X1 g4957(.A1 (client_res), .A2 (ip_resolved), .ZN (n_226));
NAND4_X1 g4962(.A1 (n_197), .A2 (n_198), .A3 (n_194), .A4 (n_196),
     .ZN (n_221));
NAND4_X1 g4963(.A1 (n_185), .A2 (n_182), .A3 (n_172), .A4 (n_174),
     .ZN (n_220));
NAND4_X1 g4964(.A1 (n_190), .A2 (n_183), .A3 (n_187), .A4 (n_179),
     .ZN (n_219));
NAND4_X1 g4965(.A1 (n_189), .A2 (n_191), .A3 (n_186), .A4 (n_188),
     .ZN (n_218));
NAND4_X1 g4966(.A1 (n_177), .A2 (n_180), .A3 (n_175), .A4 (n_178),
     .ZN (n_217));
NAND4_X1 g4967(.A1 (n_169), .A2 (n_171), .A3 (n_167), .A4 (n_173),
     .ZN (n_216));
NAND4_X1 g4968(.A1 (n_192), .A2 (n_181), .A3 (n_165), .A4 (n_170),
     .ZN (n_215));
NAND4_X1 g4969(.A1 (n_164), .A2 (n_161), .A3 (n_160), .A4 (n_162),
     .ZN (n_214));
```

```
NAND4_X1 g4970(.A1 (n_159), .A2 (n_157), .A3 (n_155), .A4 (n_163),
     .ZN (n_213));
NAND4_X1 g4971(.A1 (n_154), .A2 (n_152), .A3 (n_150), .A4 (n_153),
     .ZN (n_212));
NAND4_X1 g4972(.A1 (n_138), .A2 (n_130), .A3 (n_128), .A4 (n_143),
     .ZN (n_211));
NAND4_X1 g4973(.A1 (n_146), .A2 (n_148), .A3 (n_141), .A4 (n_144),
     .ZN (n_210));
NAND4_X1 g4974(.A1 (n_139), .A2 (n_142), .A3 (n_136), .A4 (n_147),
     .ZN (n_209));
NAND4_X1 g4975(.A1 (n_135), .A2 (n_137), .A3 (n_132), .A4 (n_134),
     .ZN (n_208));
NAND4_X1 g4976(.A1 (n_124), .A2 (n_201), .A3 (n_199), .A4 (n_127),
     .ZN (n_207));
NAND4_X1 g4977(.A1 (n_125), .A2 (n_129), .A3 (n_123), .A4 (n_126),
     .ZN (n_206));
NAND2_X1 g5013(.A1 (n_72), .A2 (n_118), .ZN (n_205));
NAND2_X1 g5014(.A1 (n_521), .A2 (n_118), .ZN (n_203));
NAND2_X1 g5015(.A1 (n_69), .A2 (n_118), .ZN (n_204));
NAND2_X1 g5098(.A1 (n_474), .A2 (n_273), .ZN (n_120));
NAND2_X1 g5099(.A1 (n_474), .A2 (n_394), .ZN (n_119));
NAND2_X1 g5101(.A1 (n_68), .A2 (n_349), .ZN (n_117));
NAND2_X1 g5102(.A1 (n_474), .A2 (n_262), .ZN (n_116));
NAND2_X1 g5104(.A1 (client_res), .A2 (n_330), .ZN (n_114));
NAND2_X1 g5105(.A1 (n_68), .A2 (n_338), .ZN (n_113));
NAND2_X1 g5106(.A1 (n_474), .A2 (n_416), .ZN (n_112));
NAND2_X1 g5121(.A1 (n_474), .A2 (n_383), .ZN (n_97));
NAND2_X1 g5130(.A1 (n_513), .A2 (n_318), .ZN (n_88));
NAND2_X1 g5134(.A1 (n_68), .A2 (n_404), .ZN (n_84));
NAND2_X1 g5135(.A1 (client_res), .A2 (n_374), .ZN (n_83));
NAND2_X1 g5136(.A1 (n_474), .A2 (n_306), .ZN (n_82));
NAND2_X1 g5139(.A1 (n_474), .A2 (n_295), .ZN (n_79));
NAND2_X1 g5142(.A1 (n_68), .A2 (n_360), .ZN (n_76));
NAND2_X1 g5143(.A1 (n_474), .A2 (n_427), .ZN (n_75));
NAND2_X1 g5144(.A1 (client_res), .A2 (n_286), .ZN (n_74));
NAND2_X1 g5150(.A1 (n_62), .A2 (n_61), .ZN (n_505));
NAND2_X1 g5165(.A1 (n_57), .A2 (state[2]), .ZN (n_67));
NAND2_X1 g5167(.A1 (state[0]), .A2 (state[1]), .ZN (n_65));
NAND2_X1 g5168(.A1 (state[3]), .A2 (state[2]), .ZN (n_64));
NAND2_X1 g5173(.A1 (n_56), .A2 (state[0]), .ZN (n_59));
NAND2_X1 g5174(.A1 (n_55), .A2 (state[1]), .ZN (n_58));
NAND2_X1 g1761(.A1 (n_47), .A2 (n_69), .ZN (n_49));
NAND3_X1 g1762(.A1 (n_69), .A2 (n_46), .A3 (n_521), .ZN (n_48));
NAND2_X1 g1765(.A1 (n_72), .A2 (n_43), .ZN (n_45));
NAND2_X1 g1766(.A1 (n_42), .A2 (n_505), .ZN (n_44));
NAND2_X1 g1767(.A1 (n_518), .A2 (n_40), .ZN (n_43));
NAND2_X1 g1768(.A1 (n_518), .A2 (n_41), .ZN (n_42));
NAND2_X1 g1783(.A1 (n_22), .A2 (n_7), .ZN (n_31));
NAND4_X1 g1791(.A1 (n_69), .A2 (n_1), .A3 (n_521), .A4 (n_1987_BAR),
     .ZN (n_23));
```

Appendix C: Mapped Verilog NOR Gates

```
  NOR2_X1 g4956(.A1 (n_69), .A2 (ip_resolved), .ZN (n_227));
  NOR4_X1 g5146(.A1 (n_63), .A2 (state[0]), .A3 (state[1]), .A4
       (client_req), .ZN (n_454));
  NOR2_X1 g5147(.A1 (n_66), .A2 (n_65), .ZN (n_513));
  NOR2_X2 g5148(.A1 (n_60), .A2 (n_64), .ZN (client_res));
  NOR2_X1 g5149(.A1 (n_63), .A2 (n_65), .ZN (n_253));
  NOR2_X1 g5152(.A1 (n_67), .A2 (n_65), .ZN (n_473));
  NOR2_X1 g5154(.A1 (n_66), .A2 (n_60), .ZN (n_515));
  NOR2_X1 g5155(.A1 (n_67), .A2 (n_60), .ZN (n_506));
  NOR2_X1 g5156(.A1 (n_63), .A2 (n_58), .ZN (n_518));
  NOR2_X1 g5158(.A1 (n_63), .A2 (n_59), .ZN (n_70));
  NOR2_X1 g5159(.A1 (n_67), .A2 (n_58), .ZN (n_510));
  NOR2_X1 g5160(.A1 (n_67), .A2 (n_59), .ZN (n_252));
  NOR2_X1 g5162(.A1 (n_66), .A2 (n_58), .ZN (n_474));
  NOR2_X1 g5164(.A1 (n_66), .A2 (n_59), .ZN (n_68));
  NOR2_X1 g5170(.A1 (state[3]), .A2 (state[2]), .ZN (n_62));
  NOR2_X1 g5172(.A1 (state[1]), .A2 (state[0]), .ZN (n_61));
  NOR2_X1 g1755(.A1 (n_51), .A2 (rst), .ZN (n_53));
  NOR2_X1 g1756(.A1 (n_50), .A2 (rst), .ZN (n_52));
  NOR4_X1 g1763(.A1 (n_510), .A2 (n_506), .A3 (n_515), .A4 (n_44), .ZN
       (n_47));
  NOR3_X1 g1764(.A1 (n_513), .A2 (n_515), .A3 (n_45), .ZN (n_46));
  NOR4_X1 g1770(.A1 (n_39), .A2 (n_26), .A3 (n_27), .A4 (n_16), .ZN
       (n_40));
  NOR2_X1 g1774(.A1 (n_36), .A2 (rst), .ZN (n_38));
  NOR4_X1 g1775(.A1 (n_32), .A2 (n_29), .A3 (n_24), .A4 (n_28), .ZN
       (n_37));
  NOR2_X1 g1778(.A1 (n_34), .A2 (rst), .ZN (n_35));
  NOR4_X1 g1792(.A1 (n_252), .A2 (n_513), .A3 (n_506), .A4 (n_253), .ZN
       (n_22));
```

Appendix D: DNSLookup_area.rpt

```
============================================================
  Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:           Oct 09 2022  03:50:33 pm
  Module:                 DNSLookup
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   worst_low (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

    Instance      Cells  Cell Area  Net Area  Total Area  Wireload
-----------------------------------------------------------------------
DNSLookup           228         92         0          92    <none> (D)
  ExecCounter        43         20         0          20    <none> (D)
  WebIPToWebdata     14          3         0           3    <none> (D)

 (D) = wireload is default in technology library
```