

Assignment 3 – The MOS Transistor & Cadence

ELEC 402

Isabelle André – 12521589

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1.0 Transistor Size Calculation

In the circuits in Figure 2.1, the widths of the pull-down transistors are designed such that $V_{OL} = 0.1V$. In each of these circuits, we assume that there is no body effect, therefore $V_T = V_{TO}$ when $V_{SB}=0$.

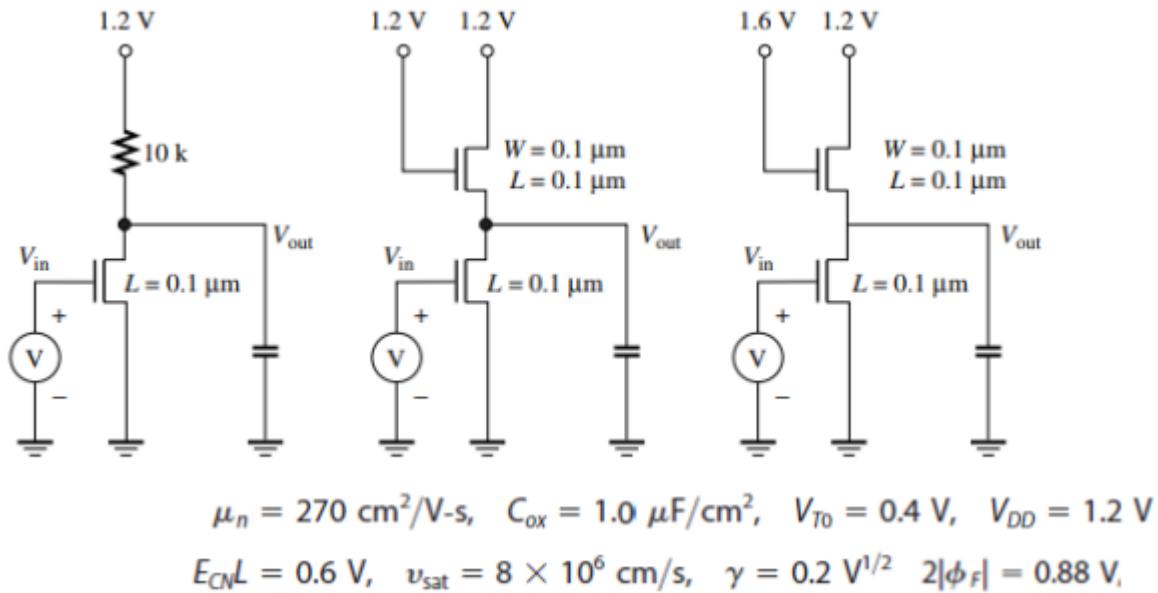


Figure 2.1: Resistive Load, Saturated Enhancement, Less Saturated Enhancement Load Inverters

1.1 Resistive-Load Inverter Design

We first take a look at the extremes of the transistor operation. At one extreme, V_{in} is low and the transistor is off hence no current flow across the resistor and $V_{OH} = VDD$.

At the other extreme, the input voltage is high, therefore we use $V_{in} = V_{OH} = VDD$ in the expression of $I_{out} = I_{load}$ to find V_{OL} :

$$I_R = I_{DS}(\text{linear})$$

In the Linear region:

$$V_{DS} < \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L}$$

$$I_{DS}(\text{lin}) = \frac{W}{L} * \frac{\mu_e C_{ox}}{(1 + \frac{V_{DS}}{E_c L})} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}$$

We use the fact that $I_{DS} = \frac{V_{DD} - V_{OL}}{R_L}$ to obtain:

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{W}{L} * \frac{\mu_n C_{OX}}{(1 + \frac{V_{DS}}{E_c L})} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}$$

We assume that $V_{in} = V_{DD}$, in which case, $V_{GS} = V_{in} = V_{DD}$ and $V_{DS} = V_{out} = V_{OL}$. This allows us to solve for W using the equation above: $W = 0.6337 \mu m$.

1.2 Saturated-Enhancement-Load Inverter Design

This inverter features a diode-connected transistor in constant saturation to alleviate the area problem caused by the resistive-load inverter.

As the load inverter is in saturation, their drain current equations are equivalent:

$$I_{DSL}(\text{linear}) = I_{DSI}(\text{saturation})$$

In the Saturation region:

$$I_{DSL}(\text{sat}) = W_L v_{SAT} C_{OX} * \frac{(V_{GSL} - V_T)^2}{(V_{GSL} - V_T) + E_c L}$$

Knowing that $V_{GSL} = V_{DD} - V_{out}$, we once again solve for the inverter width using the current of the load: $W = 0.17372 \mu m$.

1.3 Less Saturated-Enhancement-Load Inverter Design

This inverter has a higher voltage at the load gate than the maximum output of V_{DD} , therefore resulting in the upper transistor being less saturated than in the previous case.

Knowing that $V_{GSL} = V_G - V_{out}$ for the saturated load, we use the same saturation current equation as before and equate the linear current of the inverter to the saturation current of the load to solve for the transistor width: $W = 0.32805 \mu m$.

1.4 Results

The first circuit displayed a resistive-load inverter, allowing an output voltage up to V_{DD} when V_{in} is low. However the use of resistors is not recommended as they limit transistor speed and size, causing a larger width. Replacing the resistor by a saturated load allows for a faster and smaller circuit, however the output voltage is now restricted by the voltage threshold of the transistor, at $V_{DD} - V_T$. Finally, the gate voltage of the load transistor is raised V_T higher than V_{DD} to raise the output voltage back up to V_{DD} , though incurring an increase in transistor width again.

2.0 Buffer

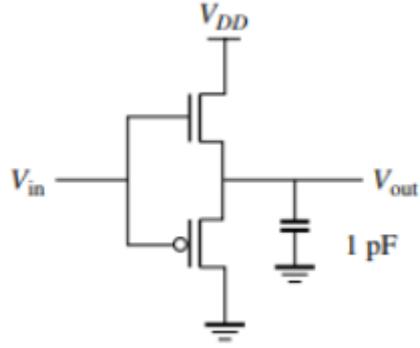


Figure 2.1: Non-inverting buffer

2.1 Function and Output Voltage Swing

This circuit represents a voltage follower or non-inverting buffer circuit. When V_{in} is high, the NMOS is on and pulls the output up to V_{DD} , while the PMOS is cut off. Therefore, V_{OH} is at most $V_{DD} - V_{TN}$. When V_{in} is low, the PMOS pulls down V_{out} while the NMOS is cut off and V_{OL} is at least V_{TP} .

$$V_{OH} \leq V_{DD} - V_{TN}$$

$$V_{OL} \geq V_{TP}$$

Therefore, the Voltage swing is $V_{Swing} = V_{DD} - V_{TN} - |V_{TP}|$

2.2 DC Voltage Transfer Characteristic

- Starting at input low, from $V_{in} = 0V$ to $V_{TP} + V_{TN}$, the NMOS is off as its voltage threshold is not met, and the PMOS is on, pulling down V_{out} to V_{TP} .
- From $V_{in} = V_{TP} + V_{TN}$ to V_{DD} , the NMOS turns on as the PMOS turns off, and the voltage increases as V_{in} increases until maximum V_{OH} is reached at $V_{DD} - V_{TN}$.
- Now starting at input high, from $V_{in} = V_{DD}$ to $V_{DD} - V_{TN} - V_{TP}$, the PMOS remains off and V_{out} remains at $CDD - V_{TN}$.
- From $V_{in} = V_{DD} - V_{TN} - V_{TP}$ to $0V$, the PMOS turns on and pulls down V_{out} to V_{TP} .

As the voltage transitions to high and low differ, hysteresis can be observed in the transition plot.

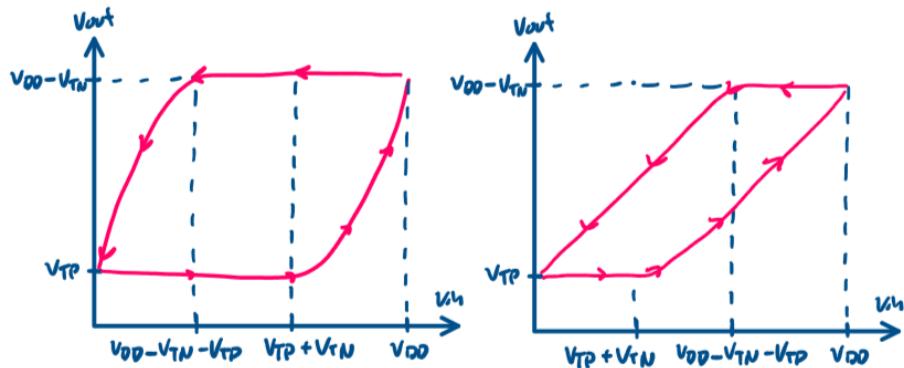


Figure 2.2: Buffer hysteresis loop with a) $VTN + VTP < VDD - VTP - VTN$, b) $VTN + VTP > VDD - VTP - VTN$

2.3 Gain

As this is a voltage follower circuit, the output voltage follows the input voltage, resulting in a gain near $A_v = \frac{V_{OUT}}{V_{IN}} = 1$.

To define a valid logic gate, the gain must be greater than 1 for high gain regions, and must have a high gain region between two low gain regions. Furthermore, the output must swing from valid low to valid high, signifying that low output should be below V_{IL} , and high output should be above V_{IH} . As this gate does not meet these requirements, this is not a valid gate, and does not have the needed noise rejection or regenerative properties.

2.4 CAD Plotting of VTC

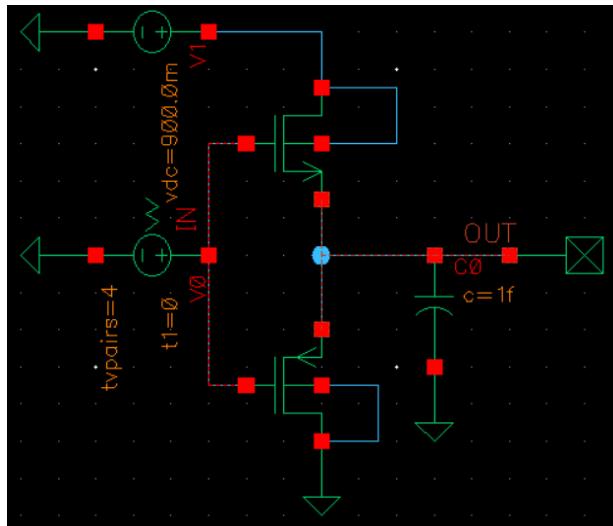


Figure 2.3: Buffer Cadence Schematic

The voltage transfer characteristics of this buffer and its hysteresis loop are shown in Figure 2.3. The left plot shows the V_{IN} and V_{OUT} responses vs time, while the right plot displays the hysteresis loop of the buffer. Body effect is neglected by connecting the PMOS bulk to VDD and NMOS bulk to GND. We assume that $VDD = 0.9\text{V}$, use two fingers per transistor, and set $C = 0\text{F}$.



Figure 2.4: Simulated CAD plot of the buffer's VTC hysteresis loop @ $C = 0\text{F}$

3.0 Body Effect and Channel Length Modulation

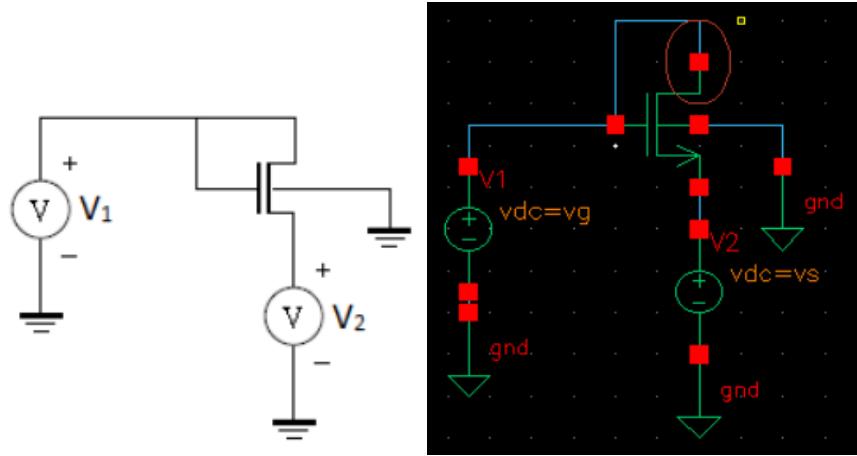


Figure 3.1: a) Diode-connected NMOS transistor, b) Diode-connected NMOS transistor CAD

The circuit in Figure 3.1 is used to measure the effective value of the body effect factor γ by measuring VT at various source voltages V2 from 0-0.8V.

3.1 Body Effect

A DC sweep is conducted for VG for values in the range of 0-1.2V. The value of VT is determined graphically for each curve, as the approximate point at which the current begins to rise for different source voltages. Source values of V2 are used ranging from 0-0.8V.

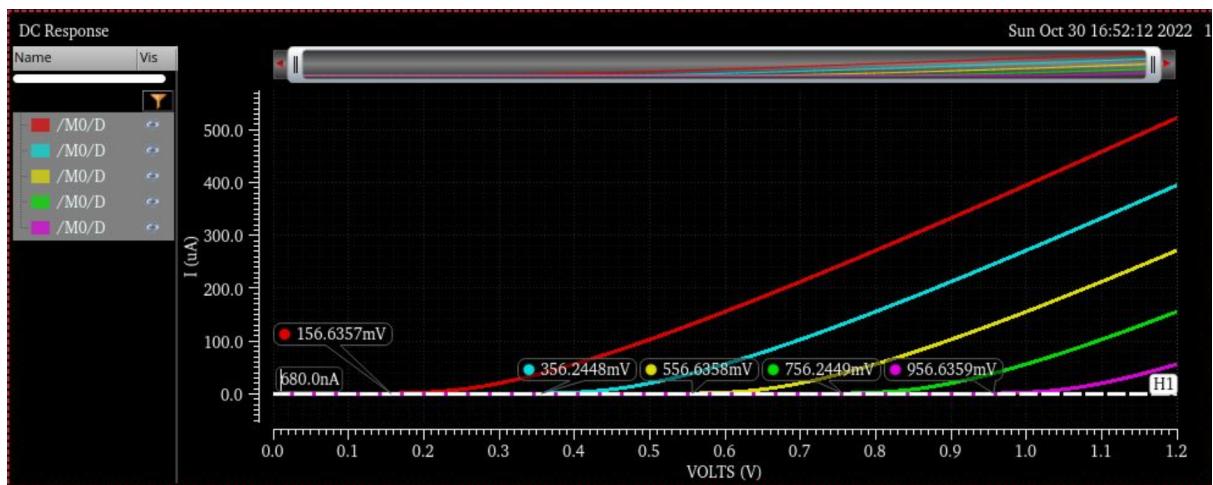


Figure 3.2: DC Sweep simulation of diode-connected transistor at $V_D = V_G$ for varying V_S

A diode connected transistor is always in saturation. To calculate V_{TO} , we measure the threshold voltage at $V_2 = 0V$, and use $V_{SB} = V_2 = 0V$ and $2\phi F = 0.88V$ with the following threshold and body effect formula:

$$V_T = V_{T0} + \gamma \sqrt{V_{SB} + |2\phi F|} - \sqrt{|2\phi F|}$$

As $V_T = V_{TO}$ when $V_{SB} = 0V$ we can conclude that $V_{TO} = V_T = 0.135V$ as measured on the plot.

As the X axis of the plot represents V_{GS} in a V_G vs I_D plot, we must determine where in the current curve is $V_{GS} = V_T$, as this plot no longer holds true for $V_G = V_{GS}$ once V_S turns on. For 15nm PDK and 2 fins, it is known that $W = 68 \text{ nm}$, and $L = 20 \text{ nm}$. Using the constant current method:

$$I_{crit} = 0.1\mu * \frac{W}{L} * 2 = 0.68 \mu A$$

I_{crit} defines the value at which to measure the voltage for $V_{GS} = V_T$, and is shown in Figure 3.2 as the horizontal cursor. From this plot, we see the values at which $V_{GS} = V_T$, and can calculate V_G as $V_G = V_{GS} + V_S$.

Using the voltage threshold and body effect formula above, we can solve for the body effect factor at every value of V_S , using $V_{SB} = V_S$, $V_T = V_{GS}$, $V_{TO} = 0.168V$, and $2\phi F = 0.88V$.

V_S (mV)	0	200	400	600	800
V_G (mV)	156.6357	356.7448	556.7958	756.8249	956.9359
$V_T = V_{GS}$ (mV)	156.6357	156.7448	156.7958	156.8249	156.9359
$\gamma (V^{1/2})$	X	7.71E-3	8E-3	7.72E-3	1.06E-2

Table 3.1: V_T and γ and at different fixed V_2 values, sweeping V_1 from 0-1.2V.

The average body effect value is found to be $\gamma = 8.5149E - 3 V^{1/2}$

3.2 Channel Length Modulation

In saturation when in presence of channel length modulation, the saturation current I_{DS} continues to increase slightly with V_{DS} . The previous testbench is modified as shown in Figure 3.3, where the drain and gate are connected to two different sources.

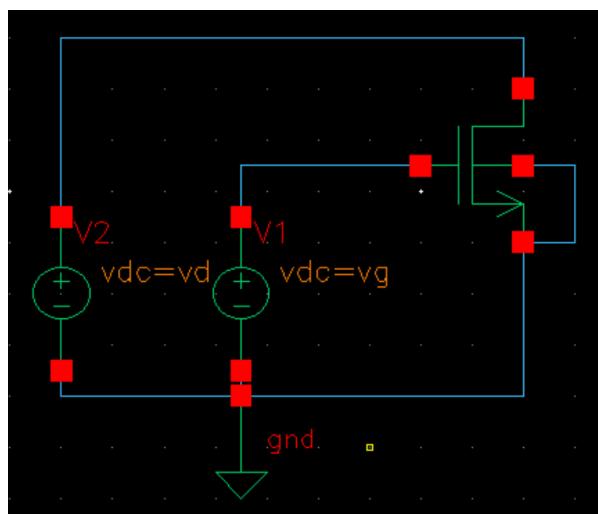


Figure 3.3: Channel Length Modulation Cadence Schematic

Once again, a DC sweep is conducted for VG for values in the range of 0-2V. As this circuit connects the bulk and source to ground, there is no body effect in this circuit, therefore VSB = 0 V. Keeping the source at VG constant at 1V, the following simulation is obtained in Figure 3.4.

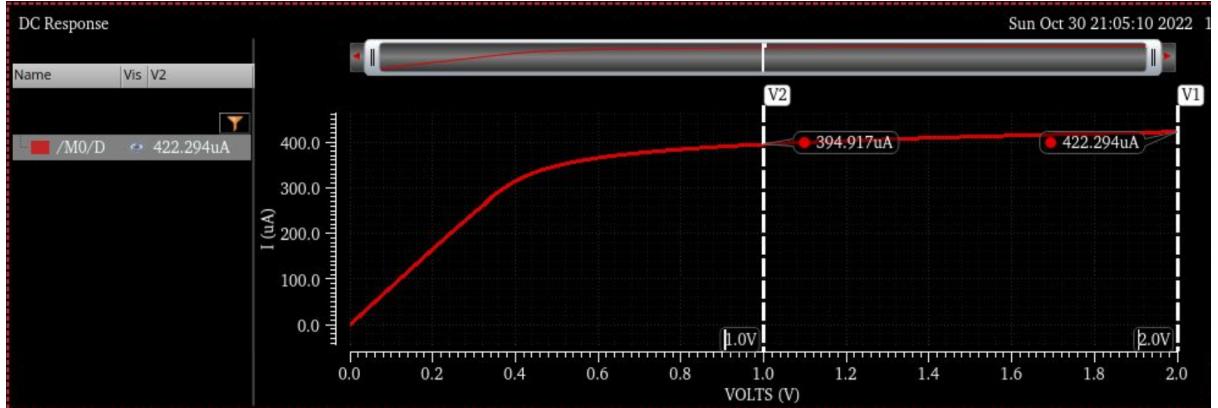


Figure 3.4: DC Sweep simulation of circuit of ID vs VD with VG = 1V

Two measurements are taken on the current curve in the saturation region at VG = 1V, and VG = 2V.

VD = VDS (V)	1	2
ID = IDS (uA)	394.917	422.294

Table 3.2: IDS at two VG points in saturation on a DC Sweep of VD

Using these two points, we can take a ratio of the saturation current equation, allowing us to cancel the remaining terms until only IDS, VDS, and the channel length modulation factor is left.

In the Saturation region:

$$I_{DS}(sat \& CLM) = W_L v_{SAT} C_{OX} * \frac{(V_{GS} - V_T)^2 (1 + \lambda V_{DS})}{(V_{GS} - V_T) + E_c L}$$

Taking a ratio of the two points in Table 3.2:

$$\frac{I_{DS1}}{I_{DS2}} = \frac{W_L v_{SAT} C_{OX} * \frac{(V_{GS1} - V_T)^2 (1 + \lambda V_{DS1})}{(V_{GS1} - V_T) + E_c L}}{W_L v_{SAT} C_{OX} * \frac{(V_{GS2} - V_T)^2 (1 + \lambda V_{DS2})}{(V_{GS2} - V_T) + E_c L}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}$$

Knowing IDS1, IDS2, VDS1, and VDS2, the channel length modulation value can be solved:

$$\lambda = 0.0744.$$

4.0 MOS Transistor Capacitance Calculation

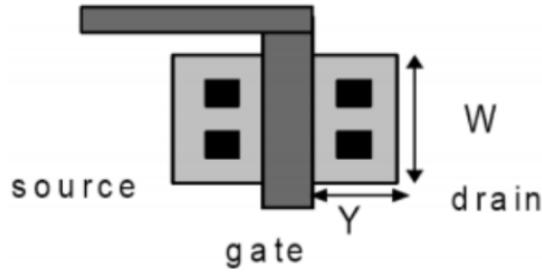


Figure 4.1: MOST Transistor layout

The layout in Figure 4.1 is implemented in a 180nm technology, with $W = 900 \text{ nm}$, $L = 180 \text{ nm}$, and a source/drain dimension of $Y = 800 \text{ nm}$, lateral diffusion of 22 nm, and $\text{tox} = 40 \text{ A}^{-1} = 40E-10 \text{ m}$.

4.1 Gate Capacitance and Overlap Effects

The worst case gate capacitance per unit width, $C_g (\text{fF}/\mu\text{m})$ is computed, along with C_{GS} , C_{GTD} , C_{GB} in linear, saturation, and cutoff, including overlap effects.

The oxide capacitance C_{ox} is first computed as $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\epsilon_0}{40E-10} = 8.63 \text{ F/m}^2$.

The gate capacitance can be found using the given transistor length:

$$C_g = C_{ox}L = (8.63) * 180E - 9 = 1.55 \text{ fF}/\mu\text{m}$$

Assuming that the thickness of the gate and fringe capacitance are negligible ($C_f = 0$), the overlap capacitance for each overlap can be calculated using the C_{ox} and the lateral diffusion.

$$C_{ol} = C_{ox}L_D = 0.19 \text{ fF}/\mu\text{m}$$

Finally, the gate-source, gate-drain, and gate-bulk capacitances can be found in each region of operation:

	Cutoff	Linear	Saturation
$C_{GS} (\text{fF}/\mu\text{m})$	$C_{ol} = 0.19$	$\frac{1}{2}C_g + C_{ol} = 0.96$	$\frac{2}{3}C_g + C_{ol} = 1.22$
$C_{GD} (\text{fF}/\mu\text{m})$	$C_{ol} = 0.19$	$\frac{1}{2}C_g + C_{ol} = 0.96$	$C_{ol} = 0.19$
$C_{GB} (\text{fF}/\mu\text{m})$	$C_g = 1.55$	X	X

Table 4.1: Capacitance in Cutoff, Linear, and Saturation

4.2 Gate Capacitance and Overlap Effects

The worst-case junction capacitance C_j can be found with $N_A = 3E16/\text{cm}^3$ and $N_D = 3E19/\text{cm}^3$, and $x_j = 300 \text{ nm}$.

Assuming that $\frac{kT}{q} = 25 \text{ mV}$ and $n_i = 1.5E10/\text{cm}^3$ voltage asymptote is first calculated:

$$\phi_B = \frac{kT}{q} \ln \left| \frac{N_A N_D}{n_i^2} \right| = 0.8981$$

Next, the zero-bias junction capacitance C_{j0} is calculated, where $\epsilon_{si} = 11.7\epsilon_0$.

$$C_{j0} = \sqrt{\frac{\epsilon_{si} q N_A N_D}{2\phi_B (N_A + N_D)}} = 0.526 \text{ fF}/\mu\text{m}^2$$

To find the junction capacitance per unit width, we multiply the capacitance by the bottom length and sidewall length.

$$C_j = C_{j0}(Y + x_j) = 0.526 * (800\text{nm} + 300\text{nm}) = 0.5786 \text{ fF}/\mu\text{m}$$

4.3 Drain Junction Capacitance

To calculate drain junction capacitance at $m=0.5$, we use the equation for drain junction:

$$C_J = \frac{C_j}{(1 - \frac{V_j}{\phi_B})^m}$$

where $C_j = 0.5786 \text{ fF}/\mu\text{m}^2$ and $\phi_B = 0.8981 \text{ V}$.

At $V_D = 1.8V$ and $V_B = 0V$:

$$V_J = V_B - V_D = -1.8 \text{ V.}$$

$$C_J = \frac{0.5786}{(1 - \frac{-1.8}{0.8981})^{0.5}} = 0.3338 \text{ fF}$$

At $V_D = 0V$ and $V_B = 0V$:

$$V_J = V_B - V_D = 0 \text{ V.}$$

$$C_J = \frac{0.5786}{(1 - \frac{0}{0.8981})^{0.5}} = 0.5786 \text{ fF}$$

5.0 FO4 Inverter Simulation

5.1 Average FO4 Inverter Propagation Delay

Using the circuit in Figure 5.1, a corresponding Cadence test bench such as in Figure 5.2 can be created to simulate the average FO4 inverter propagation delay obtained from a waveform simulation.

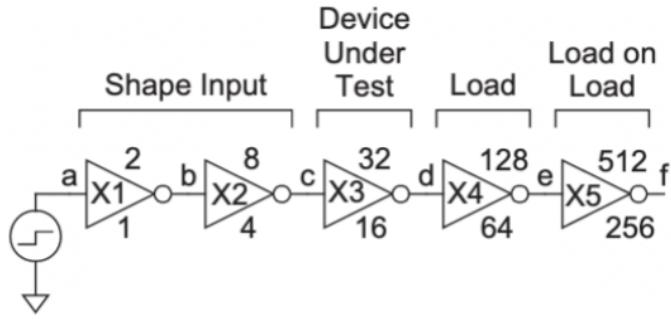


Figure 5.1: Circuit Measuring Propagation Delay of FO4 Inverter

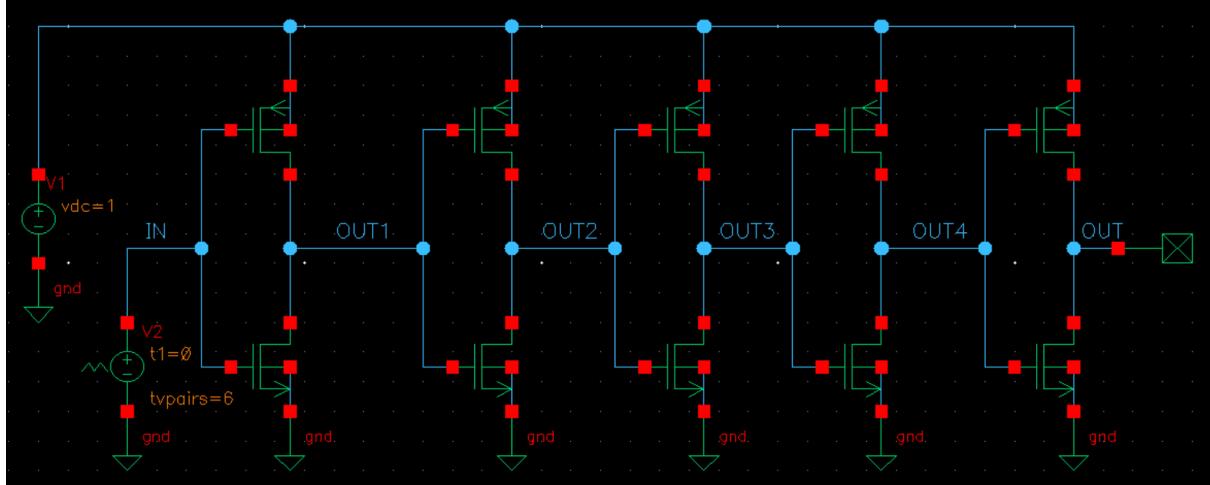


Figure 5.2: Cadence Circuit to Measure Propagation Delay of FO4 Inverter

Probing the input and 5 outputs of the circuit, the following transient simulation waveform in Figure 5.3 is obtained when inputting a VDC of 1V, and 6 pair of points: [(0s, 0V), (10ps, 0V), (11ps, 1V), (150ps, 1V), (151ps, 0V), (180ps, 0V)].

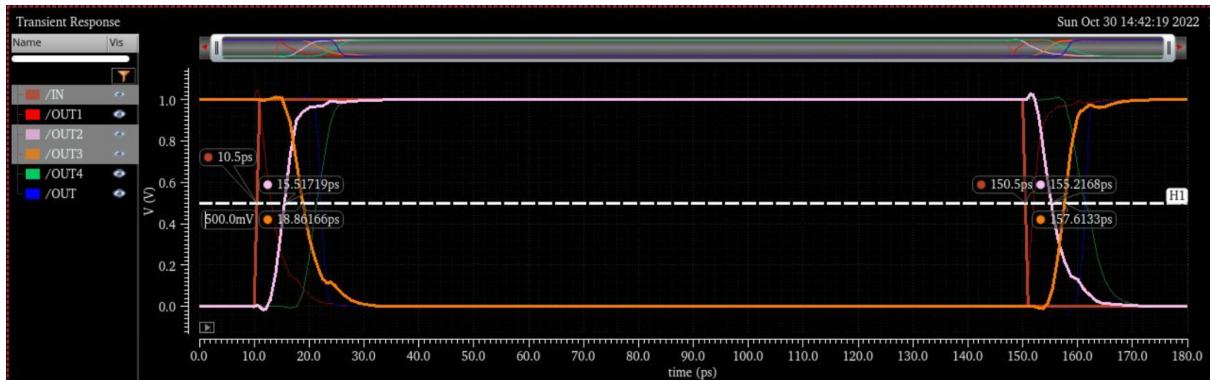


Figure 5.3: Transient Simulation of the FO4 Inverter Testbench

Using the simulation, we find that OUT2 crosses the midpoint of VDD at 15.52 ps, and OUT3 crosses the midpoint at 18.86 ps, and once again at 155.22 ps and 157.61 ps.

Therefore, the falling time is $t_{pHL} = 18.86 - 15.52 = 3.34 \text{ ps}$, and the rising time is $t_{pLH} = 157.61 - 155.22 = 2.39 \text{ ps}$. Therefore, we can calculate the average delay time as:

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2} = 2.865 \text{ ps}$$

5.2 Effective Gate Capacitance

Next, the previous testbench is modified as shown in Figure 5.4 to find the effective gate capacitance in fF/um for delay purposes. The equivalent schematics in Figure 5.4 was created in Cadence to simulate the outputs using a pulse function.

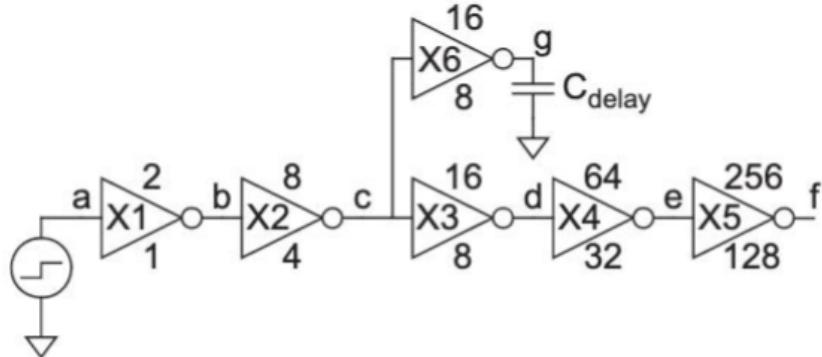


Figure 5.4: Circuit Measuring Effective Gate Capacitance

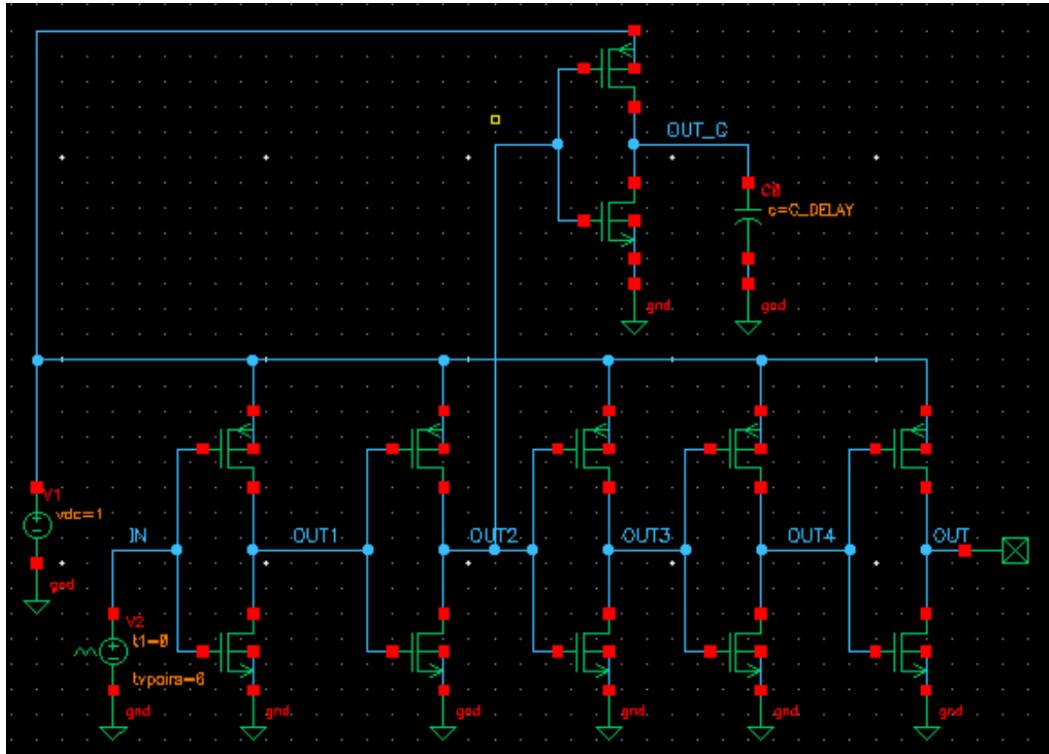


Figure 5.4: Cadence Circuit to Measure Effective Gate Capacitance

The transient analysis shown in Figure 5.5 is simulated using the Cadence Testbench and the capacitance delay C_DELAY is tuned to approximately match the rise and fall times of the capacitance output C_OUT and $OUT3$. Using these values, the effective input capacitance of $X4$ will be found. Probing the input and 6 outputs of the circuit, the following transient simulation waveform in Figure 5.5 is obtained when inputting a VDC of 1V, and 6 pair of points: $[(0s, 0V), (10ps, 0V), (11ps, 1V), (150ps, 1V), (151ps, 0V), (180ps, 0V)]$.

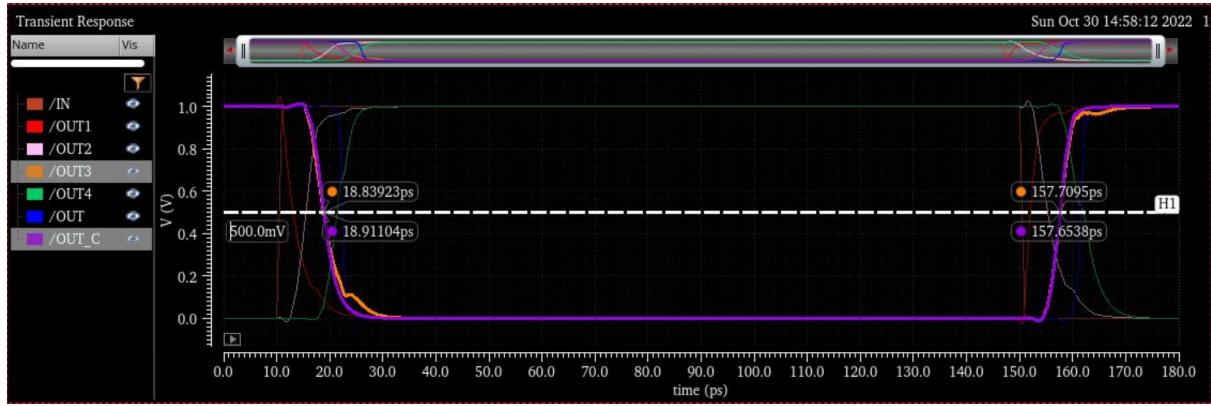


Figure 5.5: Transient Simulation of the Gate Capacitance Testbench

Using the above simulation, we find that $C_{\text{DELAY}} = 12\text{fF}$. Since $H_{\text{fin}} = 30\text{nm}$, $W_{\text{fin}} = 8\text{nm}$, $W_{\text{eff}} = (2*H_{\text{fin}} + W_{\text{fin}})*n_{\text{fin}} = 68 \text{ nm/fin}$, and the capacitance per micron of gate width can then be found, where $C_{\text{delay}} = 12\text{fF}$ and $n_{\text{fin}} = 64$:

$$C_g = 1\mu m * \frac{C_{\text{delay}}}{68\text{nm}/\text{fin} * n_{\text{fin}}} = 2.75 \text{ fF}/\mu m$$

5.3 Parasitic Capacitance

Finally, we use the circuit in Figure 5.6 to find the effective Parasitic Capacitance per micron for delay purposes. The corresponding testbench designed in Cadence is shown in Figure 5.7. The number of fins in the M1 transistor are arbitrarily chosen to be 64.

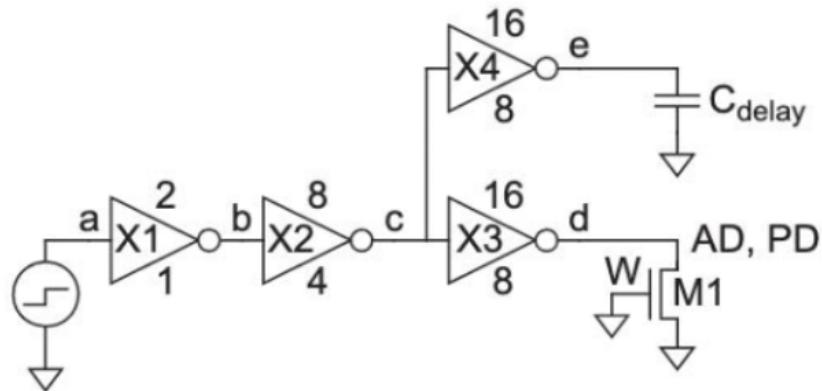


Figure 5.6: Circuit Measuring Effective Parasitic Capacitance

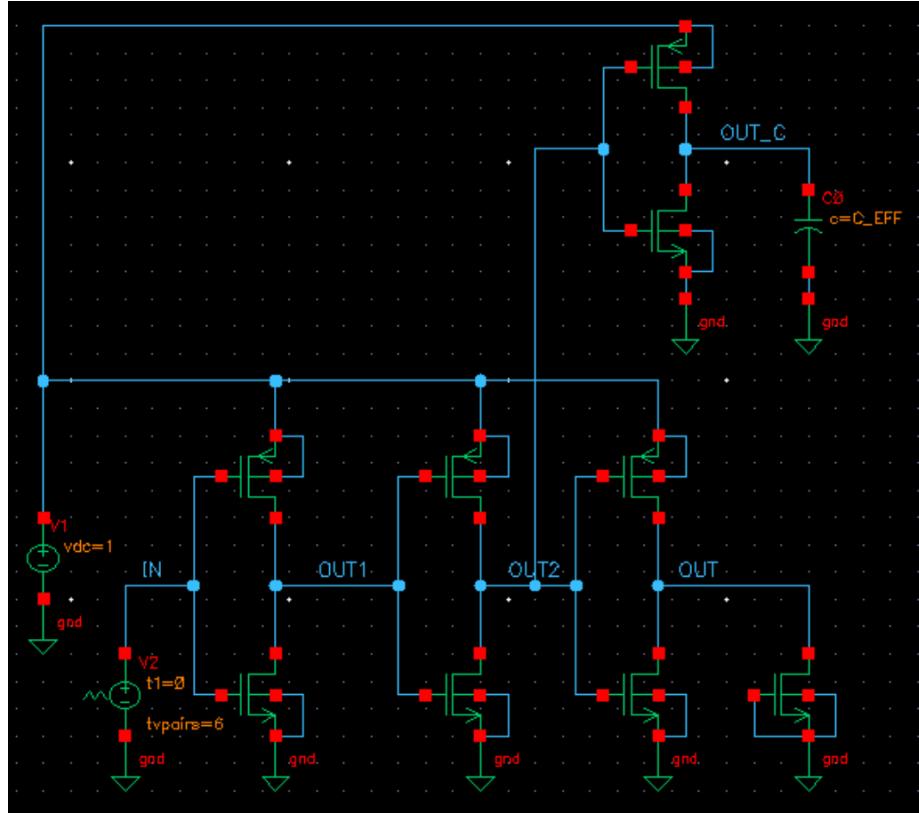


Figure 5.7: Cadence Circuit to Measure Effective Parasitic Capacitance

A transient analysis is done to tune the effective capacitance C_{EFF} until the waveform of OUT_C matches OUT . Probing the input and 4 outputs of the circuit, the following transient simulation waveform in Figure 5.8 is obtained when inputting a VDC of 1V, and 6 pair of points: $[(0s, 0V), (10ps, 0V), (11ps, 1V), (150ps, 1V), (151ps, 0V), (180ps, 0V)]$.

As OUT_C and OUT waveforms match when $C_{EFF} = 1fF$, the effective parasitic capacitance of the NMOS transistor can then be calculated.

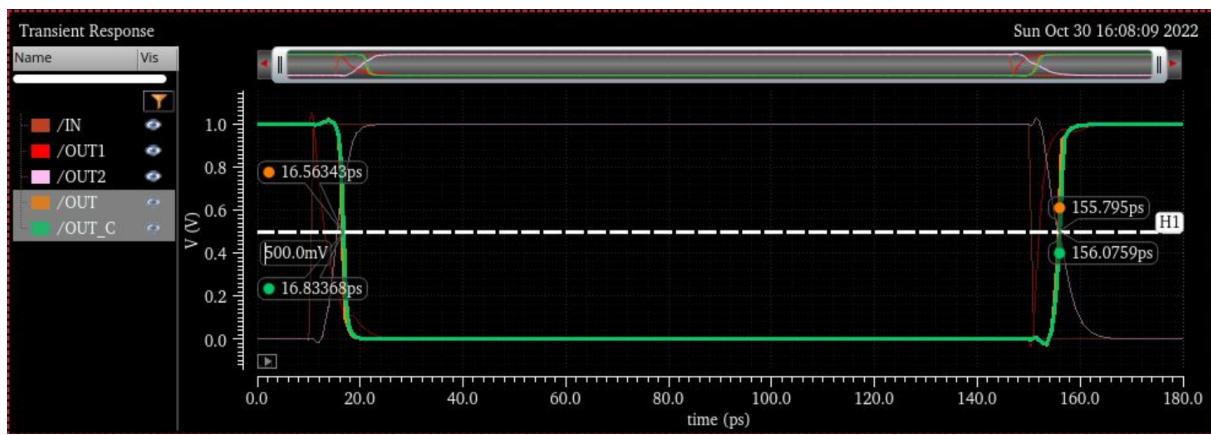


Figure 5.8: Transient Simulation of the Parasitic Capacitance Testbench

Using the above simulation, $C_{\text{EFF}} = 1 \text{ fF}$ and $nfin = 64$:

$$C_{\text{eff}} = 1 \mu\text{m} * \frac{C_{\text{EFF}}}{68\text{nm}/fin*nfin} = 0.229 \text{ fF}/\mu\text{m}$$

6.0 FO4 Inverter Delay Calculation

Given the effective resistances $R_n = 0.266 \text{ k}\Omega \cdot \mu\text{m}$ (nFET) and $R_p = 0.413 \text{ k}\Omega \cdot \mu\text{m}$ (pFET), the Fan Out of 4 Inverter Delay (FO4) t_{pd} can be calculated using the effective Gate Capacitance and effective Parasitic Capacitance obtained in the previous section.

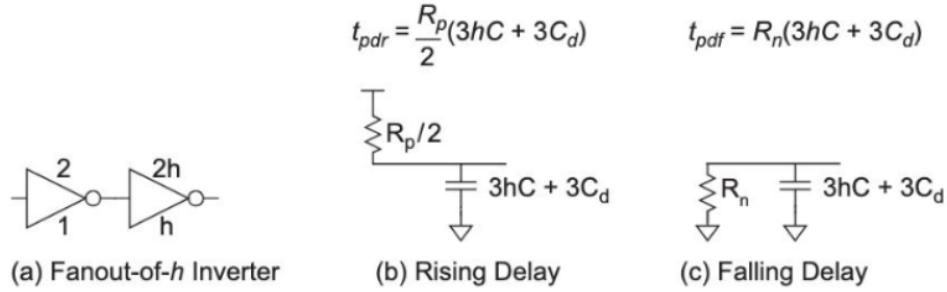


Figure 6.1: Fanout, Rising Delay, and Falling Delay of h Inverter

From Section 5.0, it was found that $C_{\text{eff}} = 0.229 \text{ fF}/\mu\text{m}$ and $C_g = 2.75 \text{ fF}/\mu\text{m}$. For each inverter, the self capacitance is $3*C_{\text{eff}}$, and the load capacitance is $3*C_g$. Therefore, the total capacitance for delay purposes is calculated:

$$C_{\text{delay}} = 3 * 4 * C_g + 3 * C_{\text{eff}} = 33.687 \text{ fF}/\mu\text{m}$$

In rising delay, the PMOS acts as a pull-up transistor, and uses R_p to calculate delays:

$$t_{pLH} = \frac{R_p}{2} C_{\text{delay}} = 6.956 \text{ ps}$$

In falling delay, the NMOS acts as a pull-down transistor, and uses R_n to calculate delays.

$$t_{pHL} = R_n C_{\text{delay}} = 8.96 \text{ ps}$$

Therefore, we can calculate the fan out by taking the average:

$$t_{pd} = \frac{t_{pLH} + t_{pHL}}{2} = 7.95 \text{ ps}$$

7.0 References

CMOS VLSI Design: A Circuits and Systems Perspective by Neil Weste and David Harris,
4th Ed.

Layout and Parasitic Extraction for FreePDK15TM: An Open Source Predictive Process Design
Kit for 15nm FinFET Devices. Link -
<https://repository.lib.ncsu.edu/handle/1840.16/10433>