

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4013B** **flip-flops** Dual D-type flip-flop

Product specification  
File under Integrated Circuits, IC04

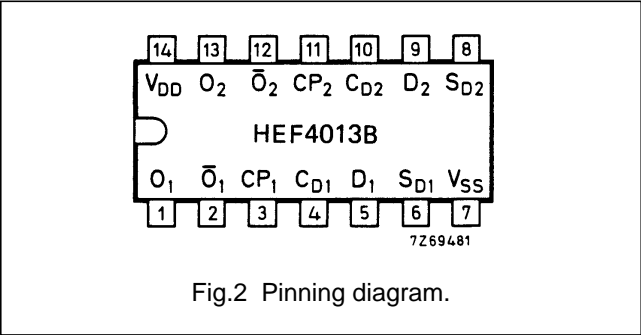
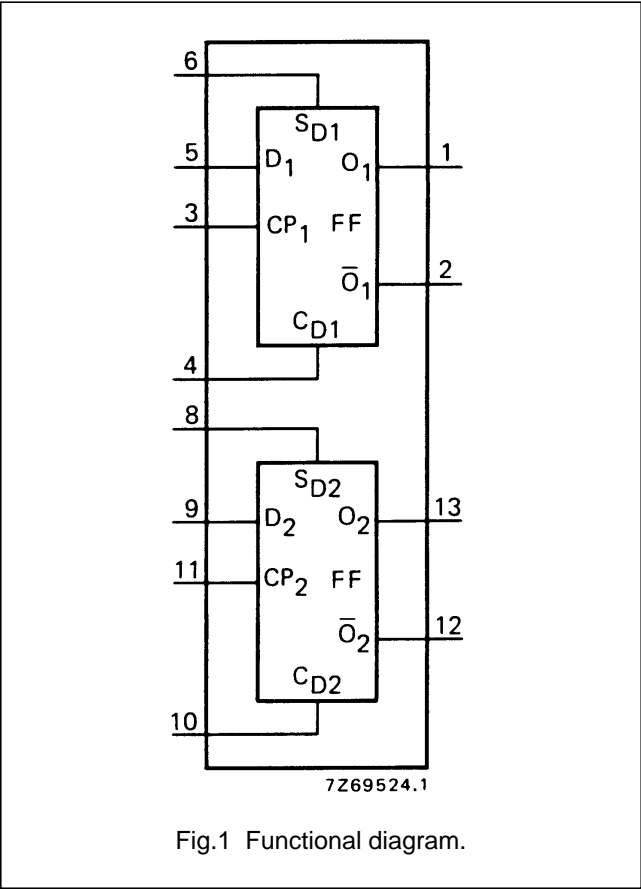
January 1995

Dual D-type flip-flop

HEF4013B  
flip-flops

DESCRIPTION

The HEF4013B is a dual D-type flip-flop which features independent set direct ( $S_D$ ), clear direct ( $C_D$ ), clock inputs (CP) and outputs (O,  $\bar{O}$ ). Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct ( $C_D$ ) and set-direct ( $S_D$ ) are independent and override the D or CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



FUNCTION TABLES

INPUTS				OUTPUTS	
$S_D$	$C_D$	CP	D	O	$\bar{O}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

INPUTS				OUTPUTS	
$S_D$	$C_D$	CP	D	$O_n + 1$	$\bar{O}_n + 1$
L	L		L	L	H
L	L		H	H	L

Notes

- 1. H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
 = positive-going transition  
 $O_n + 1$  = state after clock positive transition

PINNING

- D data inputs
- CP clock input (L to H edge-triggered)
- $S_D$  asynchronous set-direct input (active HIGH)
- $C_D$  asynchronous clear-direct input (active HIGH)
- O true output
- $\bar{O}$  complement output

- HEF4013BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4013BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4013BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

FAMILY DATA,  $I_{DD}$  LIMITS category FLIP-FLOPS

See Family Specifications

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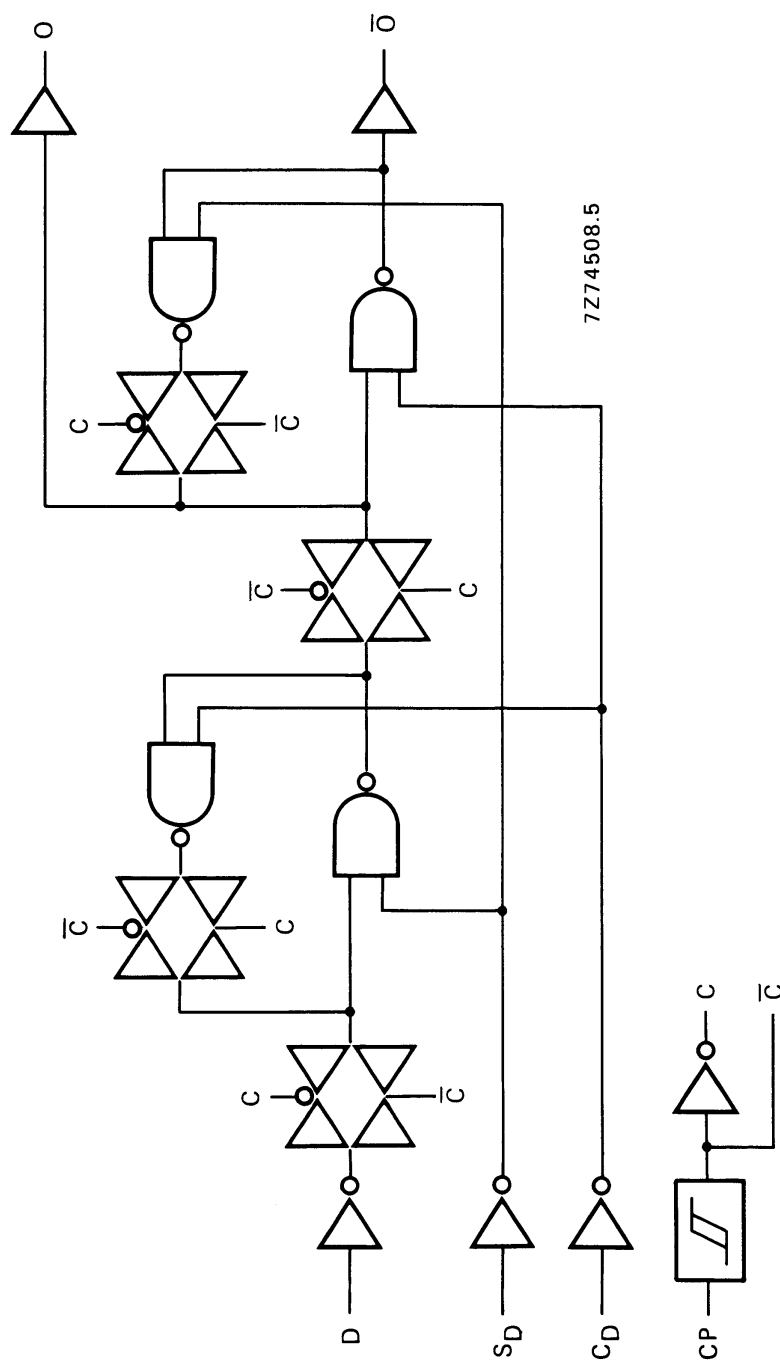


Fig.3 Logic diagram (one flip-flop).

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## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays CP → O, $\overline{O}$ HIGH to LOW	5 10 15	t <sub>PHL</sub>		110 45 30	220 90 60 ns	83 ns + (0,55 ns/pF) C <sub>L</sub> 34 ns + (0,23 ns/pF) C <sub>L</sub> 22 ns + (0,16 ns/pF) C <sub>L</sub>	
LOW to HIGH	5 10 15		t <sub>PLH</sub>		95 40 30	190 80 60 ns	68 ns + (0,55 ns/pF) C <sub>L</sub> 29 ns + (0,23 ns/pF) C <sub>L</sub> 22 ns + (0,16 ns/pF) C <sub>L</sub>
S <sub>D</sub> → $\overline{O}$ HIGH to LOW	5 10 15			t <sub>PHL</sub>		100 40 30	200 80 60 ns
S <sub>D</sub> → O LOW to HIGH	5 10 15	t <sub>PLH</sub>				75 35 25	150 70 50 ns
C <sub>D</sub> → O HIGH to LOW	5 10 15		t <sub>PHL</sub>			100 40 30	200 80 60 ns
C <sub>D</sub> → $\overline{O}$ LOW to HIGH	5 10 15			t <sub>PLH</sub>		60 30 20	120 60 40 ns
Output transition times HIGH to LOW	5 10 15	t <sub>THL</sub>			60 30 20	120 60 40 ns	10 ns + (1,0 ns/pF) C <sub>L</sub> 9 ns + (0,42 ns/pF) C <sub>L</sub> 6 ns + (0,28 ns/pF) C <sub>L</sub>
LOW to HIGH	5 10 15		t <sub>TLH</sub>		60 30 20	120 60 40 ns	10 ns + (1,0 ns/pF) C <sub>L</sub> 9 ns + (0,42 ns/pF) C <sub>L</sub> 6 ns + (0,28 ns/pF) C <sub>L</sub>

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	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	
Set-up time D $\rightarrow$ CP	5 10 15	$t_{su}$	40 25 15	20 10 5	ns ns ns	see also waveforms Figs 4 and 5
Hold time D $\rightarrow$ CP	5 10 15	$t_{hold}$	20 20 15	0 0 0	ns ns ns	
Minimum clock pulse width; LOW	5 10 15	$t_{WCPL}$	60 30 20	30 15 10	ns ns ns	
Minimum $S_D$ pulse width; HIGH	5 10 15	$t_{WSDH}$	50 24 20	25 12 10	ns ns ns	
Minimum $C_D$ pulse width; HIGH	5 10 15	$t_{WCDH}$	50 24 20	25 12 10	ns ns ns	
Recovery time for $S_D$	5 10 15	$t_{RSD}$	15 15 15	-5 0 0	ns ns ns	
Recovery time for $C_D$	5 10 15	$t_{RCD}$	40 25 25	25 10 10	ns ns ns	
Maximum clock pulse frequency	5 10 15	$f_{max}$	7 14 20	14 28 40	MHz MHz MHz	

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5 10 15	$850 f_i + \sum (f_o C_L) \times V_{DD}^2$ $3\,600 f_i + \sum (f_o C_L) \times V_{DD}^2$ $9\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = total load cap. (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

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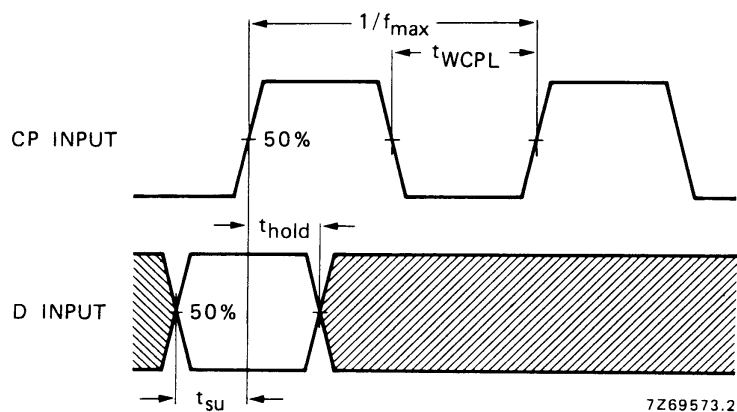
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Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

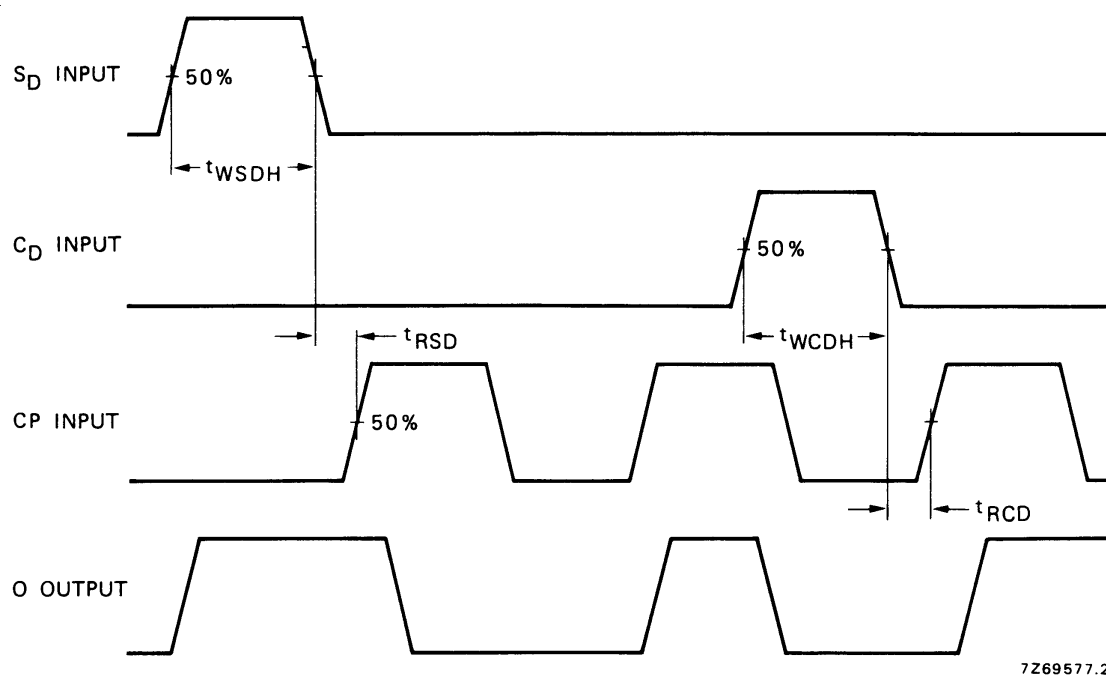


Fig.5 Waveforms showing recovery times for  $S_D$  and  $C_D$ ; minimum  $S_D$  and  $C_D$  pulse widths.

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## APPLICATION INFORMATION

Some examples of applications for the HEF4013B are:

- Counters/dividers
- Registers
- Toggle flip-flops

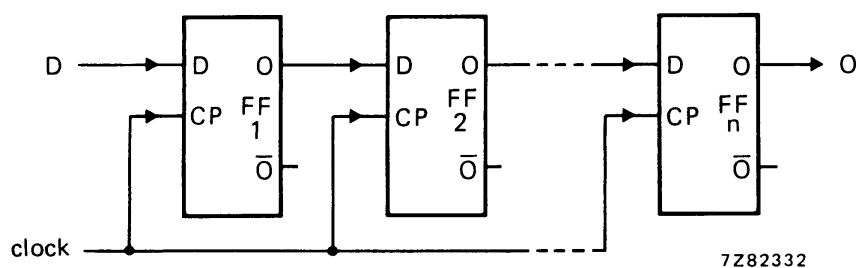


Fig.6 Typical application of the HEF4013B in an n-stage shift register.

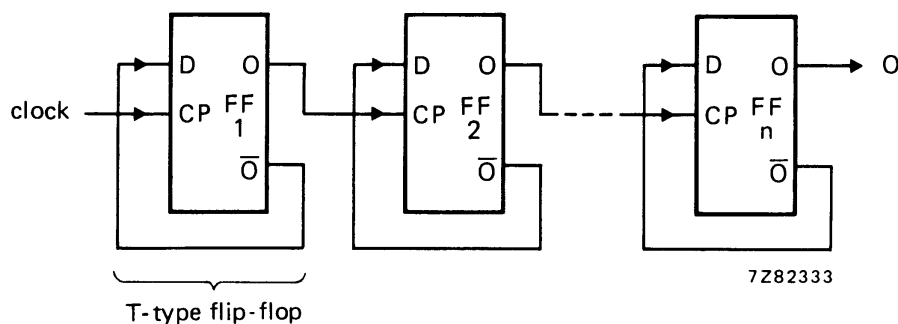


Fig.7 Typical application of the HEF4013B in a binary ripple up-counter; divide-by- $2^n$ .

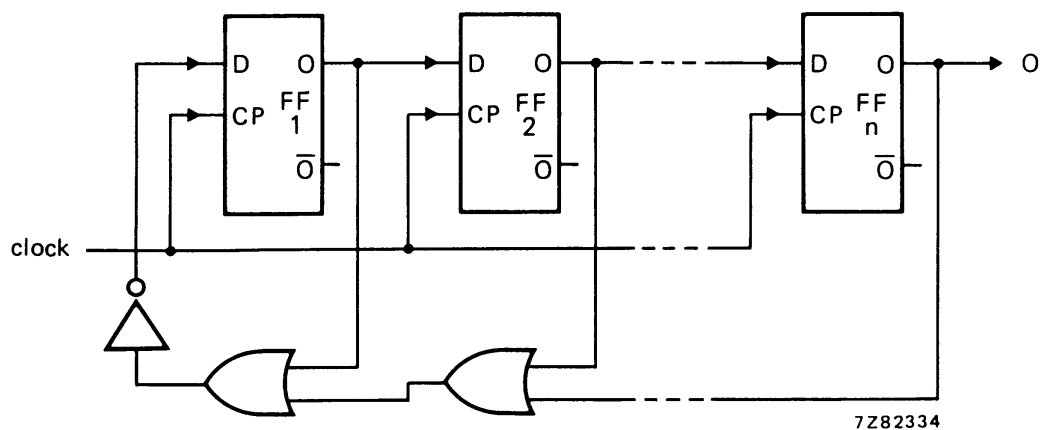


Fig.8 Typical application of the HEF4013B in a modified ring counter; divide-by-( $n + 1$ ).