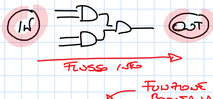
L#18 24/11/18

CIRCUITI LOGICI

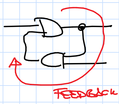
COMBINATORI



FUNZIONE BOOLEANA

$OUT = f(IN)$

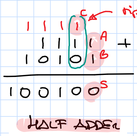
SEQUENZIALI



$OUT = f(IN, STATO)$

ESEMPI DI CIRCUITI LOGICA COMBINATORI

① Costruttivo — Sommatore Binario



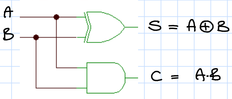
in		out	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

XOR — AND

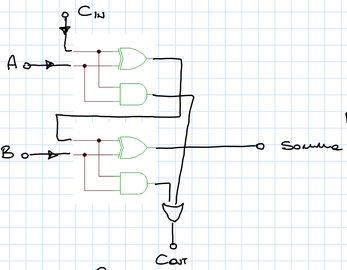
$S = A \oplus B$

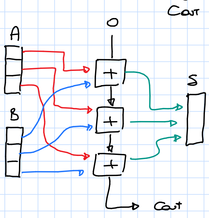
$C = A \cdot B$

HALF ADDER



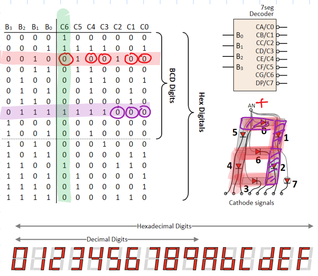
FULL ADDER





---

② "Non-costruttivo" partendo da tabella di verità. "DECODER"



2 = 0010

7 = 0111

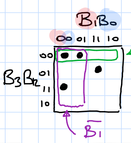
CIRCUITO PER CG

$$C_6 = \bar{B}_3 \cdot \bar{B}_2 \cdot \bar{B}_1 \cdot \bar{B}_0 + \bar{B}_3 \cdot \bar{B}_2 \cdot \bar{B}_1 \cdot B_0 + \bar{B}_3 \cdot B_2 \cdot B_1 + B_0 + B_3 \cdot B_2 \cdot \bar{B}_1 \cdot \bar{B}_0$$

$$C_6 = \bar{B}_3 \cdot \bar{B}_2 \cdot \bar{B}_1 \cdot (\bar{B}_0 + B_0)$$ — $B_0 + \bar{B}_0$ sempre vero

Ⓐ SEMPLIFICAZIONE PER ISPEZIONE

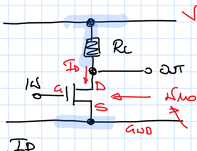
Ⓑ MAPPA KARNAUGH

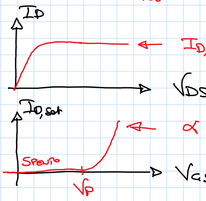


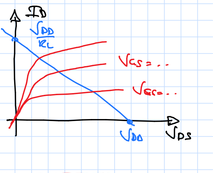
Ⓒ ALGORITMI OTTIMIZZAZIONE

ESERCITAZIONI

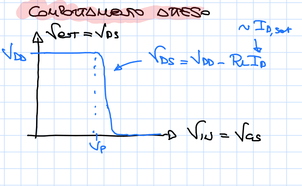
① PORTA NOT CON UN NMOS

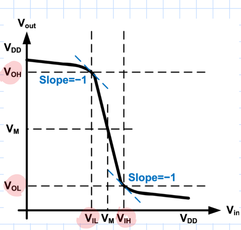


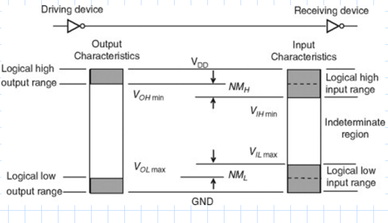




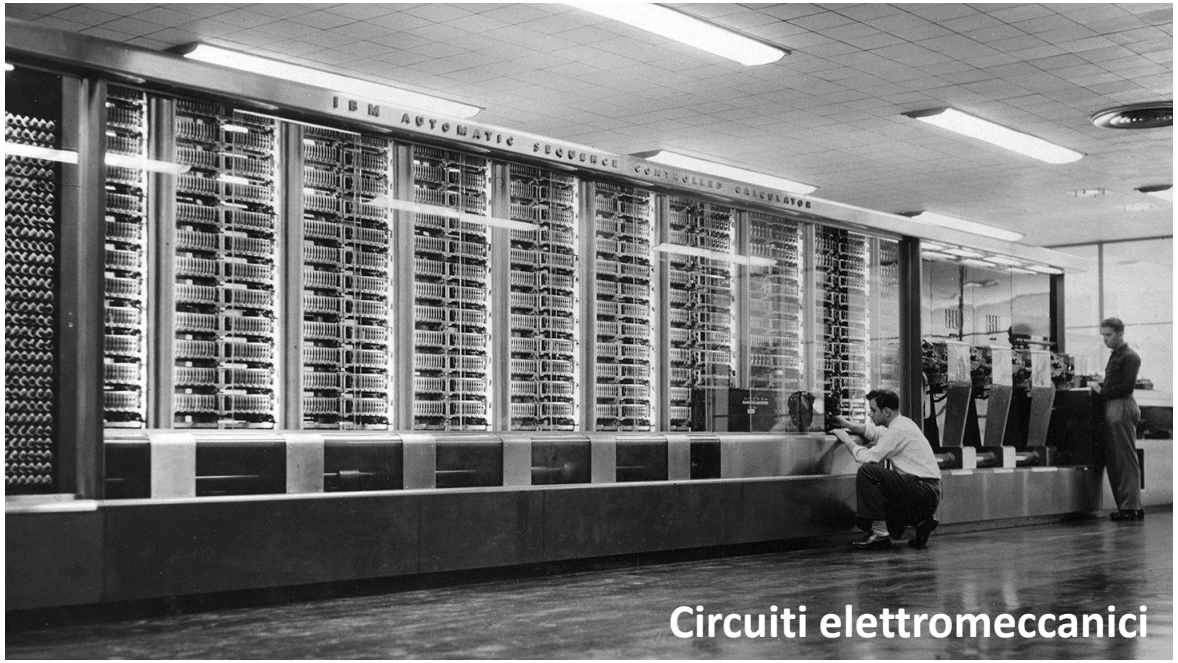
COMPORTAMENTO STATICO





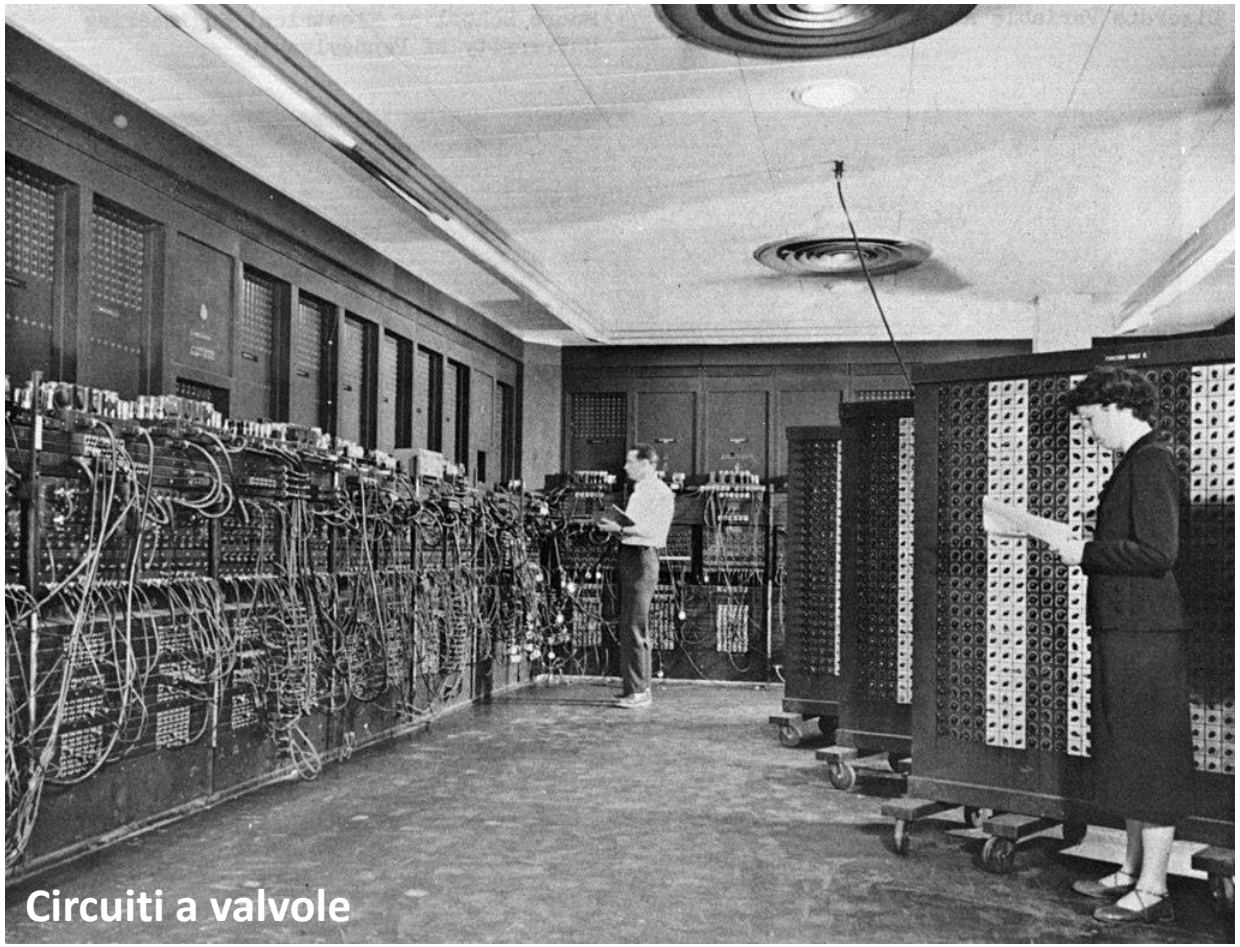


Elettronica digitale: come?



1945 Harvard Mark I

1945 ENIAC



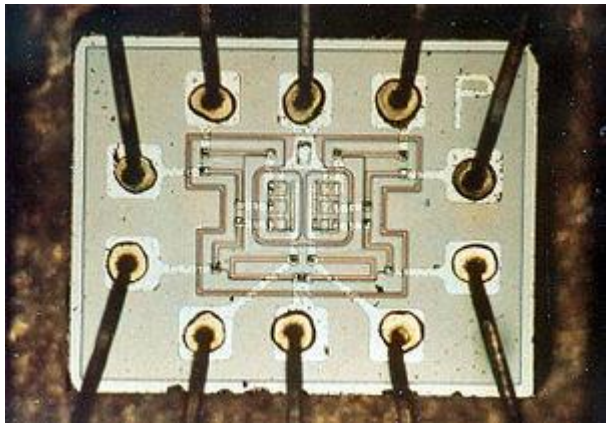
La preistoria...

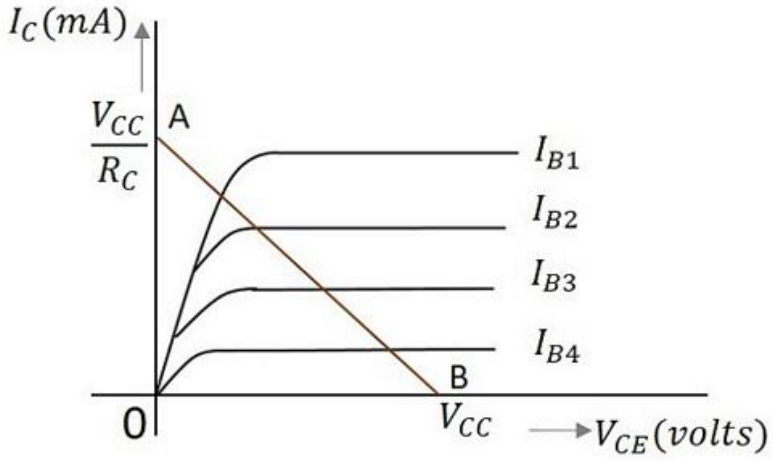
Implementazione: le famiglie logiche

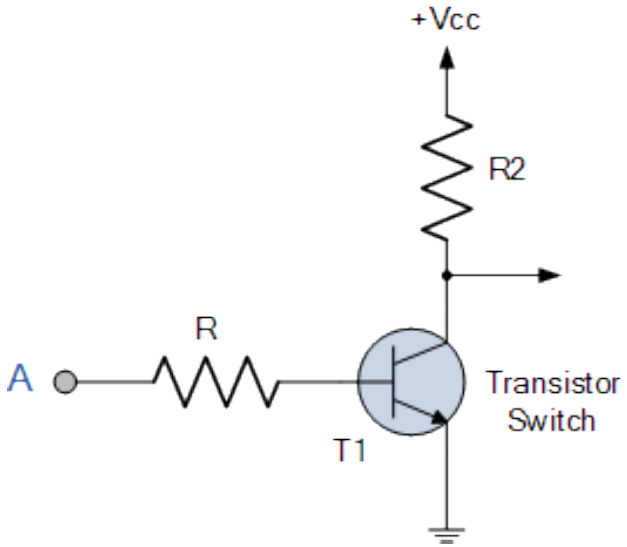
BIPOLARI

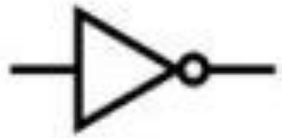
- **RTL = Resistor Transistor Logic**
- DTL = Diode Transistor Logic
- TTL = Transistor Transistor Logic

Computer Apollo







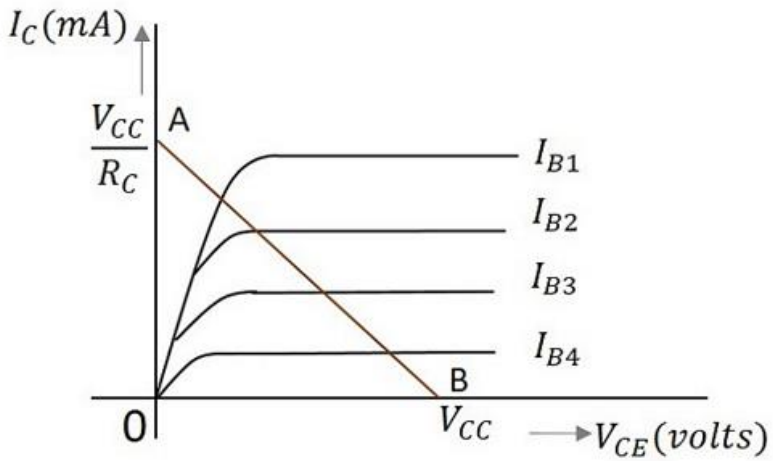


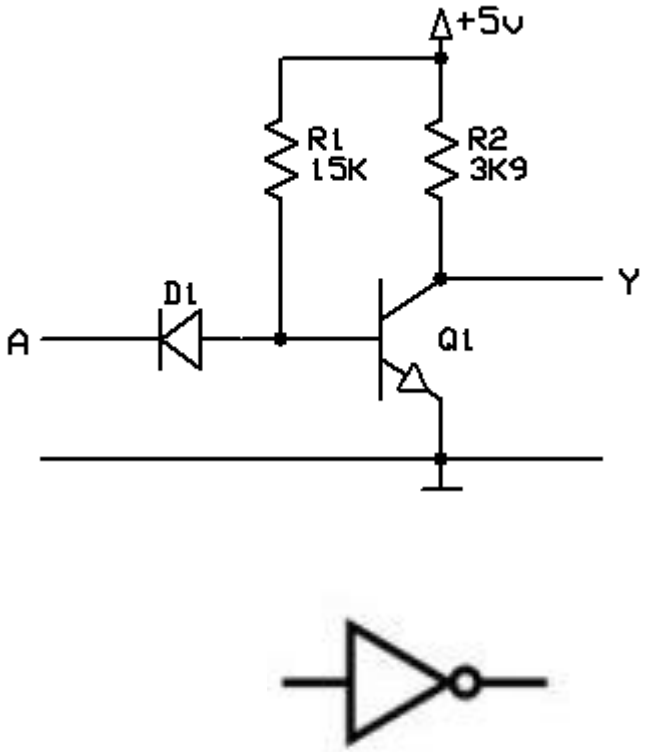
(*) lista sempificata/parziale... nella storia sono esistite un numero abbastanza spropositato di implementazioni

Implementazione: le famiglie logiche

BIPOLARI

- RTL = Resistor Transistor Logic
- **DTL = Diode Transistor Logic**
- TTL = Transistor Transistor Logic



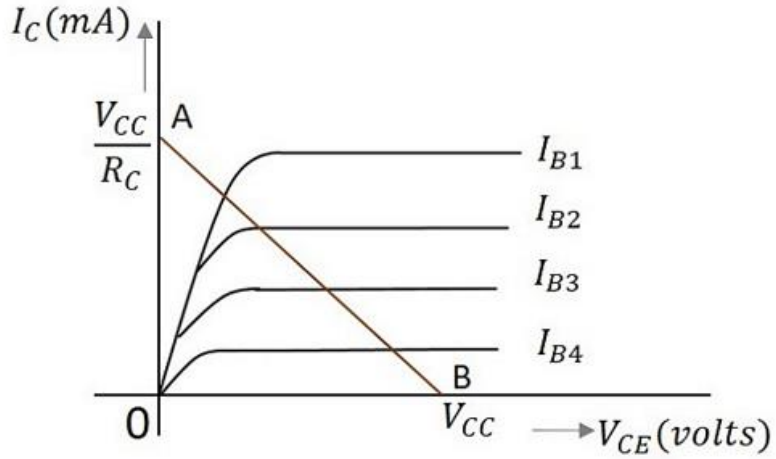


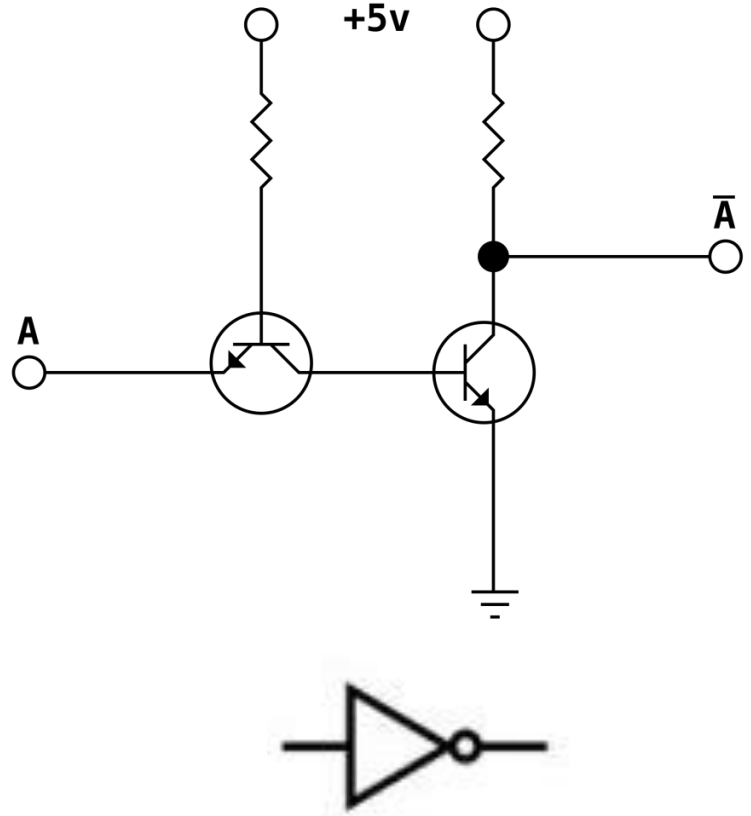
(*) lista sempificata/parziale... nella storia sono esistite un numero abbastanza spropositato di implementazioni

Implementazione: le famiglie logiche

BIPOLARI

- RTL = Resistor Transistor Logic
- DTL = Diode Transistor Logic
- **TTL = Transistor Transistor Logic**



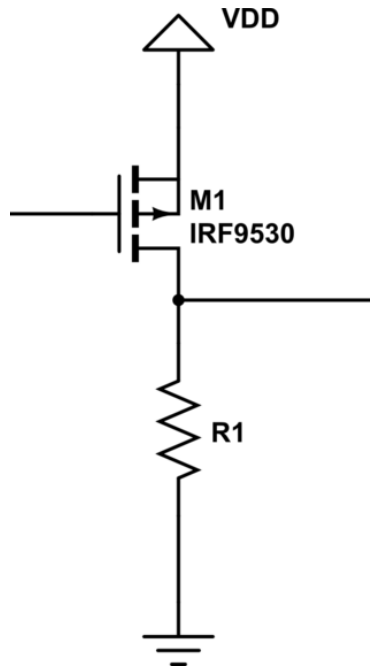


(*) lista sempificata/parziale... nella storia sono esistite un numero abbastanza spropositato di implementazioni

Implementazione: le famiglie logiche

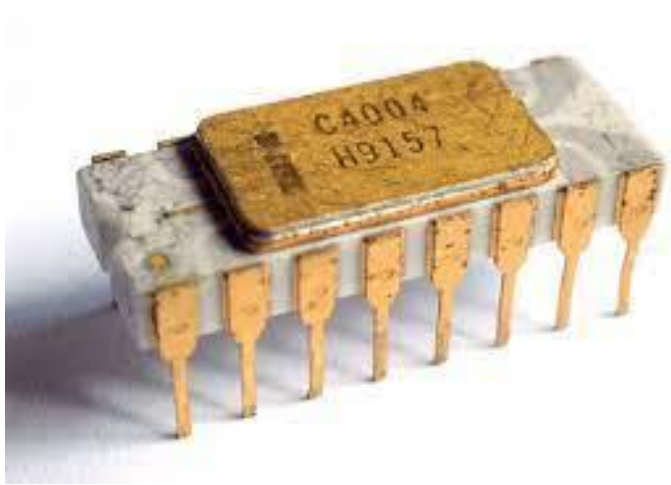
BIPOLARI

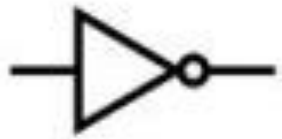
- RTL = Resistor Transistor Logic
- DTL = Diode Transistor Logic
- TTL = Transistor Transistor Logic



UNIPOLARI

- **PMOS**
- NMOS
- CMOS



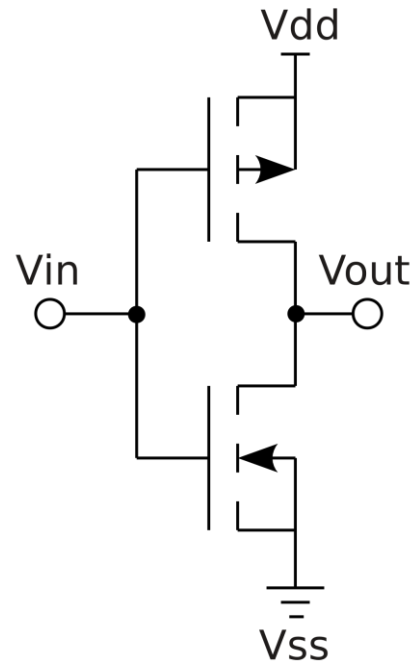


(*) lista sempificata/parziale... nella storia sono esistite un numero abbastanza spropositato di implementazioni

Implementazione: le famiglie logiche

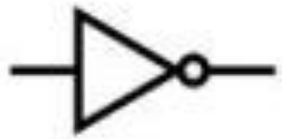
BIPOLARI

- RTL = Resistor Transistor Logic
- DTL = Diode Transistor Logic
- TTL = Transistor Transistor Logic



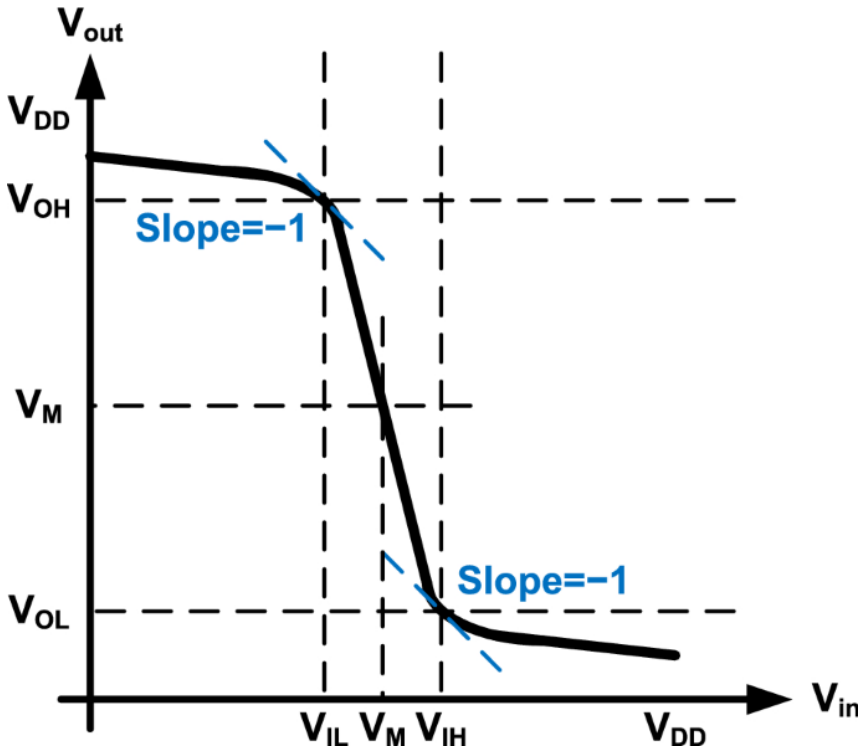
UNIPOLARI

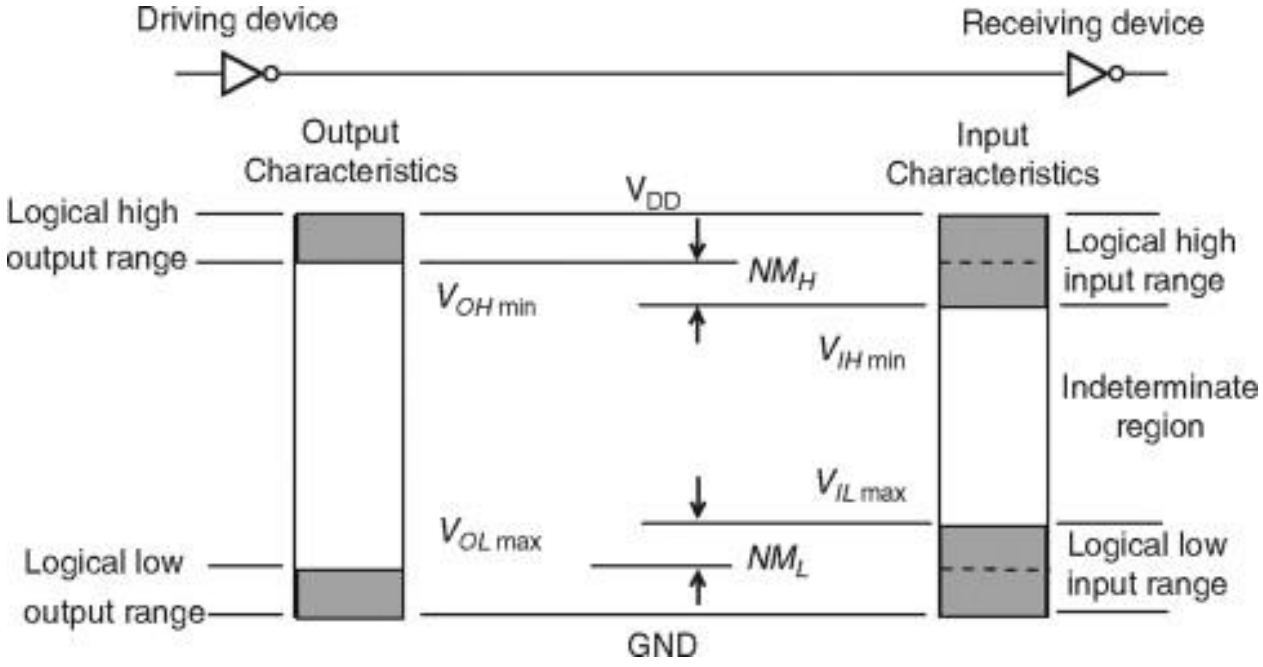
- PMOS
- NMOS
- **CMOS**



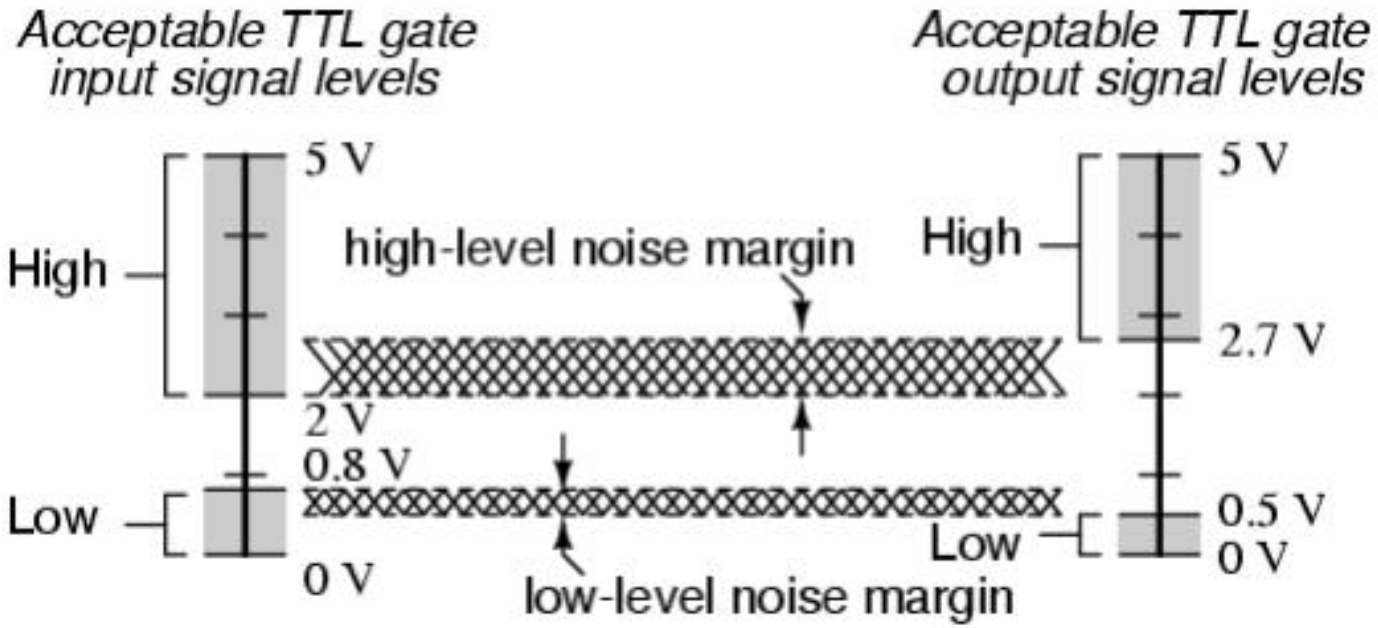
(*) lista sempificata/parziale... nella storia sono esistite un numero abbastanza spropositato di implementazioni

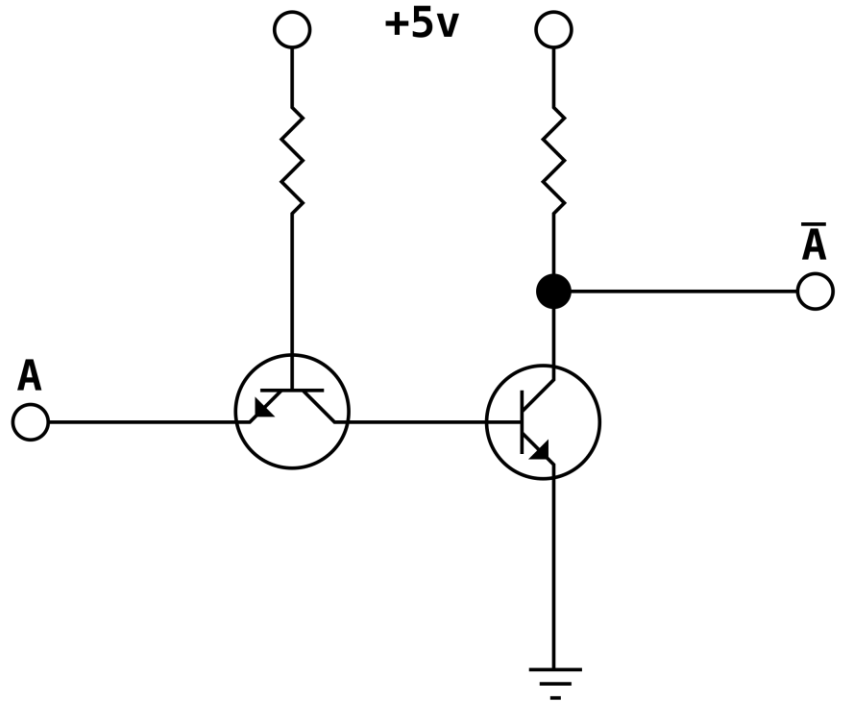
I livelli logici reali: la resilienza al rumore



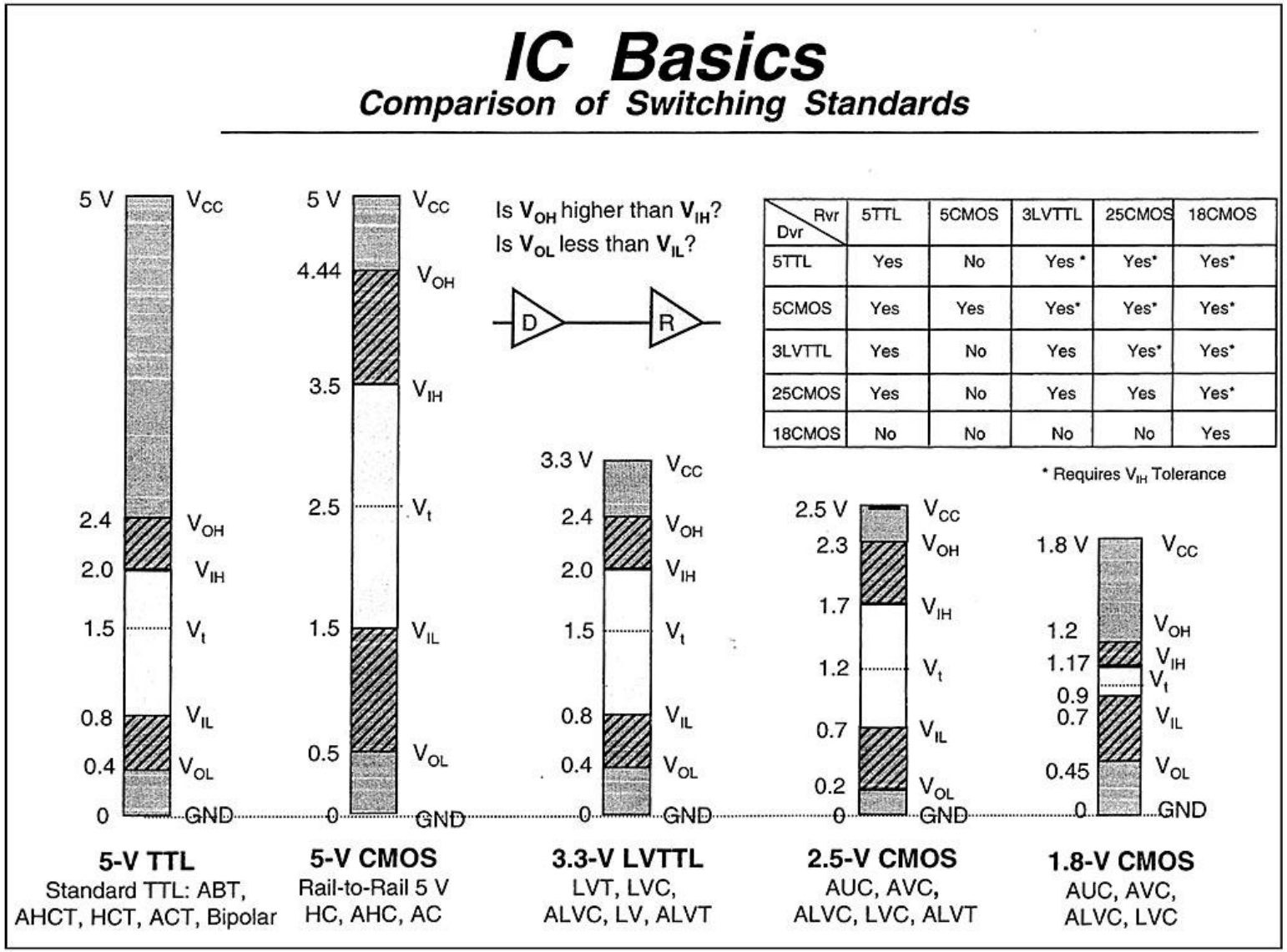


I livelli logici reali: esempio TTL

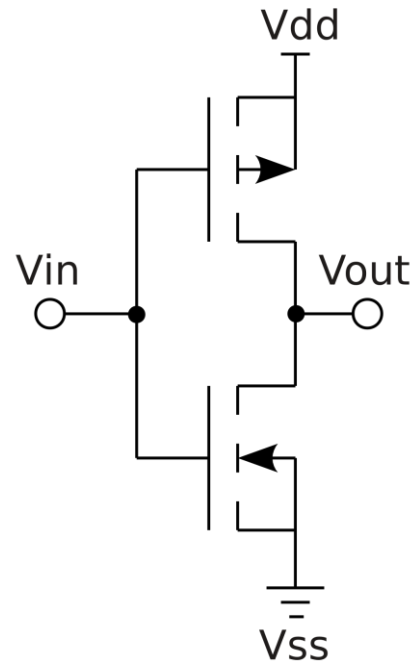




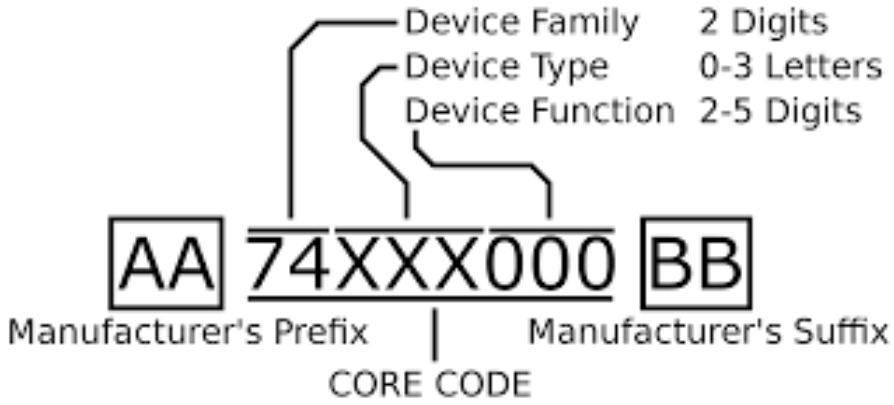
I livelli logici reali: CMOS e compatibilità?

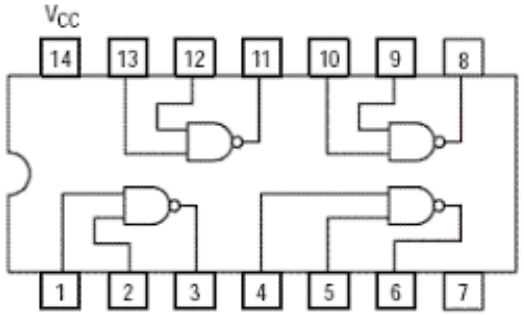


Dvr \ Rvr	5TTL	5CMOS	3LVTTL	25CMOS	18CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5CMOS	Yes	Yes	Yes*	Yes*	Yes*
3LVTTL	Yes	No	Yes	Yes*	Yes*
25CMOS	Yes	No	Yes	Yes	Yes*
18CMOS	No	No	No	No	Yes

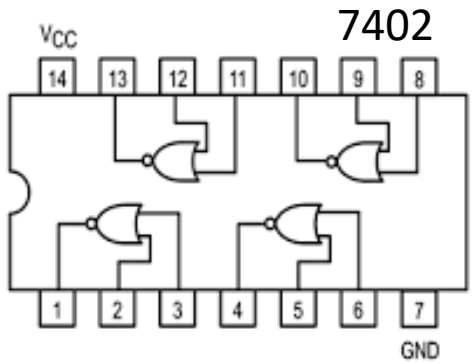


Serie 7400



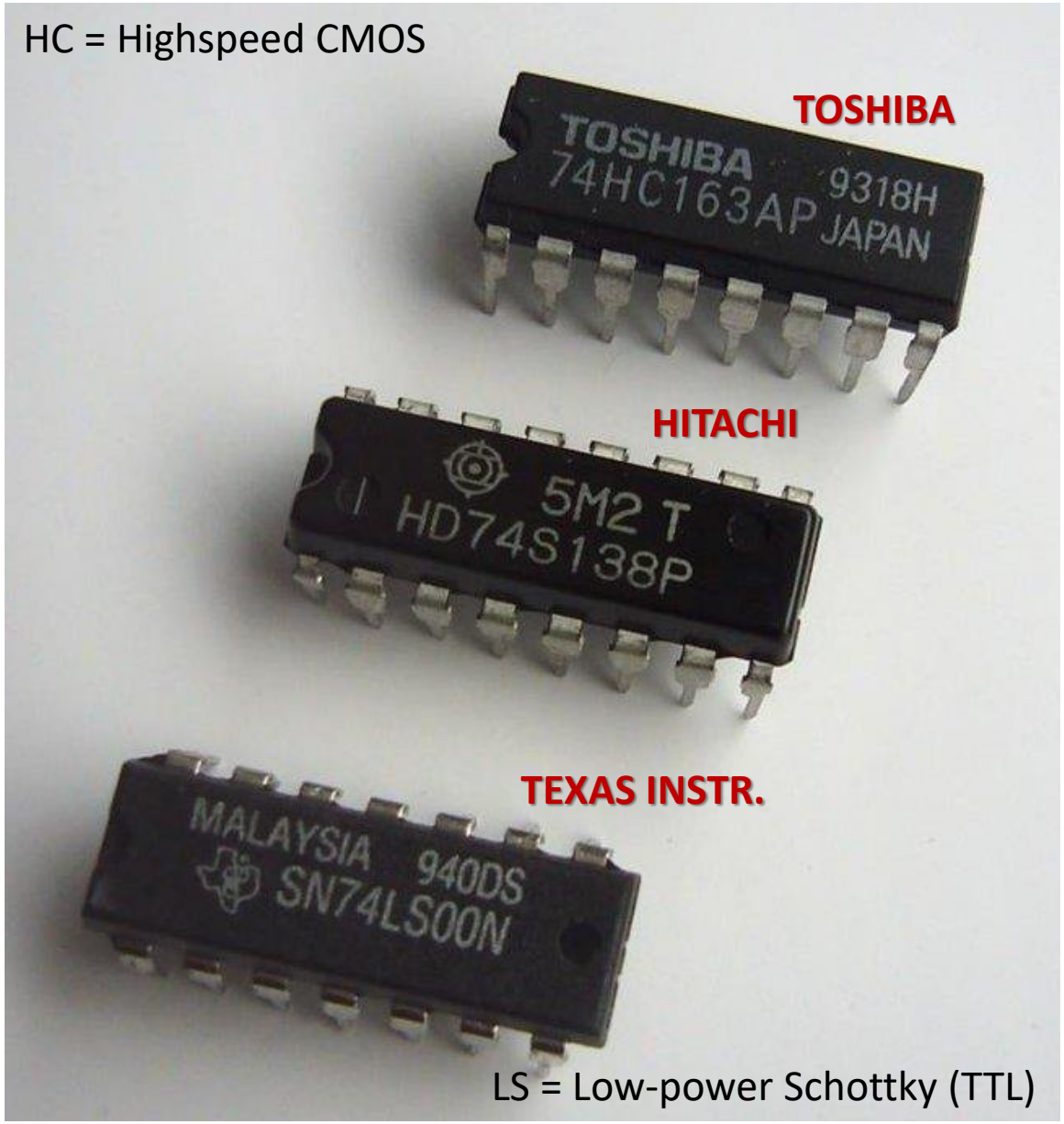


7400



7402

HC = Highspeed CMOS



LS = Low-power Schottky (TTL)

https://en.wikipedia.org/wiki/List_of_7400-series_integrated_circuits

Serie 7400: quanti sono...?

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Product Preview

Nine-Wide Buffers with Open-Drain Outputs

High-Performance Silicon-Gate CMOS

The MC54/74HC9134 consists of nine inverting buffers and the MC54/74HC9135 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

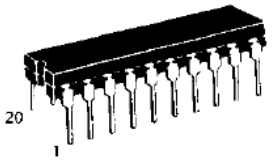
These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

Each of the HC9134 and HC9135 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

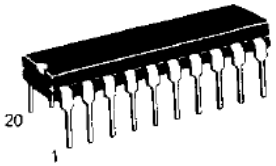
Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices

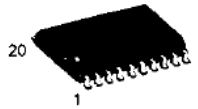
MC54/74HC9134
MC54/74HC9135



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

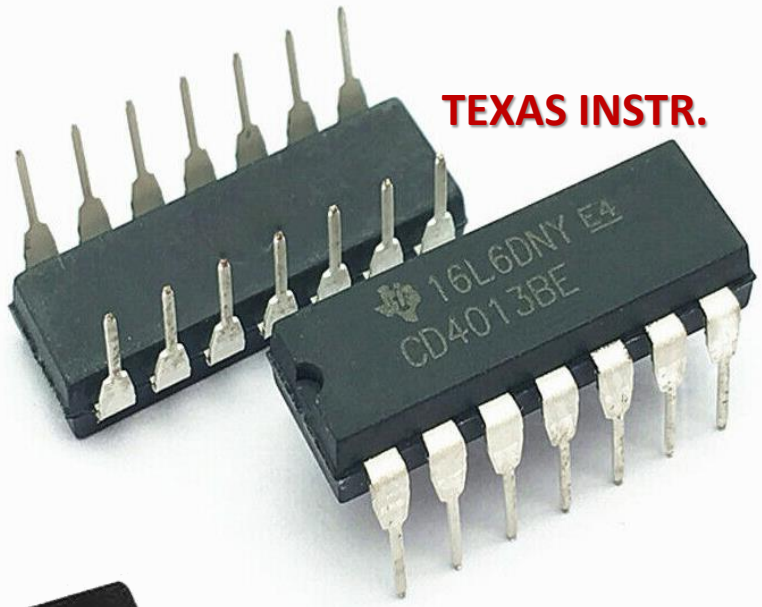
MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

Answer: migliaia

Serie 4000

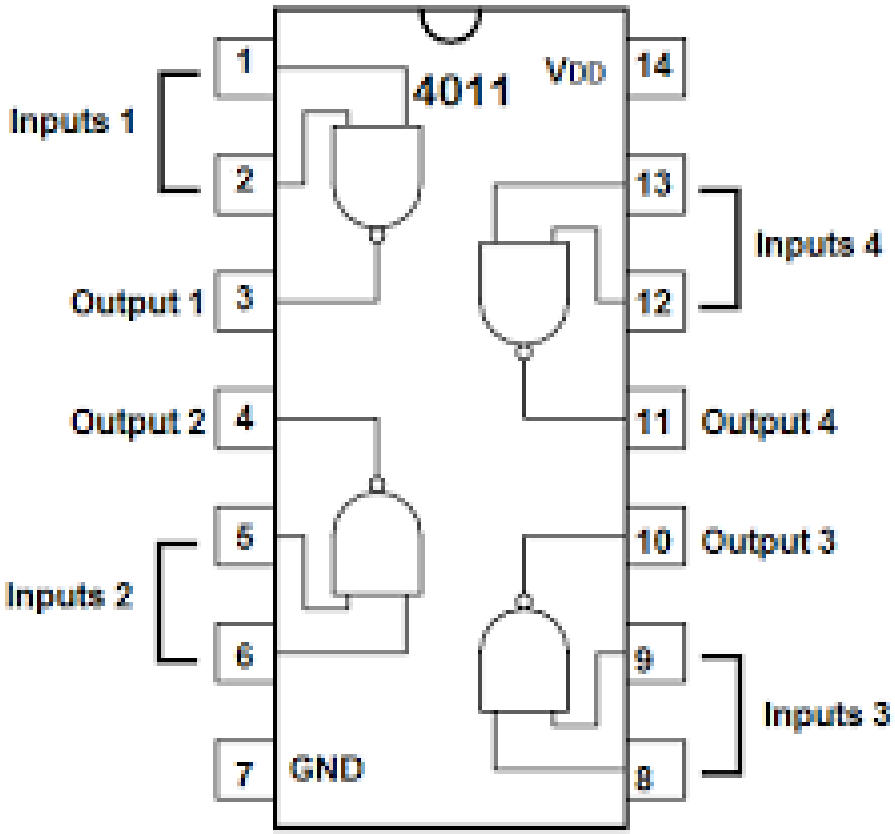
CD4001	NOR
CD4011	**NAND**
CD4013	**D-flipflop**
CD4027	**JK-flipflop**
CD4042	D-latch (diverso da CD4013!!)
...	

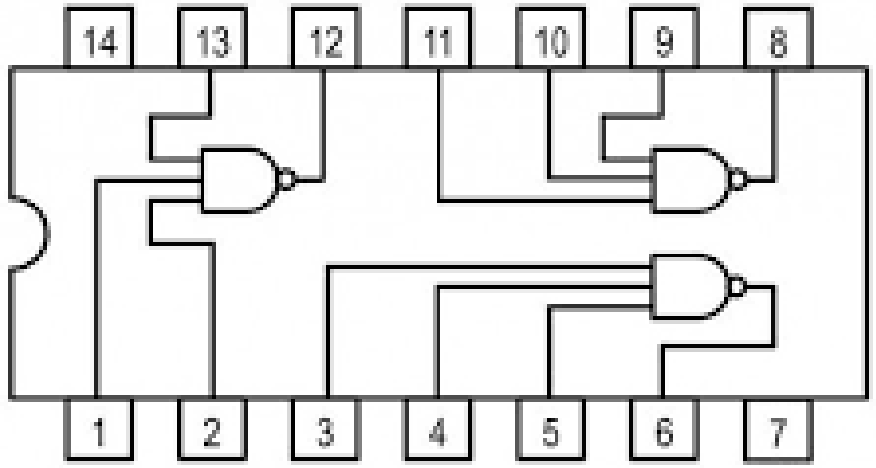


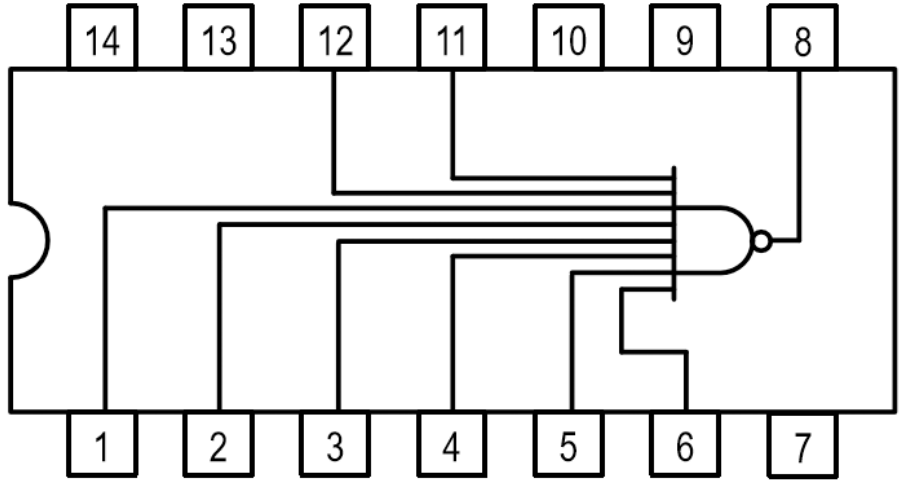
TEXAS INSTR.

NXP (da PHILIPS SEMICOND)

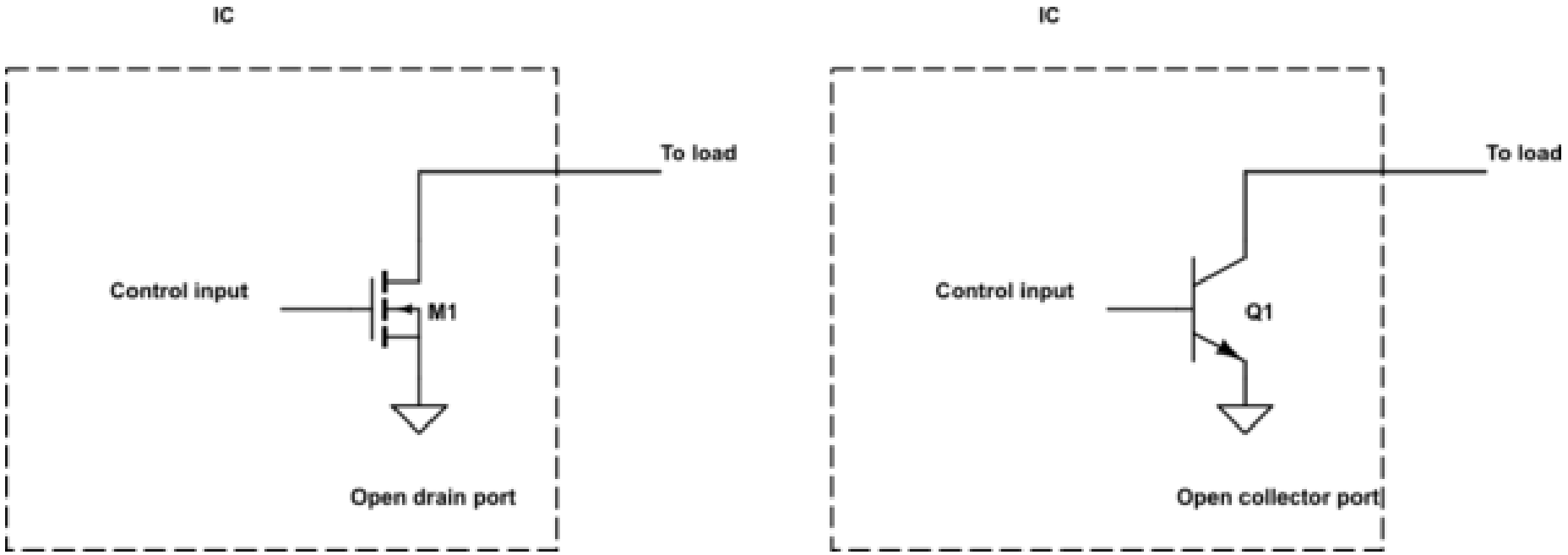
Altri dettagli: versioni multi-input



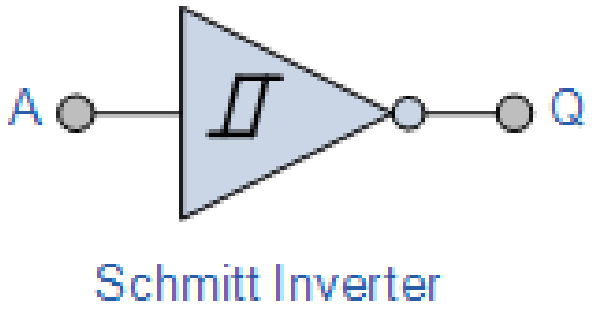




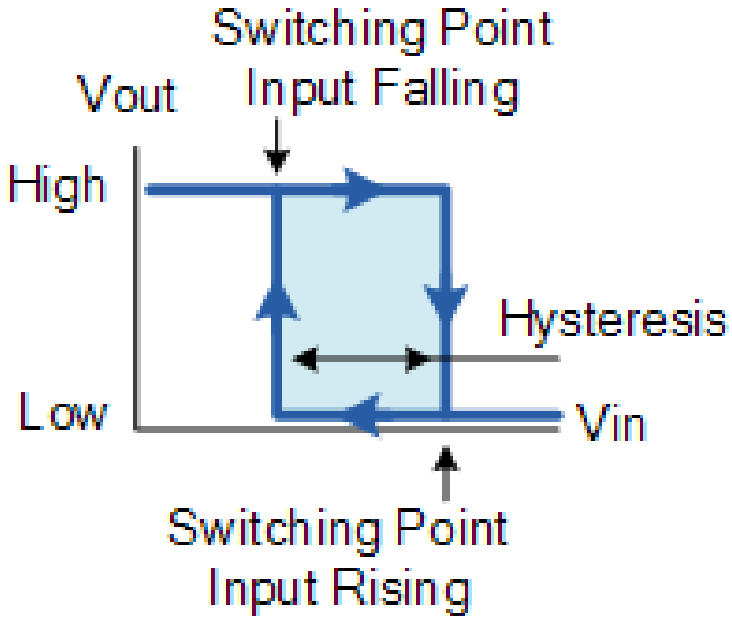
Altri dettagli: open collector/drain

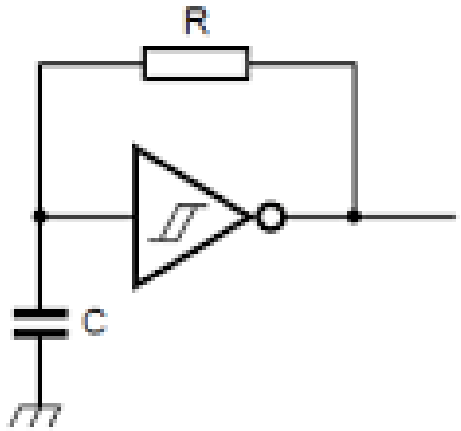


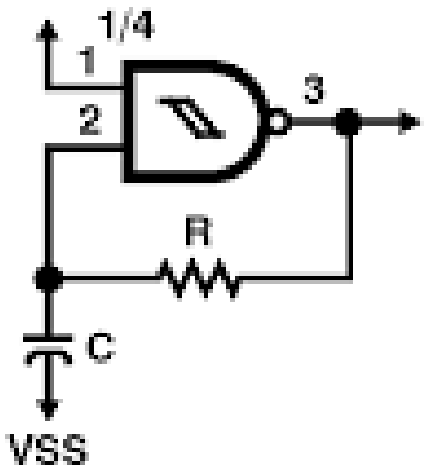
Altri dettagli: ingressi Schmitt



Schmitt Inverter

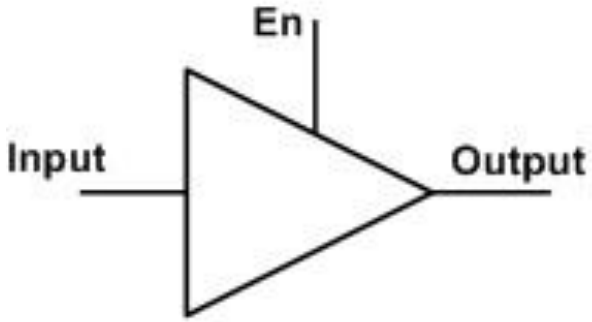






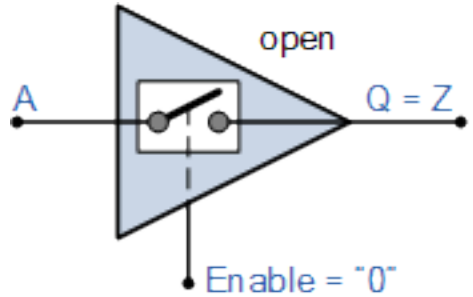
Altri dettagli: buffer «tri-state»

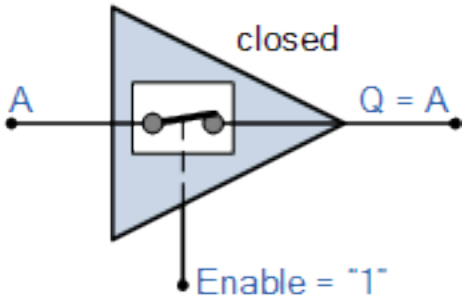
Symbol



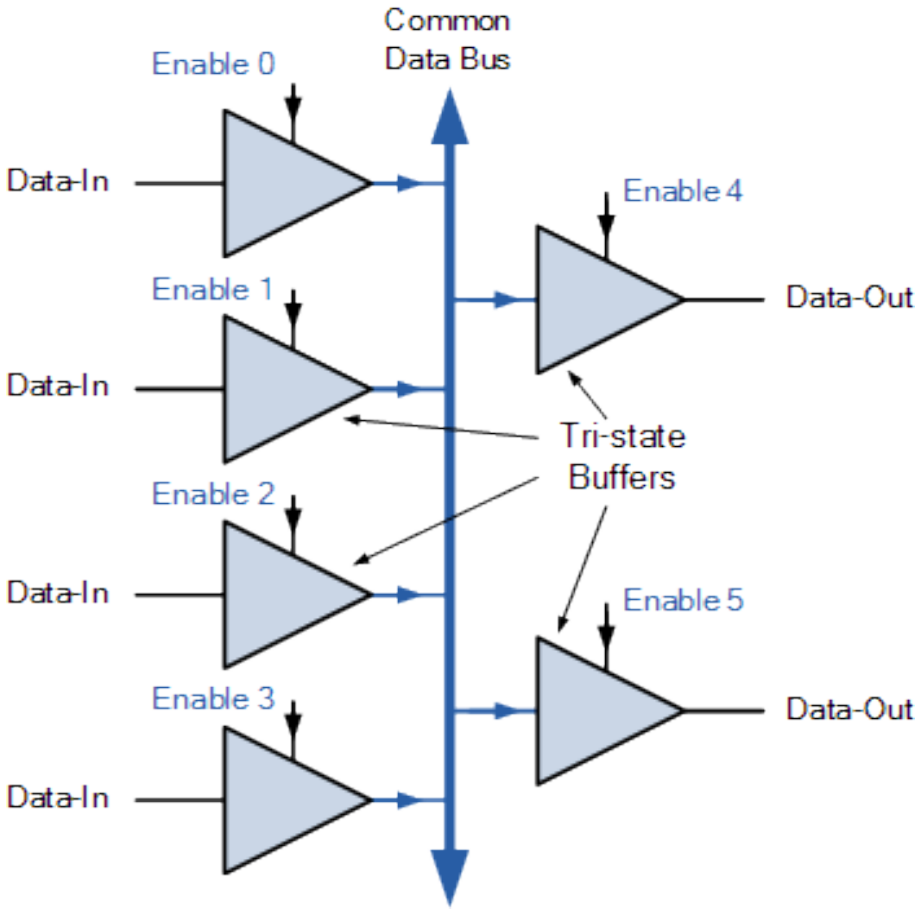
Truth Table

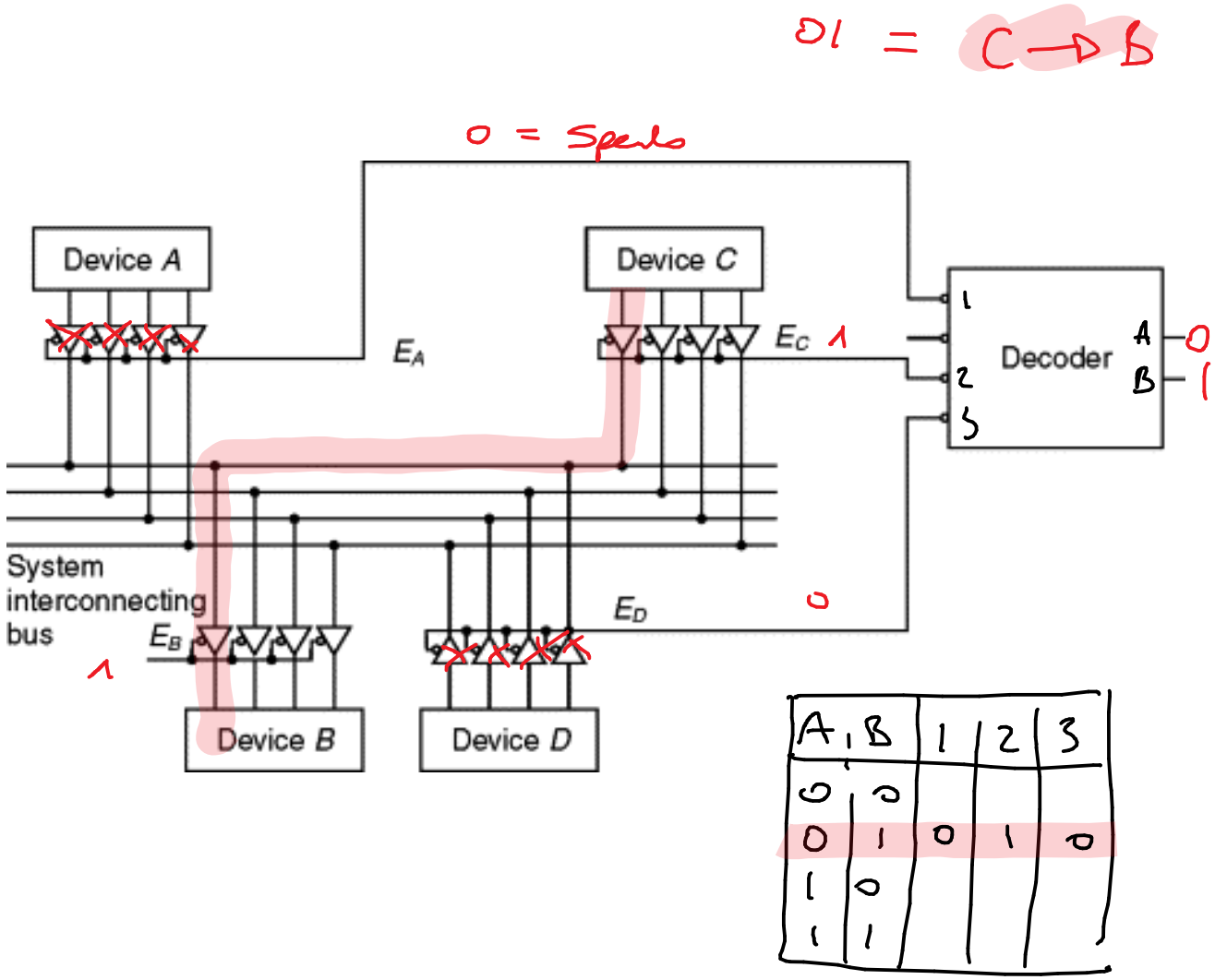
En	Input	Output
0	X	Hi-Z
1	0	0
1	1	1





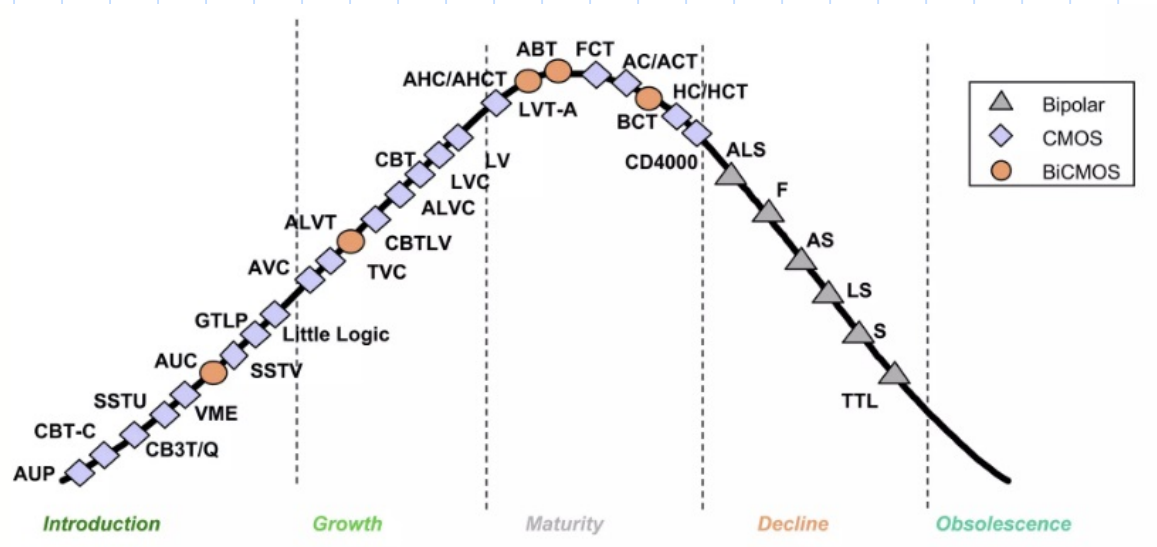
Altri dettagli: buffer «tri-state» e il bus



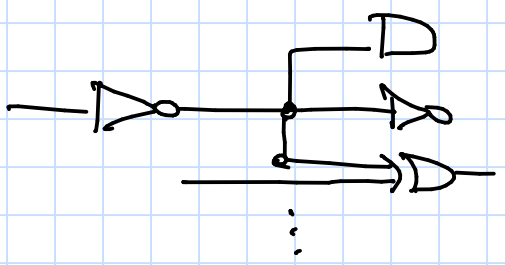


A, B	1	2	3
0 0			
0 1	0	1	0
1 0			
1 1			

ROUTE REACH: ALCUNI ASPETTI DA RICORDARE

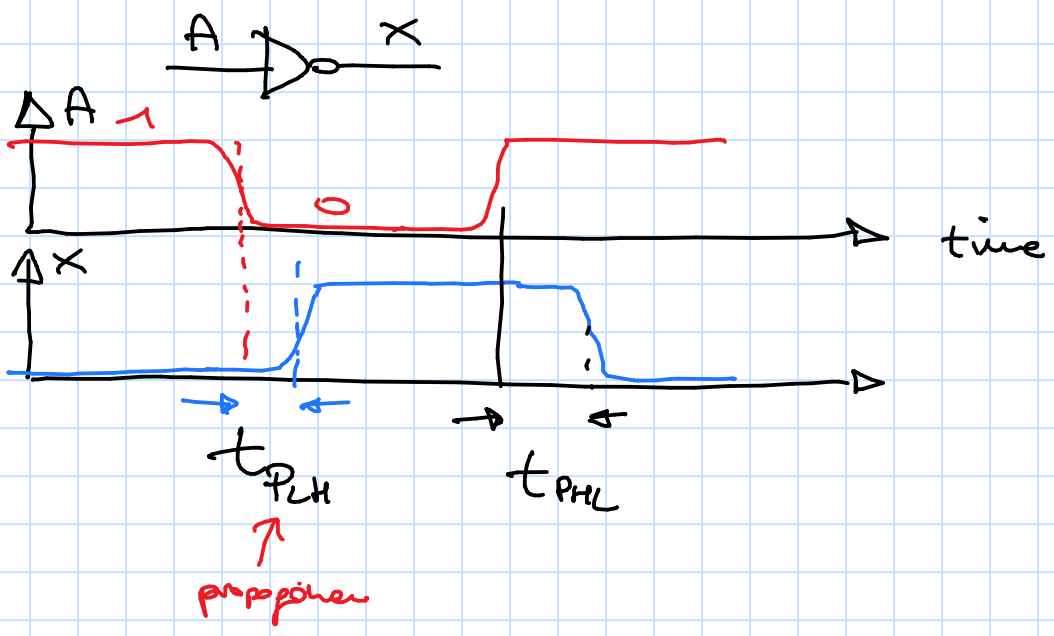


→ FAN OUT : quante porte può pilotare un output

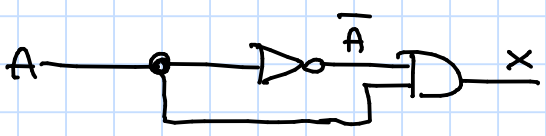


→ FAN IN

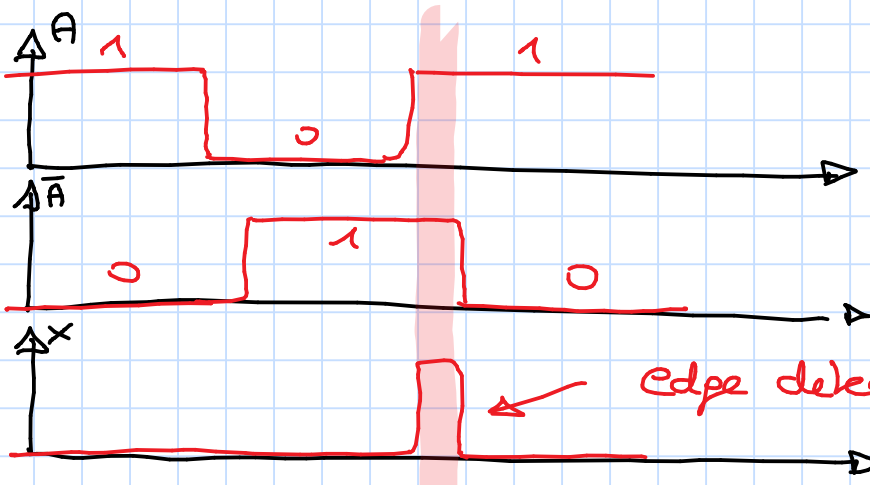
→ TEMPO DI PROPAGAZIONE DEL SEGNALE



ESEMPIO DI CONSEGUENZA DEL DELAY



$A \cdot \bar{A} = falso$?

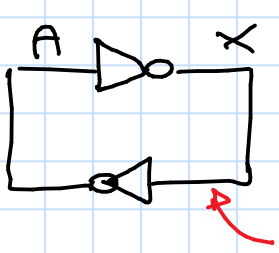


"RACING"

POTENZIALMENTE PROBLEMATICO!

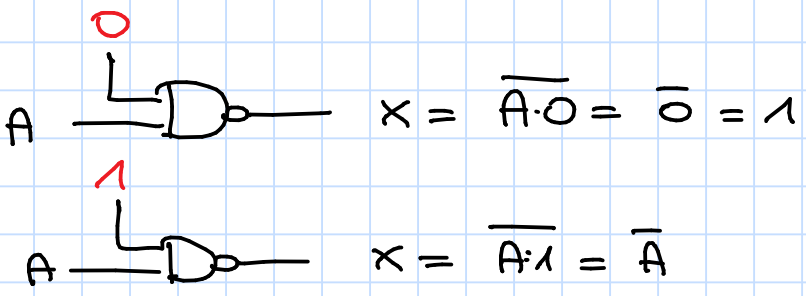
più dettagli più lordi...

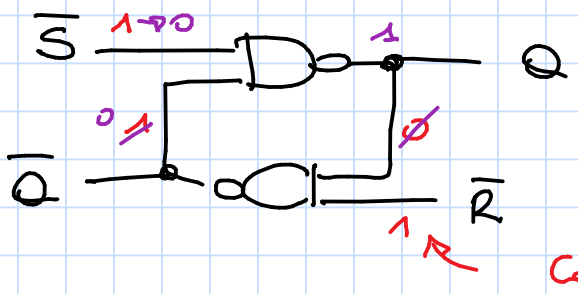
FEEDBACK



$\begin{cases} X = \bar{A} \\ A = \bar{X} \end{cases}$

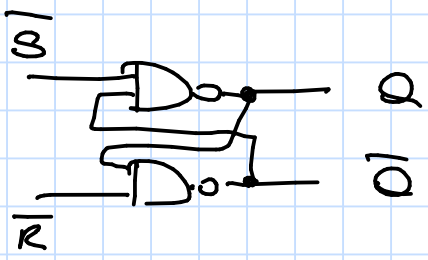
circuito "doublegica"

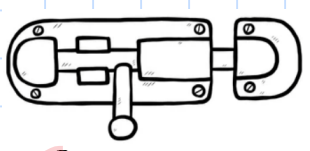




$\bar{S}$ a zero ⇒ Q va a 1
$\bar{Q}$ va a 0

$\bar{R}$ a zero ⇒ $\bar{Q}$ va a 1
Q va a 0





SR Latch

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	0	1	1	⇐ ILLEGAL
0	1	1	0	Set Command
1	0	0	1	reset Comand
1	1	Hold		