CS622A
Advanced Computer Architecture
Report on Assignment 1

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4 October 2020

Abstract

This document reports the results obtained from the simulation of multilevel cache. Given L1 cache miss traces for **six SPEC CPU 2006** applications were passed through L2 and L3 Cache. Cache inclusion policies used are inclusive, exclusive and non-inclusive-non-exclusive (NINE), for Set Associative and Fully Associative Cache with LRU and Belady as Replacement Policies.

PROBLEM 1

To simulate a two-level cache(L2 and L3) hierarchy and pass the L1 cache miss trace of given Six applications through them, considering both L2 and L3 as **Set Associative** Cache with **LRU** as the replacement policy.
I. **Results Obtained**

1. **Case A**: L2 and L3 are **Inclusive**

INCLUSIVE		**L2**		**L3**	
Application	**L1 Misses**	**Hits**	**Misses**	**Hits**	**Misses**
h264ref	2368109	1398442	969667	627507	342160
hmmer	3516421	1773033	1743388	1352161	391227
bzip2	11269773	5871585	5398188	3951787	1446401
sphinx3	10924045	2103689	8820356	612992	8207364
gcc	15388029	12351569	3036460	1663053	1373407
gromacs	3927468	3590618	336850	166318	170532

Table 1: Total number of Hits and Misses in L2 and L3 cache

2. **Case B**: L2 and L3 are **Exclusive**.

EXCLUSIVE		**L2**		**L3**	
Application	**L1 Misses**	**Hits**	**Misses**	**Hits**	**Misses**
h264ref	2368109	1402509	965600	19705	946323
hmmer	3516421	1781132	1735289	71954	1664362
bzip2	11269773	5872177	5397596	226578	5171972
sphinx3	10924045	2108908	8815137	265177	8551544
gcc	15388029	12358222	3029807	14417	3015780
gromacs	3927468	3590745	336723	41231	297037

Table 2: Total number of Hits and Misses in L2 and L3 cache

3. **Case C**: L2 and L3 are **NINE**.

NINE		**L2**		**L3**	
Application	**L1 Misses**	**Hits**	**Misses**	**Hits**	**Misses**
h264ref	2368109	1042509	965600	632054	333546
hmmer	3516421	1781132	1735289	1358944	376345
bzip2	11269773	5872177	5397596	3951738	1445858
sphinx3	10924045	2108908	8815137	609991	8205146
gcc	15388029	12358222	3029807	1663555	1366252
gromacs	3927468	3590745	336723	166263	170460

Table 3: Total number of Hits and Misses in L2 and L3 cache

II. **Analysis And Explanation**(based on Table 1,2 and 3)
Some of the observations on the simulation results.

0.1 L3 Misses: Inclusive IS GREATER THEN NINE IS GREATER THEN Exclusive.

Due to non-similarity of data in L2 and L3, L3 cache in case of Exclusive policy will have most space . This explains why L3 misses in Exclusive are significantly lesser.
For Inclusive L3 misses is slightly more then NINE, This came from the fact that eviction from L3 also evicts from L2 for Inclusive policy, which is not the case with NINE. So, an access to a block evicted from L3 would encounter a hit in L2 for NINE but would unnecessarily miss in both L2, L3 in Inclusive case.

0.2 L2 Hits/Misses (Exclusive) IS EQUAL TO L2 Hits/Misses (NINE.)

If the lower level cache contains only blocks that are not present in the higher level cache, then the lower level cache is said to be exclusive of the higher level cache.
This is observed because the addresses that are present in case of Exclusive policy are same as that of NINE, even though in different configuration.
Analyzing all possibilities:

- **L2 Hit:** No changes.
- **L3 Hit:** The block gets added to L2 Cache. Block is invalidated from L3 cache in exclusive.
- **L3 Miss:** The block is brought from memory and added to both L2 and L3 cache.

0.3 L2 Misses: Inclusive IS GREATER THEN Exclusive IS EQUAL TO (NINE).

If a block receives hits in L2 cache constantly , its rank in the LRU indexing will be quite high. As a result, the block will usually never be evicted from L2. But its age in L3 will drop significantly and might even become victim to an eviction. Following the Inclusive policy, it will also have to be removed from L2 which would unnecessarily increase L2 misses.

PROBLEM 2

To calculate Cold, Capacity and Conflict misses in L2 and L3 Set Associative Cache with LRU replacement policy. Also to calculate Cold and Capacity misses when L2 is Set Associative and L3 is Fully Associative with LRU and Belady's replacement policy.

I. L2 and L3 are both Set Associative Cache.

A. Results Obtained

- Replacement Policy: **LRU**

SET ASSOCIATIVE	**L3**		
Application	**COLD**	**CONFLICT**	**CAPACITY**
h264ref	63703	302599	157419
hmmer	75885	350908	334659
bzip2	119753	1412078	1382578
sphinx3	122069	8167227	7847586
gcc	773054	1333525	1304109
gromacs	107962	137684	126308

Table 4: COLD,CONFLICT AND CAPACITY misses in L3 Cache

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II. L2 is Set Associative and L3 is Fully Associative.

- Replacement Policy: **LRU**

FULLY ASSOCIATIVE	L3	
Application	**COLD**	**CAPACITY**
h264ref	63703	303185
hmmer	75885	344257
bzip2	119753	1328638
sphinx3	122069	8354528
gcc	773054	1337159
gromacs	107962	136601

Table 5: COLD AND CAPACITY misses in L3 Cache

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- Replacement Policy: **Belady's Optimal Policy**

FULLY ASSOCIATIVE	L3	
Application	**COLD**	**CAPACITY**
h264ref	63703	78838
hmmer	75885	120681
bzip2	119753	504073
sphinx3	122069	3035919
gcc	773054	906527
gromacs	107962	110487

Table 6: COLD AND CAPACITY misses in L3 Cache

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II. **Analysis and Explanations.**

1. As the number of unique blocks accessed in the trace files remains unaffected by the Associativity and Replacement policy used in Cache hierarchy . That's why number of COLD misses in L3 Cache are equal in all 3 above tables for each application.

2. Belady's optimal replacement policy checks the future references of the blocks present in the cache and replaces the ones which are accessed furthest in the future. While LRU replacement policy evicts the block without any knowledge of its further references. That's the reason number of capacity misses are observed to be less with Belady's optimal replacement policy in comparison to LRU for L3 Cache.