Fully CMOS Programmable Voltage Adder/Subtractor

Montree Kumngern
Department of Telecommunications Engineering, Faculty of Engineering,
King Mongkut's Institute of Technology Ladkrabang,
Bangkok 10520, Thailand
e-mail: kkmontre@kmitl.ac.th

***Abstract*—This paper presents a new programmable voltage adder/subtractor circuit. The proposed circuit is based on differential difference current conveyors and MOS switches. The adder/subtractor yields advantages over previous adders and subtractors in view of the less active components, low power consumption and its function to be programmable by digital codes which is suitable for integrated circuit implementation. Simulation results using PSPICE program are also obtained. From simulation results, it finds that the operation range of the proposed adder/subtractor is ±1.5V with a supply voltage of ±2V and the operation frequency is up to 100MHz.**

Keywords–adder/subtractor; differential difference current conveyor; digitally programmable

I. INTRODUCTION

Second generation current conveyors (CCIIs) have been found very useful in many applications. This is attributed to their high signal bandwidths, greater linearity, and larger dynamic range that operational amplifiers (op-amps) based ones [1]–[3]. In 1986, a modified current conveyor called the differential difference current conveyor (DDCC) was also presented [4]. This DDCC has been developed again by Chiu *et al.* [5]. The DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability).

Adder and subtractor circuits can be applied widely in communication and electronic systems, such as digital encoder, automatic gain amplifier, AM and FM modulations and neural networks. Therefore, several adders and subtractors have been reported in the technical literature [6]–[10]. In [6]–[7], voltage adder/subtractor circuits have been proposed. However, they provide only a positive voltage output operation range, although both positive and negative supply voltages are applied. In [8], Fried and Enz proposed a simple and accurate voltage adder with MOSs biased in weak-inversion, which is suitable for low power circuit application. However, its frequency performance and voltage operation range are limited. The operational amplifier (op-amp)-based adder/subtractor circuit in [9] offers the simplest way to obtain both positive and negative voltage output operation range, but the op-amp-based adder/subtractor uses passive resistors, although these resistors can be substituted by MOS-resistors, the drawback of using many devices and consuming high power of the op-amp still exists. Moreover, the drawback of these circuits is the well-known limitations of the op-amps.

Recently, a new technique for realizing programmable adder/subtractor using a current conveyor analogue switch is proposed [10]. The circuit uses the bias current of the current conveyor which makes program possible through the bias current. When it applies to encoder, the advantages of this circuit identified by the author are the following:

(1) The encoder uses fewer devices.
(2) The encoding formats of the encoder circuit can be changed by the voltage levels fed to the encoder whereas the encoding formats of a conventional encoder using digital gates can be changed by changing the circuit configuration. This shows that this encoder provides more flexibility.
(3) The encoder yields the voltage level output but a conventional encoder using digital gates yields the digital output. Thus the proposed encoder is more suitable for wireless analogue communication than a conventional one: frequency modulation (FM) by using an additional voltage-controlled oscillator and amplitude modulation (AM) by using an additional voltage controlled gain amplifier. For a conventional encoder, to obtain an FM or AM signal by using the same method, it needs a digital-to-analogue converter to change the digital output to the voltage, which is unnecessary for the proposed encoder.

With respect to (1)–(3) above, the circuit of [10] is a good adder/subtractor circuit for IC fabrication. However, it suffers from three disadvantages. First, the circuit uses an excessive active component, such as for a three-input adder/subtractor, it employs three CCIIs and four MOS resistors. Second, the amplification and attenuation of the circuit is controlled by current which applies through the bias current of the current conveyor. Therefore, if the voltage signal (i.e. digital signal) is supplied, the voltage-to-current converter is may be required. Third, the circuit is suitable for a high impedance load. If the low impedance load is applied, the circuit needs a voltage buffer at an output.

In this paper, we pursue the objective of developing adder/subtractor that is suitable for IC fabrication. We propose a new circuit that improves on the advantages of the circuit of [10] while overcoming the disadvantages. For a three-input adder/subtractor, the proposed circuit employs only one DDCC, six MOS switches and three inverter

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circuit (6 MOS transistors). In particular, the circuit has the following features:

(1) The proposed a three-input adder/subtractor uses 24 MOS transistors whereas the proposed circuit in [10] uses 51 MOS transistors; hence when the proposed circuit is fabricated, the proposed circuit will be used small area of chip than the previous adder/subtractor.

(2) For application to digitally programmable, the digital signal can be directly controlled the MOS switch without additional voltage-to-current converter circuit.

(3) It possesses low output impedance voltage signals.

II. Circuit Description

Fig. 1 shows the circuit symbol of the DDCC. The CMOS implementation for DDCC can be shown in Fig. 2. The port relations can be characterized by the following matrix equation:

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix}. \quad (1)$$

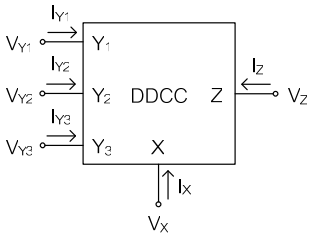


Fig. 1. Electrical symbol of DDCC.

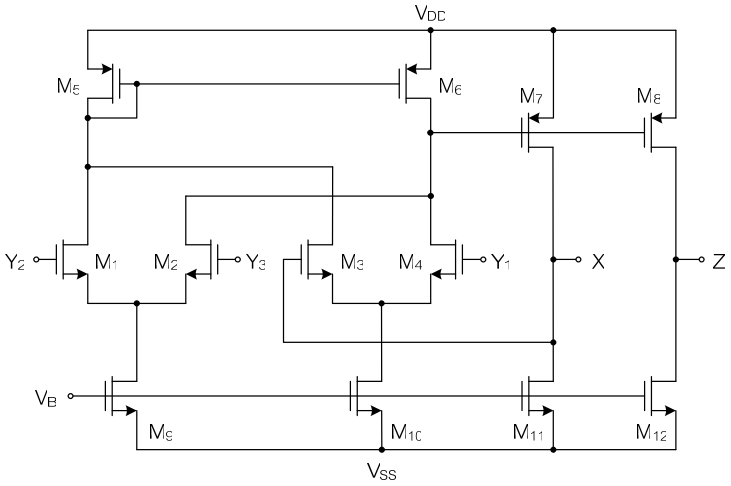
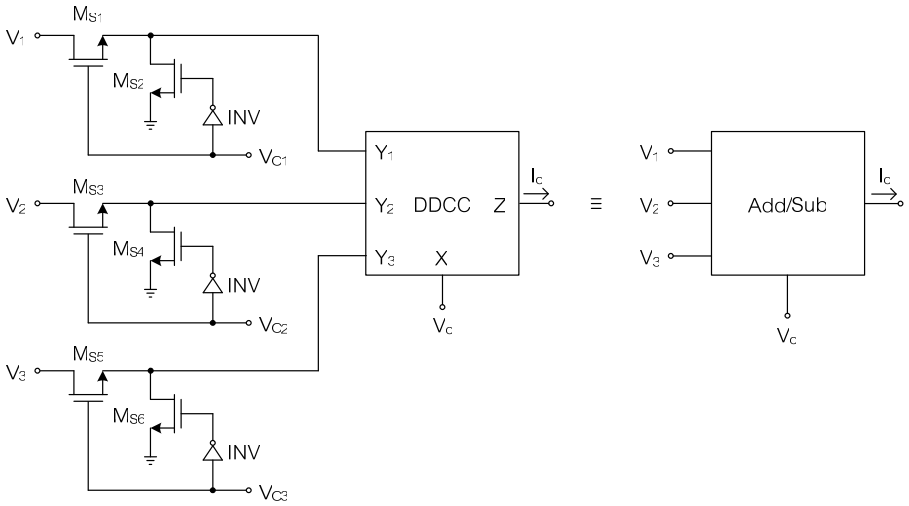
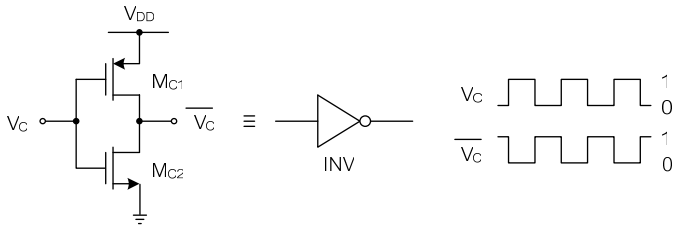


Fig. 2. CMOS implementation for DDCC.



(a)



(b)

Fig. 3. (a) Proposed programmable three-input adder/subtractor circuit, (b) MOS inverter.

TABLE 1. OPERATION OF THE PROPOSED THREE-INPUT PROGRAMMABLE ADDER/SUBTRACTOR.

V_{C1}	V_{C2}	V_{C3}	V_o
0	0	0	0
0	0	1	V_3
0	1	0	$-V_2$
0	1	1	$-V_2+V_3$
1	0	0	V_1
1	0	1	V_1+V_3
1	1	0	V_1-V_2
1	1	1	$V_1-V_2+V_3$

The proposed a three-input adder/subtractor is shown in Fig. 3. The proposed circuit consists one DDCC, six-MOS transistor switches (M_{s1} to M_{s6}) and three MOS inverters. Assuming that voltages V_{C1}, V_{C2} and V_{C3} are applied, using (1), the output voltage of proposed circuit is

$$V_o = V_1 - V_2 + V_3 . \quad (2)$$

The operation of proposed adder/subtractor can be explained. If the voltages V_{C1}, V_{C2} and V_{C3} are not supplied, the function of adder and subtractor (V_1-V_2+V_3) will be ignored (V_o=0). On the other hand, If the voltages V_{C1}, V_{C2} and V_{C3} are supplied, the function of adder and subtractor will be achieved (V_o=V_1-V_2+V_3). Each function of adder and subtractor can be obtained in Table 1. It can see that the output voltage can be programmed by V_{C1}, V_{C2} and V_{C3}, where "0" in Table 1 is having no voltage for V_C and "1" is a constant voltage.

III. CIRCUIT ANALYSIS

The impedance approximation can be derived by small signal model analysis of Fig. 3. Input impedance of the proposed adder/subtractor is the impedance at node Y of a DDCC. Due to input port for voltage controls (V_{c1}, V_{c2}, V_{c3}) is the gate of MOS transistor, impedance at port V_c (Z_c) is extremely high. Then input port impedance Z_c is approximately expressed as

$$Z_c \approx \infty . \quad (3)$$

Input impedance (Z_{in}) for voltage inputs (V_1, V_2, V_3) is the impedance at node Y of a DDCC serried with g_{ds} of MOS switch operating in saturation region. Then, input port impedance can be approximated as

$$Z_{in} \approx \infty + g_{ds(sw)} \quad (4)$$

where $g_{ds(sw)}$ is the conductance between drain and source of MOS switches in saturation region.

Output impedance of the proposed chopper modulators is the impedance at node X of a DDCC (Fig. 2). The terminal impedance looking into X can be derived by setting V_{in} and V_C to zero, applying a test voltage V_o at node X, and calculating the current I_o. The output impedance can be obtained as

$$Z_o \approx \frac{(g_{m3}+g_{m4})(g_{d12}+g_{d34}+g_{d6})}{2g_{m3}g_{m4}g_{m7}} \quad (5)$$

where g_{mi} is the transconductance and g_{di} is the drain conductance of transistor M_i, respectively. From equation (5), the following parameters are given as g_{m3}=g_{m4}=1.19×10^{-4} A/V, g_{m7}=2.86×10^{-4}A/V, g_{ds12}=g_{ds34}=5.42×10^{-7}A/V and g_{ds6}= 1×10^{-6} A/V. Output port impedances calculation is obtained around 32.5Ω agreed with the theoretical.

IV. SIMULATION RESULTS

To verify the theoretical prediction of the proposed circuit, the proposed programmable adder/subtractor in Fig. 3 has been simulated using PSPICE simulation program. The CMOS DDCC in Fig. 2 was simulated using the 0.5μm MIETEC [11]. The transistor aspect ratios are listed in Table 2 [11], the supply voltages are V_{DD}=−V_{SS}=2V and the bias voltage is V_B=−1.2V. The W/L ratios of MOS inverters (M_{C1} and M_{C2}) and MOS switches (M_{S1} to M_{S6}) are 2μm/2μm. The constant voltage V_C for turning on the MOS switch is 1.5V and for turning off is 0V.

Sine wave signals were supplied to V_1, V_2 and V_3. When the frequencies were increased, it was found that the proposed adder/subtractor could operate with the -3dB bandwidth of about 150MHz.

For the tested proposed programmable, its output voltage V_o is V_1-V_2+V_3. Fig. 4 shows the operation of proposed programmable adder/subtractor when applies a DC 0.1V at a three-input of the proposed digitally programmable adder/subtractor. Theoretically, the digital levels, 000, 001, 010, 011, 100, 101, 110, and 111 yield the DC outputs: 0, 0.1, -0.1, 0, 0.1, 0.2, 0, and 0.1V, respectively. It can see in Fig. 4 that the proposed circuit can be operated as adder/subtractor corresponding with theory.

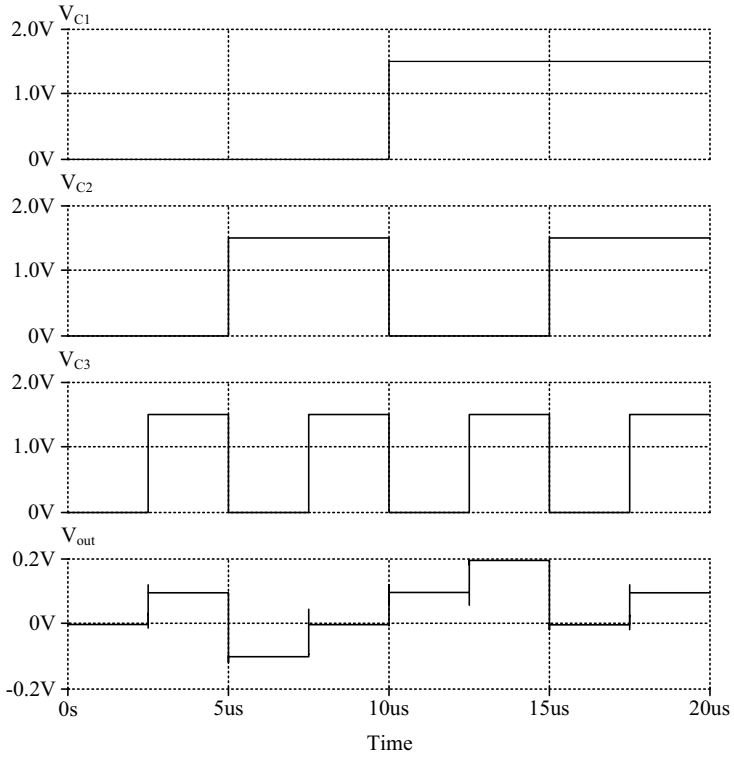


Fig. 4. Operation of the proposed programmable adder/subtractor.

TABLE 2. TRANSISTOR ASPECT RATIOS OF THE USED DDCC.

MOS transistor	W/L
M_1-M_4	1.6/1
M_5-M_6	8/1
M_7-M_8	20/1
M_9-M_{10}	29/1
M_{11}-M_{12}	90/1

V. CONCLUSIONS

In this paper, a programmable voltage adder/subtractor has been presented. Compared previous adders and subtractors, the proposed adder/subtractor uses lesser transistors, yields simpler structure and offers lower output impedance. Moreover, its operation can be directly programmable by a digital signal. It is to be further note that the proposed adder/subtractor can be realized an encoder as same the recent work in [10]. Hence when it applied to the encoder it also yields advantages in view of a number of devices, a changeable encoding format by the voltages, and a DC output suitable for wireless analogue communication as same the recent work [10].

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REFERENCES

[1] K. Smith and A. Sedra, "The current-conveyor-a new circuit building block," IEEE Proceeding, vol. 56, pp. 1368–1369, 1968.
[2] A. Sedra and K Smith, "A second-generation current-conveyor and its applications," IEEE Transactions on Circuit Theory, vol. CT-17, pp. 132–134, 1970.
[3] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, "Current controlled bandpass filter based on translinear conveyors," Electronics Letters, vol. 31, pp. 1727–1728, 1995.
[4] K. Pal, "Modified current conveyors and their application," Microelectronic Journal, vol. 20, pp. 37–40, 1986.
[5] W. Chiu, S. I. Liu, H. W. Tsao, and J. J. Chen, "CMOS differential difference current conveyors and their applications," IEE Proceeding of Circuits, Devices and System, vol. 143, pp. 91–96, 1996.
[6] S. W. Tsay, and R. Newcomb, "A neuro-type pool arithmetic unit," in Proceeding of IEEE ISCAS'91, Singapore, pp. 2518–2521, 1991.
[7] H. Chaoui, "CMOS analogue adder," Electronics Letters, vol. 31, pp. 180–181, 1995.
[8] R. Fried and C. C. Enz, "Simple and accurate voltage adder/subtractor," Electronics Letters, vol. 33, pp. 944–945, 1997.
[9] T. L. Floyd, "Basic operational amplifiers and linear integrated circuits," Macmillan, USA, 1994.
[10] A. Monpapassorn, "Programmable wide range voltage adder/subtractor and its application as an encoder," IEE Proceeding of Circuits Devices and Systems, vol. 152, pp. 697–702, 2005.
[11] M. Kumngern and K. Dejhan, "DDCC-based quadrature oscillator with grounded capacitors and resistors," Active and Passive Electronic Components, vol. 2009; doi: 10.115/2009/987304.