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SET Detection and Radiation Hardened Pipelined 8-bit ADC Using 180 nm Technology

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***Abstract*—In space and nuclear applications environment, there is a large amount of radiation present which seldom causes a soft error in electronic circuitry. The current trends in VLSI industry focus on decreasing the size of the transistors and fabricating a larger number of transistors on a chip with the same area. The threshold voltage of the transistor decreases on scaling. Due to radiation, when a particle hits a sensitive node of a digital circuit, the charge gets accumulated on that node. This small amount of additional voltage or charge can sometimes lead to a change in the state (soft error) of a digital circuitry. This paper presents a Radiation Hardened Pipelined ADC, where the effect of radiation is modeled by a double exponential pulse (DEP). DEP has been deemed as the most effective method for circuit based simulation. DEP is used to introduce the charge at a sensitive node to mimic the effect of radiation. The 8 bit ADC is implemented using 180 nm technology node with Cadence Virtuoso.**

***Index Terms*—Pipeline; Soft Errors; Single Event Transients (SET)**

I. Introduction

IN natural environment, radiation is due to the presence of heavy ions (atomic number equal to or greater than two, Suge *et al* [1]) or ionizing radiations such as alpha particles, protons or neutrons. When a semiconductor device is impacted by such ionized particles, there is a probability of electron-hole pair generation. The generation of electron-hole pair results in the accumulation of charge in the vicinity of the PN junction device [2]. If the accumulated charge exceeds the critical charge limit (i.e. the minimum charge, which can bring a change in the existing state of the transistor), a soft error in the digital circuitry might be introduced [2]. When a voltage transient is introduced in a circuit, there is a pile-up of charges at a node. If this collected charge is more than the critical charge, the state of the flip-flop changes and hence a soft error is said to have occurred. The process of attaining/designing a radiation resistant electronic component, which is resistant to ion particles impact is known as radiation hardening [3].

There are two radiation damages which occur in a semiconductor device. First is Displacement Damage which is because of displacement of atoms. Second is Ionization Damage, which is because of charge carriers being trapped in the insulating region (silicon dioxide) [1].

One way to detect the SEE (single event effect) is to take similar devices, operating under same conditions, with the only difference being that one device is provided with a double exponential pulse (DEP) while other is not. The outputs of both the devices are given to the inputs of XOR gate. As shown in Fig. 1, the first device (i.e. model device) is provided with same input only and second device (i.e. device under test) is provided with the same input as well as excited with a double exponential pulse simultaneously [4]. The output of model device is p which can be either a 0 or a 1. The output of device under test is q which can again be a 0 or a 1. The Single Event Transient can be detected if the outputs are different (i.e. p=0 and q=1 or p=1 and q=0). The outputs of these two devices are given to a XOR gate. If the inputs of the XOR device are different than XOR writes a 1 in the output (i.e. out). Hence when out=0, one can deduce that there is no effect of radiation on the circuitry and when out=1, then it can be concluded that a soft error has occurred. Therefore, a radiation hardening circuitry is required for proper operation. In this work, the conventional NAND gate of the D flip-flop are replaced with the RHBD NAND gate, Praveen *et al* [2].

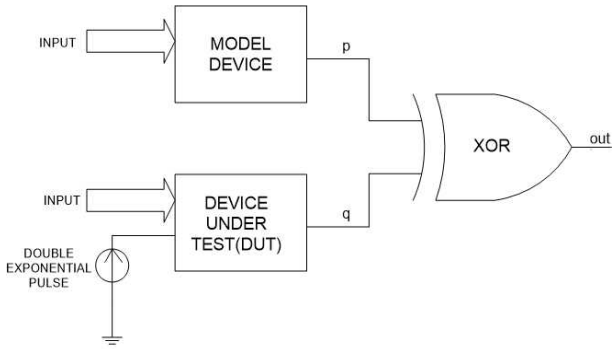

Fig. 1: Single Event Effect Detection

The effect of radiation can be seen either with device-level tools like TCAD or at circuit-level by modeled with double exponential pulse [1]. The circuit level radiation can be encountered in software packages such as Cadence Virtuoso tool. Recent work shows that the simulation at device-level and circuit-level can be combined together and is popularly known as mixed-mode simulation or mixed-level simulation [1] [5]. Scaling can be deemed as one of the effective methods in order to make a circuit radiation hardened [2]. By scaling, the size of the transistors is made big enough to tolerate critical charge.

With the rapid advancement in technology, there is a continuous shrinking in the device dimension to the deep sub-micron level. When the device dimensions are very small, the transistors become extremely vulnerable to particle hit [5] [11]. The chances of causing an error increases and this temporary

error is known as soft error. One way to model the effect of radiation in circuit is by using a DEP [12]. This method is most accurate for the modeling of radiation in circuit-based simulations and has been widely used by researchers in their work [2] [4] [6] [7] [8]. In 1982, the time-dependent double exponential pulse was developed by Messenger [6]. The DEP is a very efficient method for a circuit designer for testing the effect of radiation on circuits. The DEP can be modeled by [6].

$$I(t) = Io(e^{-\frac{t}{T_r}} - e^{-\frac{t}{T_f}}) \quad (1)$$

Where I_o is maximum value of current, T_r is rise time constant, T_f is fall time constant.

II. Proposed work

This paper derives an architecture of ADC from Manju *et al* [9] and Jay Shri *et al* [10]. In this work, the most sensitive part of the circuit is identified in the architecture (i.e. flipflop). This flip-flop consists of various conventional NAND gates, which are highly sensitive to the effect of radiation. This radiation may produce an erroneous value by altering the circuit operation. The pipelined architecture has the advantage of easily expandable number of stages and it allows power minimization, digital gain calibration, digital error correction through capacitor scaling [9].

In this proposed work, the conventional NAND gates of flipflop is replaced with Radiation Hardening by Design (RHBD) NAND gate, Praveen *et al* [2]. Fig. 2 depicts RHBD NAND gate. The difference between the critical charge of conventional NAND gate and critical charge of RHBD NAND gate varies for different input combinations. For P=0, Q=0, the critical charges are 56.3fC and 293fC respectively. For P=0, Q=1, the critical charges are 27.3fC and 166fC respectively. For P=1, Q=0, the critical charges are 41.5fC and 166fC respectively. For P=1, Q=1, the critical charges are 732fC and 4800fC respectively. This data shows RHBD NAND gate require more charge to change the state than its conventional counterpart. All this data is for a DEP with duration of 300 pS and different values of peak current. [2].

The presence of soft error in RHBD NAND gate can be detected by the technique mentioned in Fig. 1. In this technique, two RHBD NAND gates are followed by XOR gate. The first RHBD NAND gate is provided with inputs P and Q. The second RHBD NAND gate is provided with inputs P and Q along with a DEP at the sensitive node X. It is assumed that the particle strikes the RHBD gate at the node X. The outputs of these RHBD NAND gates are then fed to the inputs of the XOR gate. If the outputs of both RHBD NAND gates are same the output of the XOR gate is 0 and hence, it can be concluded that there is no soft error. If there is a change in an output of the second RHBD NAND gate from the first RHBD NAND gate, the output of the XOR gate is changed to 1 and one can deduce that a soft error has occurred in the second RHBD NAND gate. The first RHBD NAND gate is a model device, while the second device is called Device Under Test (DUT) [4]. Using this methodology, one can test any digital circuitry for soft error due to radiation effect.

In the proposed circuit, the RHBD NAND gate and flipflop are tested by using a model and a DUT method [4]. The output of the XOR gate is 0 for all the time. Hence, this radiation hardened flipflop does not have a soft error in the presence of radiation. In this work, a Radiation Hardened ADC is achieved which gives correct output even in the presence of radiation.

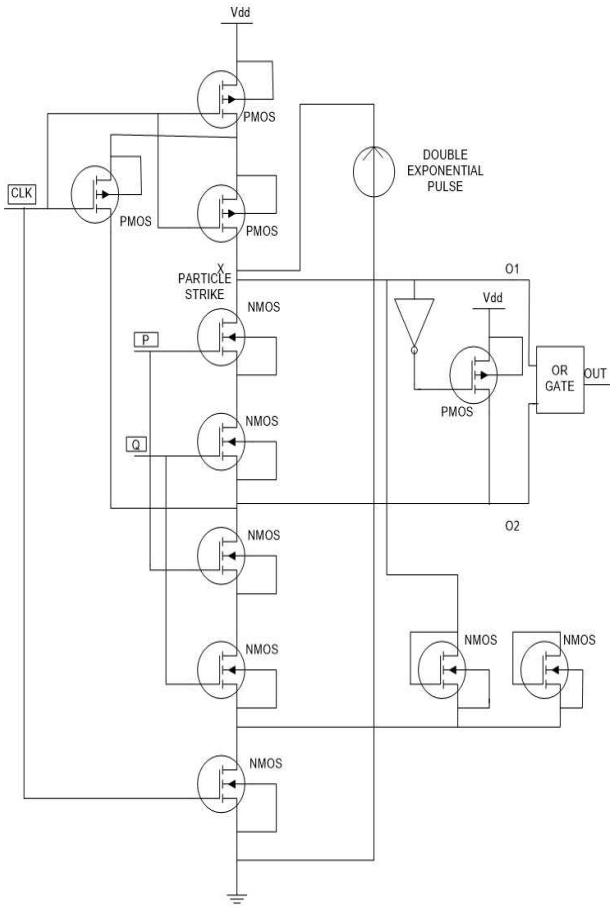

Fig. 2: RHBD NAND gate

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III. Schematic Diagram

The architecture in this paper is designed with the following components [9] [10]

A. Operational Amplifier (Op-Amp)

Fig. 3 depicts Op-Amp schematic diagram. There are two stages in Op-Amp. The primary stage is differential amplifier and the secondary stage is common source stage.

B. Sample and Hold circuit (S-and-H)

The S-and-H circuit consist of a switch and a storage element. Fig. 4 depicts the schematic of S-and-H. The basic circuitry of an S-and-H circuit is a control input and a capacitor which is used for storing the voltage. The capacitor is followed by a buffer. When the control signal allows a connection, the output voltage will be replicated with input at the capacitor.

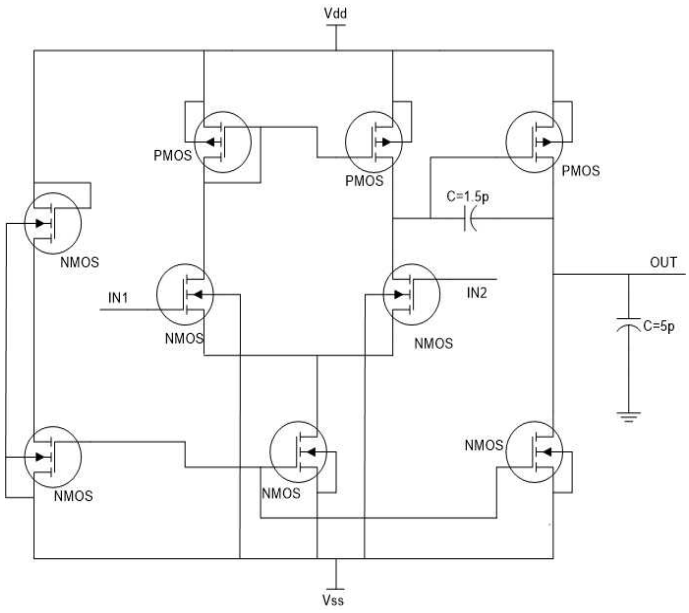

Fig. 3: Op-Amp circuit

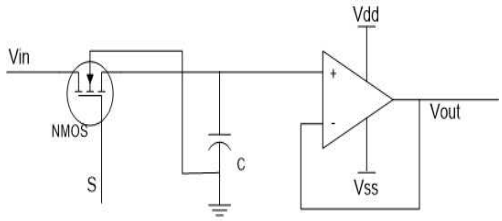

Fig. 4: Sample and Hold circuit

C. Comparator

Fig. 5 depicts comparator circuit, two inverters are connected one after the other. Two inverter connected together are used as a comparator circuit.

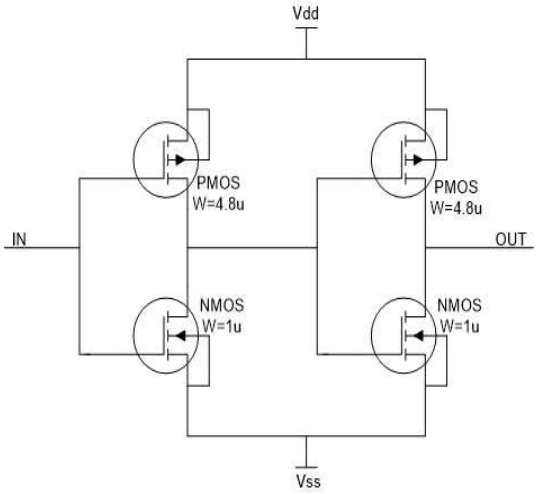

Fig. 5: Two inverter as Comparator

D. D-flipflop

In this architecture, the D-flipflop is used in a master-slave configuration, which is used for storing one-bit information and as a delay element. The master configuration is provided with a positive clock while a negative clock (i.e. output of inverter) is provided to the slave configuration. Fig. 6 depicts the schematic of D flipflop.

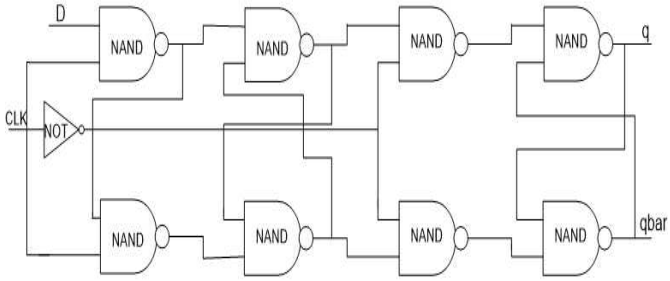

Fig. 6: D-flipflop

E. 1-bit DAC

1-bit DAC is used to obtain an analog equivalent of the digital bits. This 1-bit DAC uses a multiplexer which passes the signal V_{ref1} or V_{ref2}. The multiplexer passes V_{ref1} from upper part while the lower part passes V_{ref2}. The schematic of 1-bit DAC is illustrated in Fig. 7.

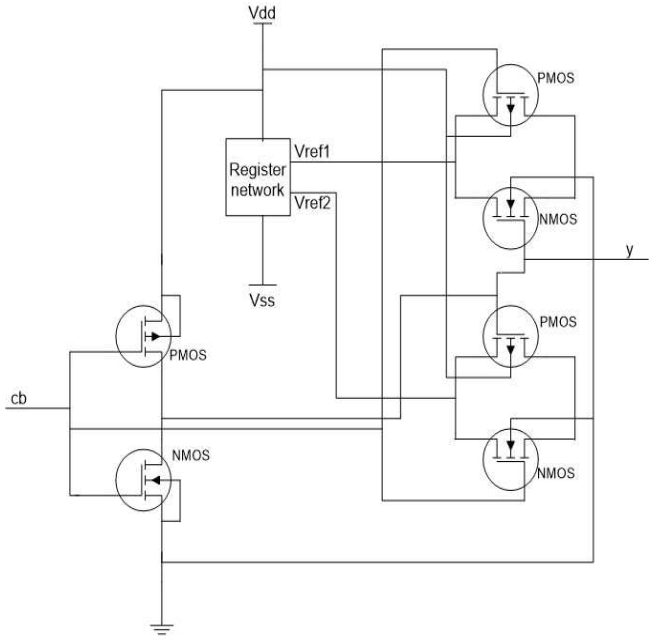

Fig. 7: 1-bit DAC

F. Inverting Amplifier

The inverting amplifier is designed for a gain of 2. This acts as the gain block for every pipelined structure. Each gain stage is the product of n (number of stage) and the inverting

amplifier gain i.e. 2. Hence each stage has gain of 2n. Fig. 8 illustrates the schematic of inverting amplifier.

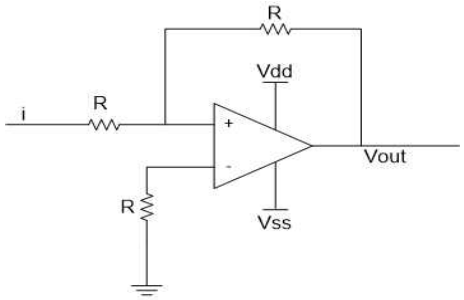

Fig. 8: Inverting Amplifier

G. 1-bit single stage ADC

On combining the above-mentioned components, one can obtain a single bit ADC. The schematic of 1-bit single stage ADC is shown in Fig. 9.

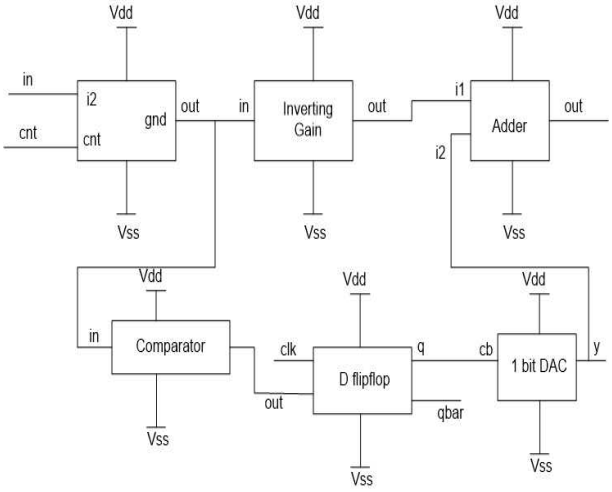

Fig. 9: 1-bit single stage ADC

H. 8-bit pipelined ADC

On combining the eight stages of the 1-bit single stage ADC, an 8-bit ADC has been obtained which is depicted in Fig. 10.

IV. SIMULATION RESULT

The simulation results are shown below:

A. Op-Amp Circuit Simulation

Fig. 11 illustrates the magnitude plot of Op-Amp circuit. The vertical axis represents the magnitude plot (in dB scale) while the horizontal axis represents the frequency (in Hz) the approximate gain is 28.48dB.

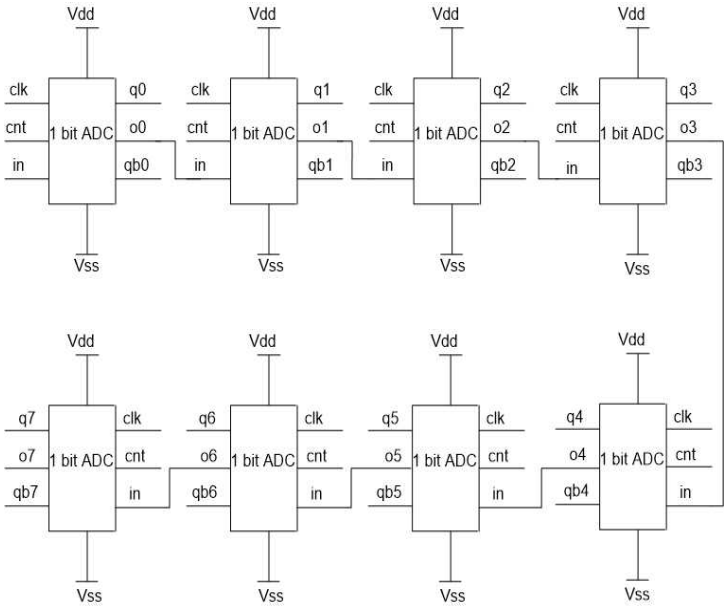

Fig. 10: 8-bit pipelined ADC

B. Sample and hold simulation (S-and-H)

Fig. 12 shows the output of S-and-H circuit. The input applied is sinusoidal signal which is multiplied with pulse input. First signal shows sinusoidal input while second is S-and-H output.

C. Comparator simulation

Fig. 13 illustrates the comparator circuit output. The input is compared with a reference voltage. If the input voltage is greater than the reference voltage, comparator gives 1.8V else comparator gives -1.8V as output.

D. RHBD NAND simulation

Fig. 14 illustrates the simulation of RHBD NAND gate. DEP with peak value of 3.5mA and duration of 300pS is applied to the RHBD gate, RHBD output does not suffer from the radiation effect. First input applied is DEP, second and third are inputs p and q and the fourth one is output of RHBD NAND gate.

E. D flip-flop simulation

Fig. 15 depicts the output of D-flipflop. The conventional NAND gates are replaced by RHBD NAND gates. The output does not suffer from the presence of the DEP when input pulse is less than 2mA in magnitude and pulse width of 300pS. First and second pulse are the outputs of flipflop qbar and q respectively. Third pulse is input D, while fourth signal is clock pulse.

F. 8-bit pipeline ADC simulation

Fig. 16 illustrates the output of the eight-bit ADC. First signal shows sinusoidal input signal, second signal shows

pulse train, while third signal shows S-and-H output. The last 8 outputs are 8 bits of the ADC (i.e. from MSB (D7) to LSB (D0)).

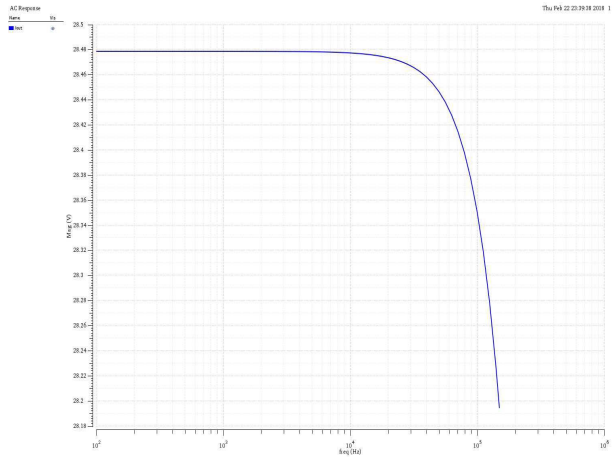

Fig. 11: Op-Amp Magnitude plot

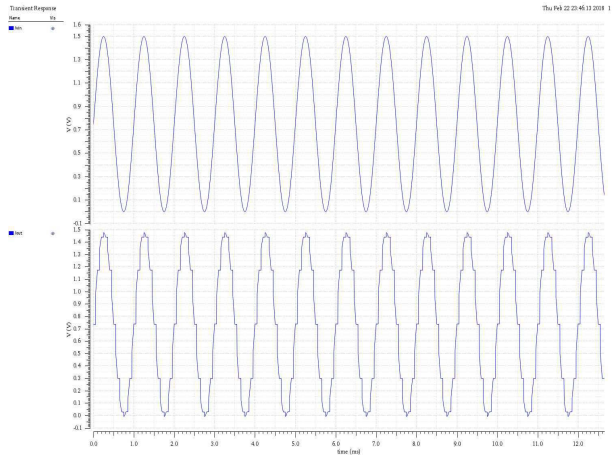

Fig. 12: Sample and Hold circuit output

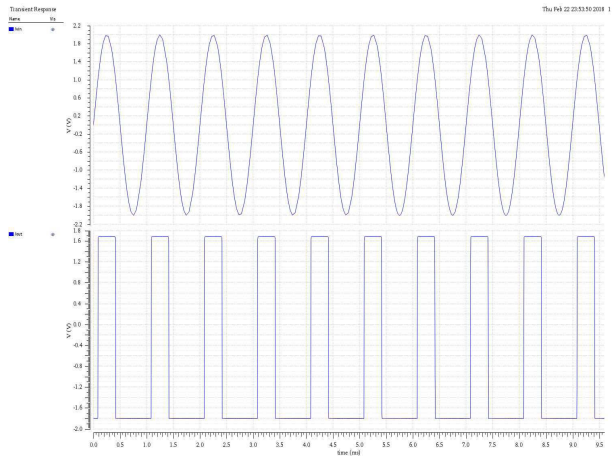

Fig. 13: comparator output

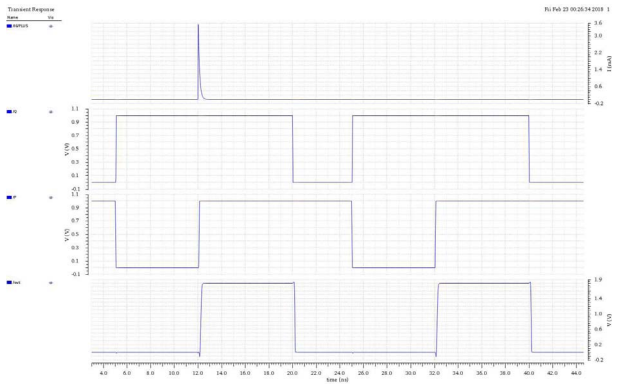

Fig. 14: Output of RHBD NAND gate in presence of SET pulse

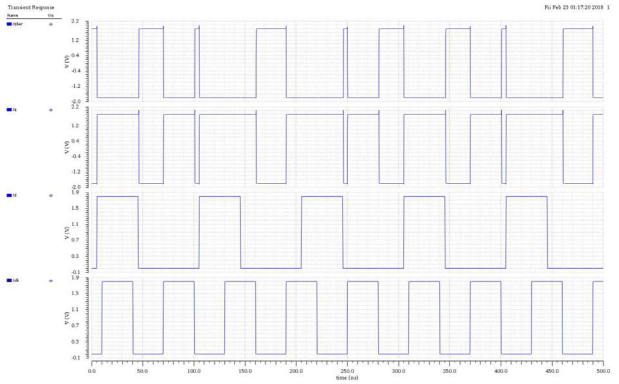

Fig. 15: Output of D-flipflop by using RHBD NAND gates in presence of DEP

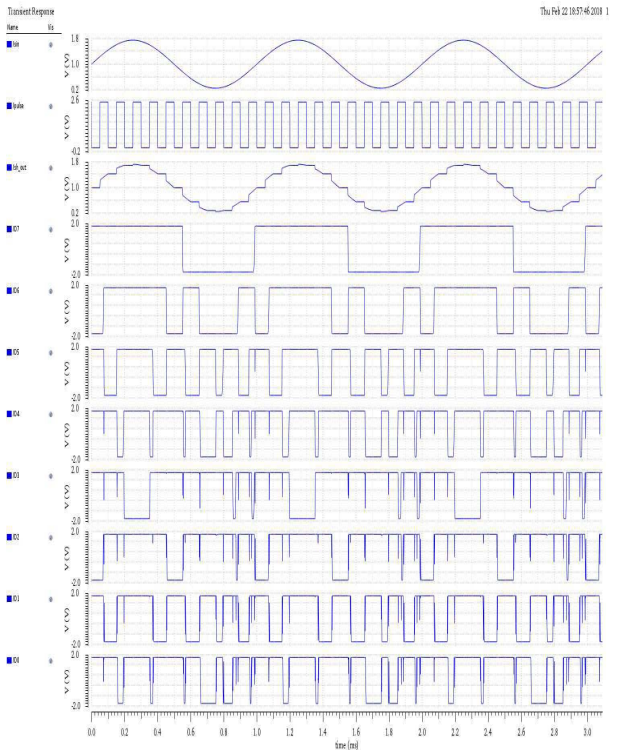

Fig. 16: Output of 8-bit pipelined ADC

V. CONCLUSION

The logic gates along with information storing elements (such as latch, flipflop etc) are highly sensitive to radiation. The effect of radiation sometimes causes soft errors. At times, there may arise a case when there is an overall loss of functionality in the circuitry. Radiation effects may result in erroneous value at the output of the circuit or cause a temporary error. In this work, the digital circuitry is tackled to become radiation resistant up to certain radiation level. As radiations cause the reliability of the system to suffer, a radiation tolerant circuitry is required that provides correct output even in the presence of radiation.

In this work, an 8-bit pipelined ADC is developed which is more radiation tolerant than its conventional counterpart. There is a scope to develop more radiation tolerant architectures which can serve as a groundwork for future research.

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