Design of 4-Bit Flash ADC using 180nm Technology

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Abstract— Analog to digital converter (ADC) is an integral part of communication and a crucial asset for digital signal processing. ADCs, find a wide variety of applications in today's digitized world. Flash ADCs are fastest among all the types of ADCs discovered so far. A 4-Bit Flash ADC has been designed using Cadence Virtuoso in 180nm CMOS technology. ADC has been developed using two stage open loop comparators, a priority encoder. The analog output of each comparator depends upon the input, the reference voltage supplied to the priority encoder, and finally, the digital output obtained. Parameters calculated are bandwidth (Mhz), resolution (mV) and power consumption (mW) are 79.53, 50, .005 respectively for comparator. For ADC calculated parameters are DNL, Delay(ms), Maximum input Frequency(Mhz), Rise time(ns), Fall time(ns), power consumption (mW) are .029, 1.9, 87.19, 15.89, 3.87,368.

Key words: Flash ADC, Comparator, Priority Encoder, Cadence Virtuoso, Power Dissipation, Delay

I. INTRODUCTION

Analog to Digital Converters (ADCs) are the most important devices, which connect analog world to digital world. ADC is a device that converts the input analog quantity to digital numbers. ADCs incorporate three fundamental parameters, which can't be changed once it has been planned, and the parameters include speed, resolution and power dissipation.

ADC, which is being outlined nowadays, requires an architecture having low power dissipation and high speed of operation. A single architecture cannot be used for all the applications as various types of ADCs differ from each other on the basis of performance parameters such as speed, power consumption, and resolution [1]. Hence, it is extremely vital to pick an ADC for every specific application. Distinctive kind of ADCs is accessible like SAR ADC, Dual-Slope ADC, Sigma Delta ADC and Flash ADC yet among all these; the most commonly utilized ADC is the Flash ADC due to its better tradeoff between its performance measurements. Flash ADCs are used for application where high speed and low resolution is required. Flash ADC has a bank of comparators testing the input signal in parallel. The comparator bank output is fed to an encoder logic circuit that produces a unique digital code for each voltage range. The device architecture utilizes vast quantities of resistors and comparators and is constrained to low resolutions, and on the off chance that it is to be quick, each comparator must keep running at generally high power levels. Thus, the issues of flash ADC incorporate constrained resolution, high power dissemination as a result of the huge Ease of Use number of active comparators and generally extensive (and in this manner costly) chip sizes.

The paper is organized as follows; Sect. II covers the Design concept and various sub-blocks involved in designing a 4-bit Flash ADC. Section III discusses result and discussion about the 4-bit Flash ADC. Section IV is the conclusion of the paper.

II. DESIGN METHODOLOGY FLASH ADC ARCHITECTURE

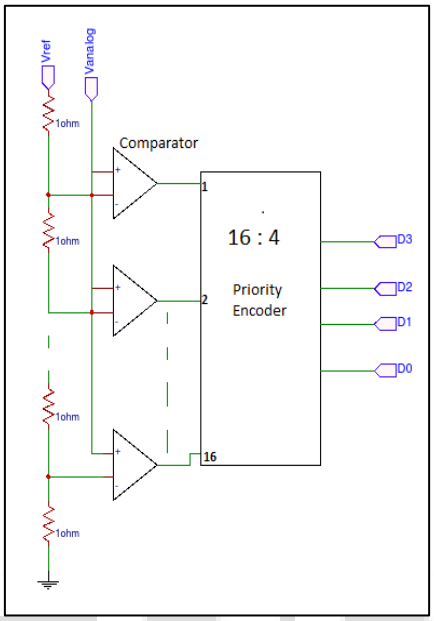

Fig. 1: Block Diagram of 4-Bit Flash ADC

Figure1 represents the basic block diagram of 4-bit Flash ADC. It consists of three primary components: resistors, comparators, and encoder. For N-bit Flash ADC 2^N resistors and 2^N–1 comparators are required. For 4-bit ADC the circuit utilizes 2^4-1= 16-1=15 comparators and 2^4=16 resistors [2].The comparator comprises of wide band and low gain stages cascaded together. At high frequencies, the low gain is obtained as it is hard to obtain high bandwidth and high gain at the same time. Each comparator has a reference voltage which is 1 LSB higher than that of the one underneath it in the chain. An analog voltage is sustained to every voltage comparator to contrast input voltage with reference voltages. The reference voltage is created by the resistive stepping stool circuit and relying upon the correlation made amongst V_{IN} and the comparator generates V_{ref}, 0 and 1 output. If V_{IN} is less than V_{ref}, the output is zero otherwise one. The output of the comparator is fed to the priority encoder to obtain the digitized output.

A. Comparator

Comparator plays an essential part in the design of Analog-to-Digital converters (ADC). The execution of the objective application is essentially impacted by the design of the comparator [3]. The speed and resolution of an ADC are affected by the input offset voltage, delay and input signal range of comparator.

Two stage open loop comparator consists of two different stages. The first stage comprises a differential amplifier and the second stage consists of output gain stage as shown in Fig. 1 As this circuit contains a minimum number of transistors, so its circuit area is small.

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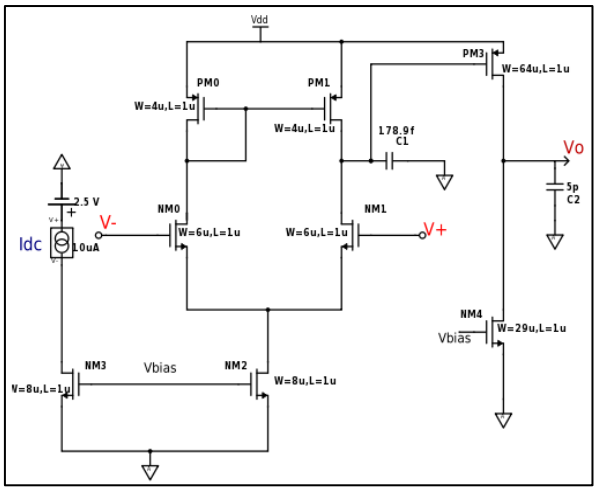

Fig. 2: Schematic of two stage open loop comparator

References	[6]	This work
Technology(µm)	.18	.18
Tool Used	SPICE	Cadence
Power supply(V)	1.8	2.5
Bias current(µA)	-	10
Resolution(mv)	-	50
Bandwidth (Mhz)	-	79.53
Slew rate(v/µs)	-	5
Power consumption (mW)	.345	.005

Table 1: Comparator's design specification and simulation results

Figure 3 demonstrates the DC response of the comparator circuit from that it can comprehend that the circuit is prepared to do recognizing even 50mV of distinction amongst V_{IN} and V_{ref}.

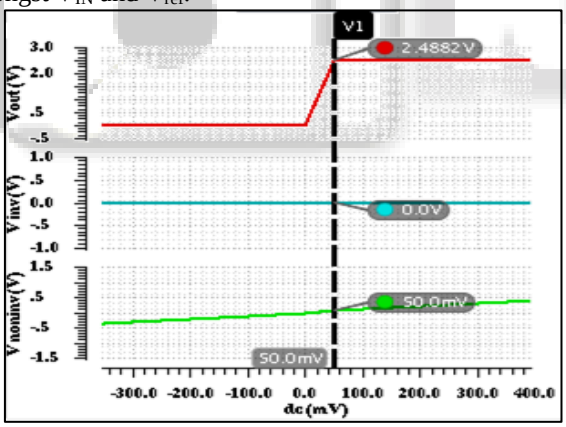

Fig. 3: Resolution of comparator

B. Priority Encoder

A Priority encoder is a circuit that packs various paired Binary input to a few outputs i.e. it compresses the multiple inputs. The priority encoder incorporates the priority function. In priority function, the input having the larger priority will be encoded first. Here in this circuit of the priority encoder, priority is defined by magnitude, higher the magnitude higher will be a priority. For example, if the pin5 and pin15 are simultaneously high than based on priority the output will be (1111)2=15.

The priority encoder is designed by using the very basic technique it consists of the simple encoder (i.e. designed by using 4-simple 8-bit or gates), 14-and and 16-not gates are used. [4] As the circuit is using many transistors in its design so its delay is 17.4ns.

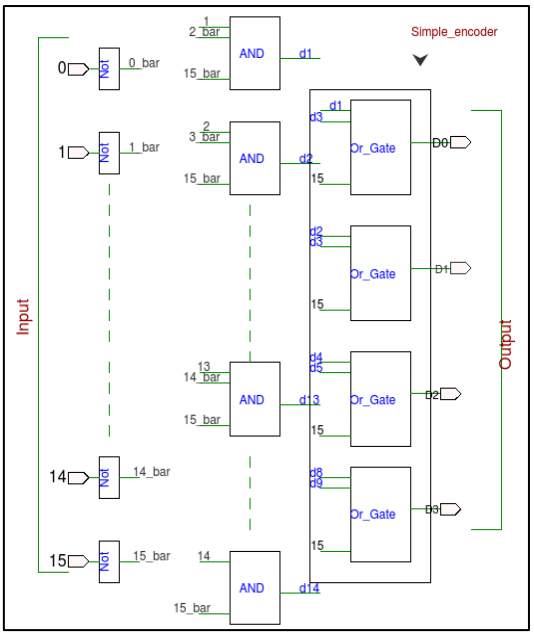

Fig. 4: Block diagram of priority encoder

Figure 5 shows the simulation of the priority encoder. When applied input at pin15 and pin5 the output is according to the priority.

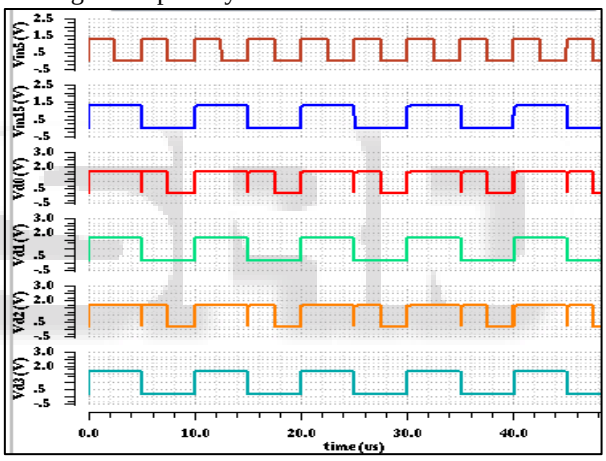

Fig. 5: Output waveform of priority encoder

III. SIMULATION AND RESULTS

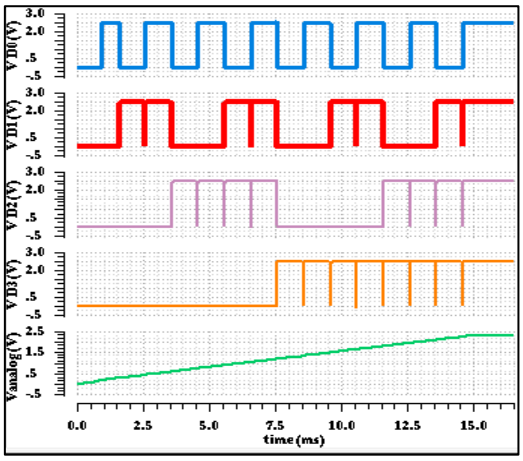

Fig. 6: Output waveform of 4-Bit Flash ADC

The 4-Bit Flash ADC is fed with vpwl (piece-wise linear voltage source) input having 16 paired points, period 0ms to 15ms i.e. each point is 1ms apart, voltage 0V and voltage2.25V (each voltage is .15 voltage difference).[5]

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Each voltage in the vpwl is of value of +k (i.e. resolution of comparator for example v2=.15+k, v3=.30+k….v16 =2.25+k. K is minimum value 50mV.The reference voltage is applied 2.4V.The output signal is digital output depending upon the input signal which compares with the reference voltage at respective nodes. DNL, noise, rise time, fall time, settling time and Delay have been evaluated from this output signal using calculator tool. Transient analysis is done for above parameters and for maximum input frequency, the AC analysis is done.

Vanalog	D3D2D1D0
0	0000
.15+k	0001
.30+k	0010
.45+k	0011
.60+k	0100
.75+k	0101
.90+k	0110
1.05+k	0111
1.20+k	1000
1.35+k	1001
1.50+k	1010
1.65+k	1011
1.80+k	1100
1.95+k	1101
2.10+k	1110
2.25+k	1111

Table 2: Digital output depending upon the input voltage

References	[8]	[7]	This work
Technology(µm)	.18	.18	.18
Power supply(V)	1.8	1.8	1.8-2.5
I/p range (V)	.5-1.1	0-1.8	0-2.25
Area(µm)^2	-	-	1000x800
Resolution(bits)	4	4	4
Noise(pV**2/HZ)	-	-	63.22
Max input Frequency (Mhz)	20	45	87.19
Delay(ms)	-	-	1.9
DNL	.7	1.04	.029
Rise Time(ns)	-	-	15.89
Fall Time(ns)	-	-	3.87
Settling time(ms)	-	-	14.68

Table 3: Flash Adc Design Specification and simulation results

IV. CONCLUSION

In this paper, 4-bit Flash ADC based has been proposed for reduction of DNL, Delay, and an increase in maximum input frequency. In this work, comparator was also designed as low power, less delay. The proposed 4-bit Flash ADC circuit showed improvement in DNL that is .029 more than double to previous work and improvement in maximum input frequency is also around double. Delay is 1.9ms that indicates that the ADC is very fast.

REFERENCES

[1] S. Park, Y. Palaskas and M. P. Flynn, "A 4-GS/s 4-bit flash ADC in 0.18_m CMOS," IEEE J. of Solid-State Circuits, vol. 42, no. 9, pp.1865-1872, Sep. 2007.

[2] S. Banik, D. Gangopadhyay and T. K. Bhattacharyya, "A low power 1.8V 4-bit 400 MHz flash ADC in 0.18_m digital CMOS," in Intl. Conf. Of VLSI Design, 2006.

[3] Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design,2nd ed., Oxford Indian Edition, 2006

[4] M. Morris Mano, Michael D. Ciletti:"Digital Design", Pearson Education Inc., pp. 167-168, Fourth Edition, 2008.

[5] Amritesh Ojha, Rajesh Mehra"Low Power Layout Design of Priority Encoder Using 65nm Technology", International Journal of Engineering Trends and Technology (IJETT), V23(9),450-453 May 2015. ISSN:2231-5381.www.ijettjournal.org. published by seventh sense research group.

[6] A. Jackuline Moni and P. Jisha, "High-speed and low-power dynamic latch comparator," 2012 International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, 2012, pp. 259-263.

[7] A. Malathi, R. Greeshma, R. Sanjay and B. Venkataramani, "A 4-bit medium speed flash ADC using inverter based comparator in 0.18µm CMOS," 2015 19th International Symposium on VLSI Design and Test, Ahmedabad, 2015, pp.1-5.

[8] N. Agrawal and R. Paily, "A threshold inverter quantization based folding and interpolation ADC in 0.18 _m CMOS", Springer J. of Analog Integr. Circ. Sig. Process, vol. 63, no. 4, pp. 273-281, Sep. 2009.

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