Design of Sample and Hold Circuit with Improved Charge Leakage and Linearity for Low Power Applications

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***Abstract*—This paper presents a novel sample and hold (S/H) circuit for improving charge leakage problem which leads to better linearity. Design of cascaded simple switch is a vital attribute in the proposed circuit. In this work, various sample and hold circuits are simulated using LTSPICE XVII, in 180nm TSMC technology and their performances are examined. The results show that the proposed design is a better choice for front end design of biomedical or sensor applications. From the simulation results, it is observed that the proposed cascaded S/H circuit with boosted driver consumes 2.02 nW of power at 1 V supply voltage. In addition, Signal-to-noise plus distortion ratio (SNDR) of 87.288 dB is achieved for 200 Hz input signal with 250 KS/s sampling rate.**

***Index Terms*—sample and hold circuit , cascaded switch, bootstrap circuit, linearity, charge leakage**

I. Introduction

Sample and hold circuit is the critical part of analog-to- digital converter (ADC) in biomedical applications [1]. Sampling with high linearity, reduced charge leakage and low power consumption at lower supply voltage is a crucial job. In modern CMOS circuits, the maximum allowable supply voltage, V_{DDmax} decreases continuously in low power applications. However, the threshold voltage V_{TH} of the devices is not scaled proportionally. The high value of V_{TH}/V_{DDmax} is usually acceptable in digital world, however, in case of analog circuits, it eventually results in the reduction of signal swing [2].

The aim of this work is to design a sample and hold circuit for low-frequency signals such as ECG, EMG, EEG etc. These signals have frequencies ranging from a few Hz to 10 KHz. The main features of these signals are low amplitude and low frequency. However, these low-frequency signals cause several challenges. Power dissipation is the most significant problem in an analog to digital converter. This can be solved by reducing the supply voltage. By choosing the advanced technology nodes, the power dissipation problem can be resolved.

For low power applications, the threshold voltage of MOS switch is larger than the supply voltage. Charge leakage and poor linearity are also identified as the issues limiting the design of efficient S/H circuits. The linearity and speed of S/H circuits depends on ON resistance of the switching device. The ON resistance of an NMOS sampling switch is given by,

$$R_{ON} = \frac{1}{\mu_n C_{OX} (V_{GS} - V_{TH}) \frac{W}{L}} \tag{1}$$

Where

$$V_{GS} = V_{DD} - V_{in} \tag{2}$$

Substitute equation (2) in equation (1) gives,

$$R_{ON} = \frac{1}{\mu_n C_{OX} (V_{DD} - V_{in} - V_{TH}) \frac{W}{L}} \tag{3}$$

In equation (3), R_{ON} depends on input voltage, V_{in}. Any change of input voltage makes changes in R_{ON}, that leads to nonlinearity [3]. In this case, sampling is not done properly due to charge leakage when the switch is in the OFF condition. Thus, it adversely affects the linearity of the signal. To overcome these constraints, an adaptive analog circuit approach, which avoids increased circuit complexity and increased cost, is required by the designer. By connecting the bootstrap switch to a clock booster, nonlinearity is reduced [4]. There are different available methods for sampling, but they have limited bandwidth and output voltage swings, which also affect accuracy and power consumption.

The bootstrapped sampler is an essential component of analog-to-digital converters (ADCs). With bootstrapping, distortion is minimized and speed is improved without sacrificing power. Several sources of distortion exist in metal oxide semiconductor (MOS) sampling switches. Their ON-resistance and channel charge vary depending on the gate to source voltage, V_{GS}, and thus

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with the analog input level. In order to minimize these effects, it is essential to maintain V_{GS} constant during sampling. This can be achieved by attaching a battery to the gate and the source terminals. As the gate voltage varies in accordance with the source voltage, it is said to be 'bootstrapped'.

The paper is organised as follows. The first section introduces the problems of conventional sample and hold circuits. The second section describes the different types of S/H circuits and their limitations. The third section describes the proposed S/H circuit with boosted driver and cascaded simple switch. The fourth section analyses the performance of the proposed S/H circuit. The last section concludes the work.

II. EXISTING APPROACHES FOR S/H CIRCUIT DESIGNS

An overview on various S/H circuits used in the design of ADCs is presented in the following section.

A. Simple NMOS switch design

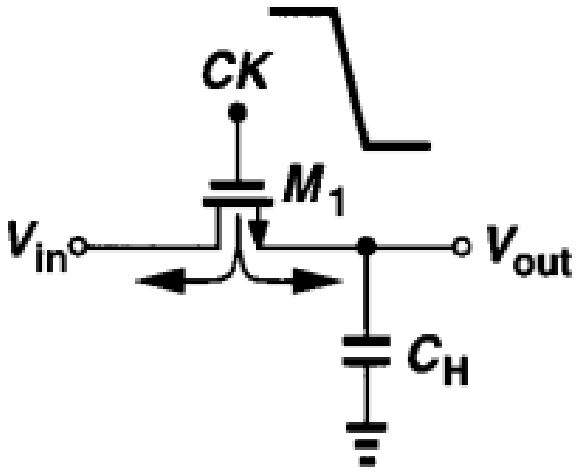

Fig. 1. Channel Charge injection [6]

Fig. 1. depicts the circuit of a simple NMOS switch. The NMOS switch is controlled by clock. When CK is high, the switch is closed, then the input, V_{in} appears across the capacitor. When the gate voltage is sufficiently high, the transistor behaves as a closed switch and the output tracks the input, which is called tracking or sampling phase. When the gate voltage is too low, the transistor behaves as an open switch. It is assumed that, all the voltage levels of the circuit are between 0 and V_{DD}. The equivalent ON resistance is given in equation (1). In this equation, $V_{GS} - V_{TH}$ is not a constant as it is a function of input and substrate body voltage, V_{SB}. If V_{in} becomes greater than $V_{DD} - V_{TH}$, M_1 will not turn ON and it restricts the amplitude of the output signal. Here, the resistance of the switch is very low. If the resistance of the switch increases, the bandwidth of the signal falls. In order to fix this issue, an NMOS with larger W/L ratio can be used, which will reduce the ON resistance [5].

Another problem which limits the operation of a S/H circuit is charge injection, when the switch is turned OFF. Charges are present at the oxide-silicon interface when the switch is in ON condition. The total charge in the inversion layer of a MOSFET is given as

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}) \tag{4}$$

where L is effective channel length and W is the channel width. When the switch is getting turned off, the channel charges get injected to the right and left side as shown in Fig. 1. The charges injected to the source side get absorbed and no error is created in circuit operation. However, in drain side, the charge is dumped on sampling capacitor, C_H which introduces inaccuracy in the voltage across the capacitor [6].

B. Pass transistor switch design

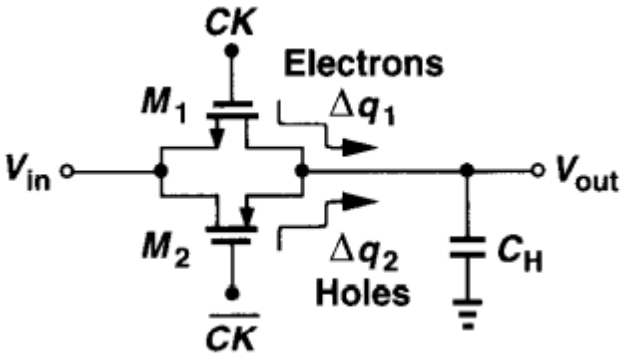

Fig. 2. Pass transistor switch [6]

The schematic of a pass transistor switch is shown in Fig. 2. To reduce the effect of charge injection, PMOS and NMOS devices are integrated, such that the opposite charges injected into the capacitor C_H cancel each other. The cancellation occurs only for one input level. However, in clock feedthrough, where MOS switch combines the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance introduces an error. The circuit does not offer whole cancellation of charge since, the overlap capacitance of NMOS is not identical to that of PMOS.

C. Cascading pass transistor sample and hold circuit

Fig. 3. illustrates a cascaded pass transistor switch-based S/H circuit. The cascaded structure is used to overcome the subthreshold leakage problem when the switch is in OFF condition [7]. The OFF-state leakage current rises exponentially with diminishing threshold voltage. This OFF current mostly takes place during

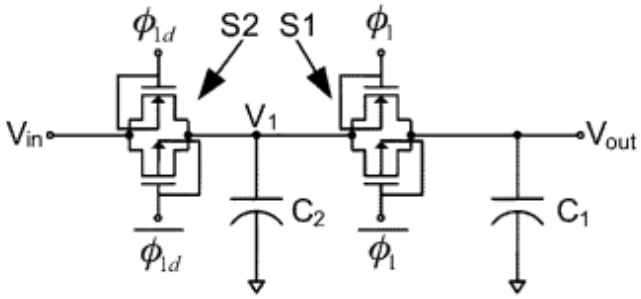

Fig. 3. Cascading pass transistor switch design [7]

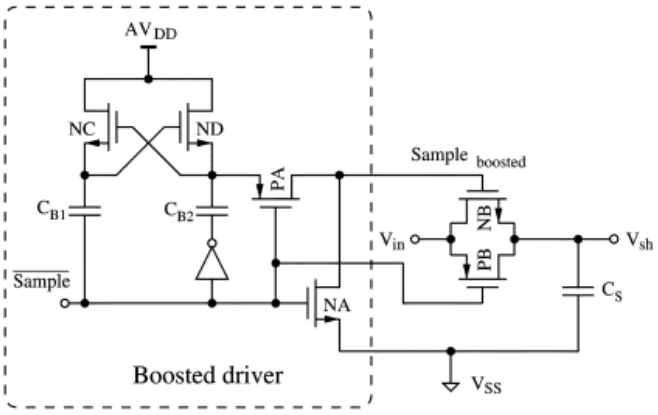

Fig. 4. Schematic of track and hold with boosted driver [8]

sampling and holding phase, when the capacitor is not associated with any voltage source. This makes the output voltage discontinuous when switch is OFF.

This technique includes an additional simple NMOS switch and a smaller holding capacitor, C_2 before the main NMOS switch and the hold capacitor, C_1, as depicted in Fig. 3. Both switches operate in same clock phase, but falling times are different. Both switches are ON during the track phase and both are OFF in the hold phase. In track phase the V_{out} follows V_{in}. In the hold phase, the switch, S_1 enters weak inversion and the voltage difference between V_{out} and V_1 is very small. As the switch, S_1 is in linear region, it is having a very low drain-source voltage V_{ds,S_1}. The channel leakage current of each of the transistors in hold phase is given by

$$I\alpha\frac{W}{L}exp\left(\frac{-V_{TH}}{\frac{nKT}{q}}\right)\left[1-exp\left(\frac{-V_{ds,S1}}{\frac{KT}{q}}\right)\right]\approx 0 \qquad (5)$$

Since the switches are cascaded in series, the overall size of the circuit gets increased. Hence, the added holding capacitor, C_2 was set to ¼ C_1 to restrict the size of the circuit and to settle the constraints on time constant. To diminish the threshold voltage of switch and progress the settling throughout the ON state, the switch-transistor gate and body terminals are shorted and it is attached to the clock signal. To improve the signal distortion and reduce power consumption, a clock booster circuit can be cascaded with simple switch for low power applications.

D. Clock booster circuit operation

Fig. 4. depicts the schematic of a track and hold circuit with boosted driver for attaining both low power and a wide band width, which produces a periodical output [8]. This circuit consist of a sampling capacitor, C_S and simple NMOS and PMOS switches as shown in Fig. 4. The power of the boosted switch is ignored, since the driver operates at $1/9^{th}$ the clock frequency. This technique ensures low ON resistance; it has a bandwidth $1/(2\pi R_{ON}C_S)$, where R_{ON} is the ON-resistance of the boosted switch.

III. PROPOSED S/H CIRCUIT WITH BOOSTED DRIVER AND CASCADED SWITCHES

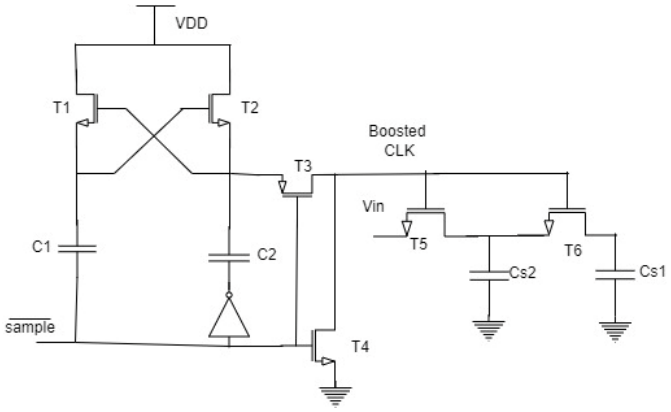

Fig. 5. Proposed S/H circuit with cascaded simple switches and boosted driver

The major drawback of a transmission gate-based S/H circuits design is the subthreshold leakage current when switch is OFF and the fluctuations in the output voltage. The reason behind the leakage is ON resistance between source and drain terminals. It is related to the input clock signal. By boosting the clock signal, ON resistance can be reduced. The circuit for boosting the clock signal is called boosted driver. The schematic diagram of sample and hold circuit with boosted driver circuit followed by a transmission gate is depicted in Fig. 4. The schematic includes a driver circuit and a sample switch and the output of the driver circuit is linked to the gate of the NMOS transistor NB in the transmission gate circuit. The boosted voltage is found to be between $2V_{DD}-\Delta V$ and ground. It is coming at the output due to charge sharing between the PA and the parasitic capacitance at the output node [9]. The boosted voltage can be calculated

as per equation (6).

$$V_{boosted} = 2V_{DD}\left(\frac{C_{B2}}{C_{gateNMOS} + C_{B2} + C_{parasitic}}\right) \quad (6)$$

A. Proposed cascading simple switch with boosted driver

ADC front-end circuits require uniform conductance. It is necessary to use bootstrap circuits in order to accomplish this requirement. Based on a variable input signal, the bootstrap circuit generates a linearly varying output voltage. Clock signals are generally used to drive bootstrap circuits. Here, a sample signal can range from 0 to V_{DD} when applied to the capacitors C_1 and C_2, which are the boosted capacitors. An inverter is used before the capacitor C_2. With the boosted driver, the low power and wide bandwidth can be achieved by cascading two simple nMOS transistors.

Initially, assume that both the capacitors, C_1 and C_2, are uncharged. When the sample bar signal is low, the approximate output voltage of the inverter is V_{DD}. Then the voltage at the top plate of the left capacitor C_1 is '0' and the top plate of the right capacitor C_2 will be V_{DD}. Consider the transistor T_1. The gate is at V_{DD} and the drain is at V_{DD}. The source potential of this transistor is $V_{DD} - V_{TH}$. When the state of the sample bar signal has changed to high, which means the absolute voltage has gone to V_{DD}, the absolute voltage of the inverter and the top plate of the capacitor C_1 changes to V_{DD} and $2V_{DD} - V_{TH}$, respectively. This $2V_{DD} - V_{TH}$ appears at the gate of the transistor T_2. The drain is at a voltage of V_{DD}, and the source voltage rises towards V_{DD}. Hence, the capacitor charges towards V_{DD}. In the next phase, the gate of the transistor T_1 is set to $2V_{DD}$ and the drain is at V_{DD}. The potential at the source of transistor T_1 is V_{DD}. Within a couple of cycles, both the capacitors C_1 and C_2 are charged to $2V_{DD}$.

The schematic of proposed S/H circuit with cascaded simple switch design and boosted driver is shown in Fig. 5. The cascaded transistors T_5 and T_6 acts as the sample switch. The boosted voltage available at T_3 steers the cascaded switch and also removes the low supply voltage restrictions. It also enables the rail-to-rail input signal through the two simple NMOS switches. This circuit consumes less power compared to cascaded transmission gate which is shown in Fig. 3. All transistors are sized as 12µm/0.36µm, and value of capacitors are C_{S1} = 200 pF, C_{S2} =50 pF, C_1 = C_2 = 5 pF. Since, the capacitor values of C_{S1} and C_{S2} are different, the charging and discharging time constants are also different. It leads to stable output and ensures constant sampling which makes high linearity and reduced leakage reduction.

IV. RESULT ANALYSIS

The S/H circuits discussed in section II and III were analysed in 180 nm CMOS technology using LT-SPICE XVII. An input signal of frequency 200 Hz and $250mV_{P-P}$ amplitude is applied to these circuits. A supply voltage of 1 V is applied, as depicted in Fig. 7. The sampled signal is analyzed with and without clock booster circuit. A train of pulses with 0.5 V amplitude and 2 KHz frequency is used as the clock signal, and is shown in Fig. 7. The output waveforms are shown in Fig. 9. and Fig. 10. respectively. The rail-to-rail sampling is not achieved under 1 V power supply and clock pulses with 0.5 V amplitude [10]. Due to these reasons, the amplitude of sampled signal is severely distorted when small supply voltage (less than 1.2 V) and the clock signal is used.

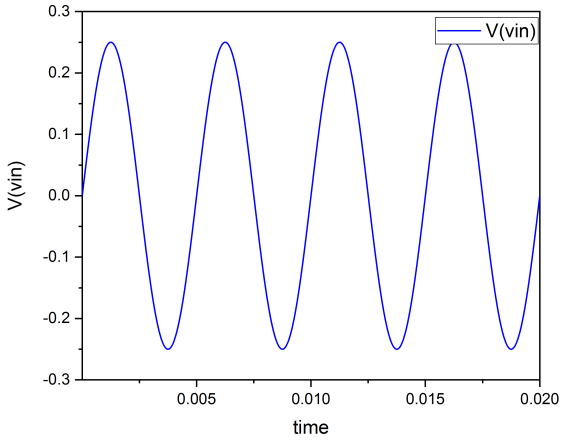

Fig. 6. Input signal with frequency 200 Hz

The boosted clock signal is depicted in Fig. 8. which was simulated under V_{DD} of 1 V. Here, the same clock signal is used as input of boosted driver. Fig. 8. shows that, the boosted driver attains rail-to-rail sampling of the signal and it boosts the clock signal to $2V_{DD}$. Boosted clock signal and the sampled output signal are shown in Fig. 9. Fig. 10. shows the input and sampled output signal. Simulation results show that the linearity has been improved and charge leakage has got reduced.

The power utilization of the different switching designs was estimated, and is enumerated in Table I. The table displays the average power consumption in nW and SNDR in dB. The cascaded simple NMOS switch with boosted driver dissipates lesser power compared to cascaded transmission gate with boosted driver. The simulation results show that use of clock boosting circuit not only decreases the sampling distortion reduces power utilization.

The proposed cascaded simple NMOS switch with boosted driver exhibits an SNDR of 87.288 dB. It is greater than the SNDR corresponding to the conventional S/H circuits. The FFT spectrum of the sampled signal of the proposed circuit is shown in Fig. 11.

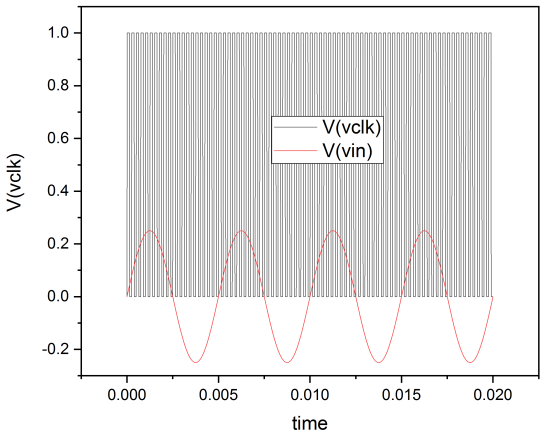

Fig. 7. Sample clock signal and input signal

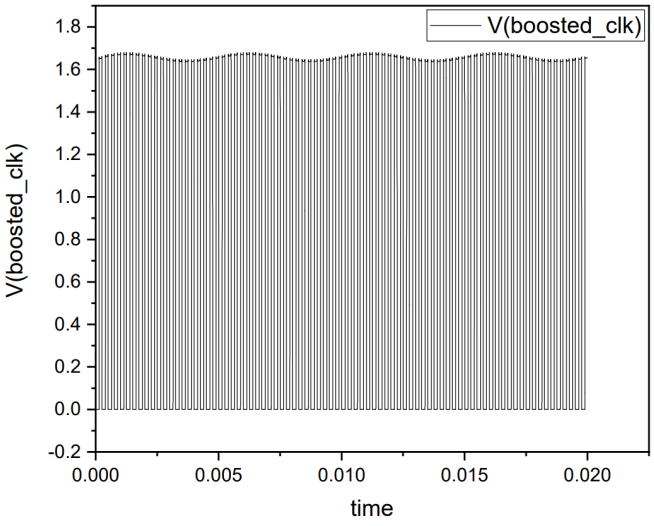

Fig. 8. Boosted clock signal

The switching design circuits used for low frequency signals were realized in 90nm CMOS technology in literature [5]. In this work, the power consumption of the sample and hold circuit with boosted driver is 1.09 nW [5]. Here a minor difference in average power is attained with 180 nm design. The cause of this discrepancy is the increased total power dissipation found in advanced technology nodes. However, the advanced technology nodes result in reduced dynamic power consumption.

The average power consumed by sample and hold circuits were analyzed with and without clock boosting circuits. The proposed cascaded sampling switch (two transistors) with booster driver attains 2.02 nW power . This displays a 0.383 nW reduction in power compared with the cascaded transmission gate with booster circuit. The cascaded transmission gate switch design consumes

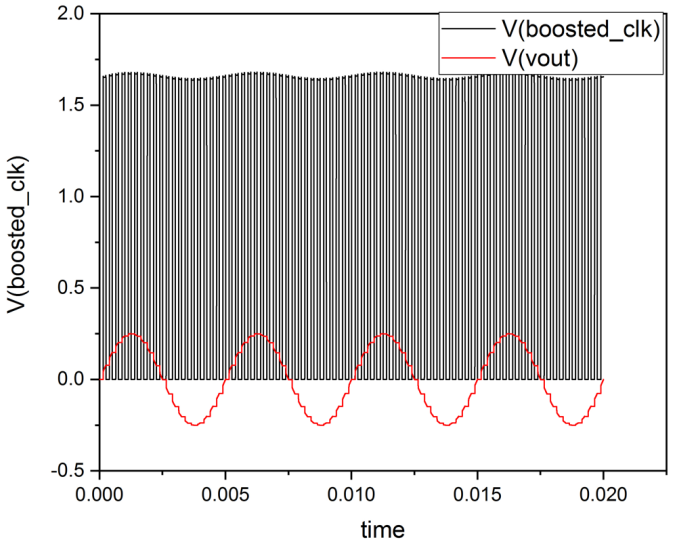

Fig. 9. Boosted clock signal and sampled output signal

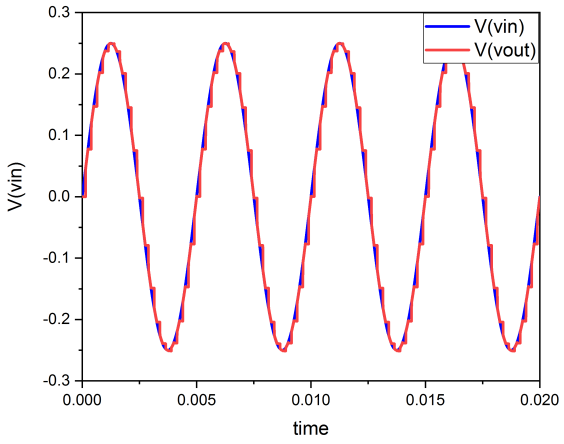

Fig. 10. Input and sampled output signal

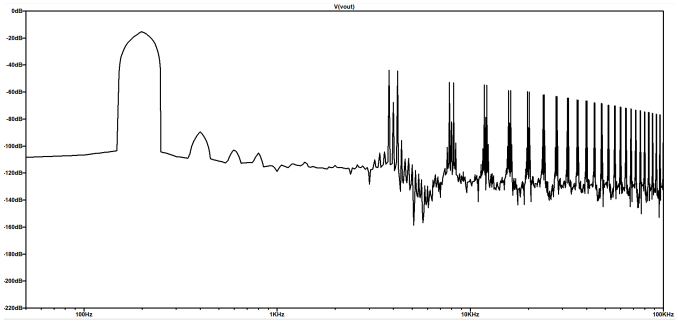

Fig. 11. FFT spectrum of sampled output signal

an average power of 2.403 nW, which is greater than the other designs reported in the preceding literature.

TABLE I
DIFFERENT TYPES OF SWITCHING DESIGN CIRCUITS

Sl. No.	Sample and Hold circuits	Average Power consumption (nW)	SNDR (dB)
1	Simple NMOS Switch	1.96	33.588
2	Transmission gate switch	2.008	33.038
3	Cascading transmission gate switch	2.01	45.01
4	Cascading transmission gate with boosted driver	2.403	54.65
5	Proposed cascading simple NMOS switch with boosted driver	2.02	87.288

V. CONCLUSION

To improve subthreshold leakage and linearity of S/H circuits, a cascaded simple NMOS switch with clock boosting circuit is designed via 180 nm CMOS technology in LTSPICE XVII, the rail-to-rail input voltage sampling can be attained in such a design. Different switching circuits were simulated, and the proposed cascaded simple switch design is found to be more power efficient and immune to noise for sampling biomedical signals. This proposed work can be a part of efficient analog to digital converters for biomedical implantable systems.

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