Report

on

Design of 8-Bit Clock-less Pipelined ADC

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CONTENTS

Chapter 1: Introduction

Clocked analog to digital converters have dominated the computer industry since the 1960s because chip designers saw them as more reliable, capable of higher performance, and easier to design, test, and run than their clock-less counterparts. The clock establishes a timing constraint within which all chip elements must work, and constraints can make design easier by reducing the number of control decisions. In synchronous designs, the data moves on every clock edge, causing voltage spikes thereby causing high power consumption

In clock-less designs, data bits are not all produced at the same time, which spreads out current flow, thereby minimizing the strength and frequency of spikes and emitting less electromagnetic interference (EMI). Less EMI reduces both noise-related errors within circuits and interference with nearby devices. Because asynchronous chips have no clock and each circuit powers up only when used, asynchronous processors use less energy than synchronous chips by providing only the voltage necessary for a particular operation. Thus, clock-less ADCs are gaining relevance in many fields, ranging from astronomy to medicine. Another possible application of clock-less ADC is in wireless net data and web applications components. The new equipment generation for wireless nets imposes a significant change in the converting data circuits. These systems must be low-cost, reduced-size, and especially low-power because they are frequently powered by batteries or remotely powered.

Analog-to-digital converters are usually specified to have a fixed conversion time. In synchronous pipeline ADC designs, worst case delay fixes the time period of the clock. Thus sampling rate of ADC remains fixed irrespective of fact whether operation has completed earlier. But, in clock-less pipeline ADC, next stage is activated by the completion of previous stage. Thus entire pipeline can operate at an average delay, thereby speeding up the overall operation

Chapter 2: Architecture of Pipelined ADC

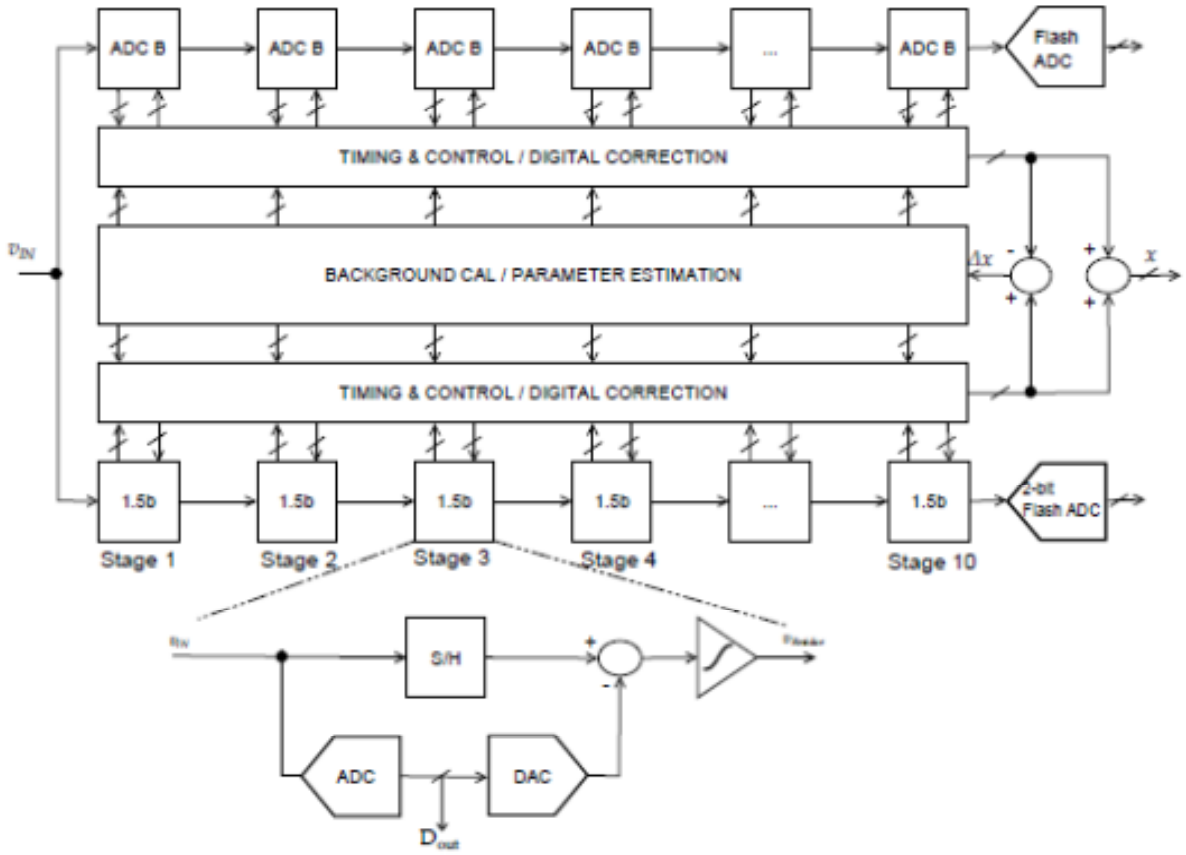


Fig 2.1: Complete pipelined ADC architecture

The output bits of the eight stages are sampled by a register of flip- flops controlled by the end-of-conversion (EoC) signal, which is a delayed version of the start-of-conversion (SoC) signal, and added with a ripple-carry adder (RCA) in order to achieve the final eight output bits with digital error correction. Each 1.5 bit conversion stage consists of a flash ADC with a resolution of 1.5 bits, a DAC, an adder, and a gain stage with a gain equal to 2.

The key requirement of the circuit design is to ensure that the overall ADC data conversion ends within the scheduled time slot. The most critical point to achieve this target is the calculation of the residual error at each 1.5 bit stage for the following stage, which is operated using the results of the previous stage. The overall data conversion time slot is obtained adding the residual calculation time of each of the seven stages of conversion. If it is assumed that each operation is completed within a certain time slot, then the clock can be removed, thus obtaining the proposed structure.

The general functionality of a comparator in a pipeline ADC is two-fold:

1) To take a decision within the available time slot
2) To maintain the output signal for the needed time for the following stage operation.

Possible solution is proposed for the two points.

1) The comparator structure uses only an open-loop amplifier stage, whose output will be used as a digital signal. Such an amplifier has to feature very large gain (much larger than the preamplifier of a clocked comparator) to guarantee a decision even for the minimum signal within the available time slot and to prevent having metastability of the comparator.

2) Since the comparator input signal could, in principle, change during operation (due to noise or disturbances), due to the comparator open-loop operation, the comparator output signal could change with a consequent error in the following stage operation. A proper hysteresis has then been implemented in the comparator. Thus, once a decision is taken, the comparator does not change its output signal.

These two arrangements guarantee the functionality of the overall pipeline-like clock-less ADC.

The only digital signal in the proposed clock-less pipeline like ADC is the SoC that is generated by the experiment trigger. A second control signal is the EoC, which is obtained by delaying the SoC signal through an analog block, consists of an RC network followed by a comparator same as that used in the main ADC. The value of delay is equal to and has been chosen in order to match the delay of the pipeline chain. This signal is used to strobe the digital output of each stage and to control the digital correction section.

The MDAC subtracts the voltage generated by the DAC from the input signal, generating the residual voltage, which is amplified by two, and represents the input signal of the next stage. Also, in this stage, the use of a non-clocked structure results in novel implementation solutions. The adder and the gain stage can be realized with an operational amplifier in closed-loop configuration with two possible solutions. The use of this structure results in the additional requirement for the operational amplifier to feature the same input and output common-mode voltage.

The 1(7*1.5+2)1 bits provided by the eight conversion stages are sampled by an array of flip-flops driven by the EoC signal.

It useful to point out that the proposed structure could have a potential issue of error propagation due to the fact that the comparator could decide far before the input signal is fully settled

(e.g., because of the ripple of the signal during its settling). This could happen because, the comparator structure is continuous-time and hence it can switch at any time. The conversion process with cascaded stages results in a limit of the sampling frequency that is times lower than a clocked pipeline A/D converter.

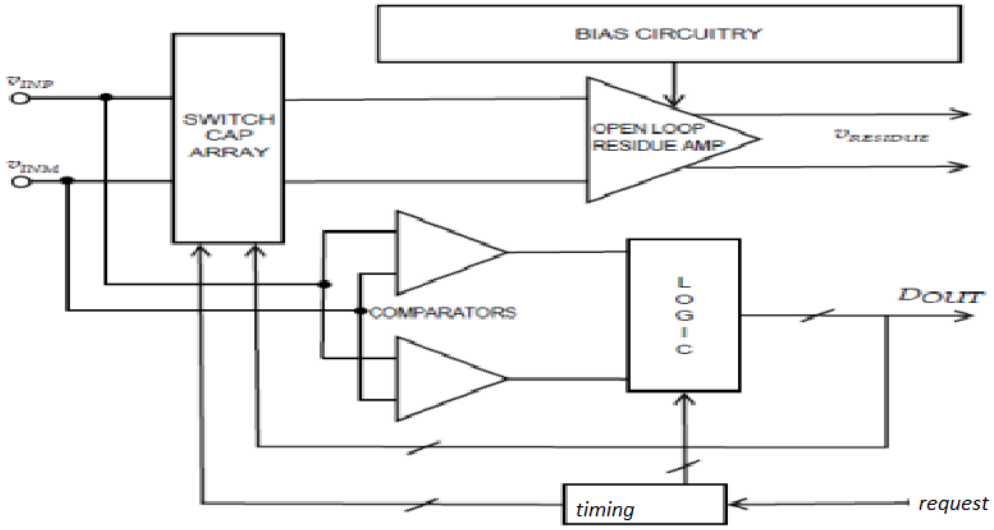


Fig 2.2: Single stage of pipelined ADC (includes both analog and digital blocks), where timing is controlled by request signal.

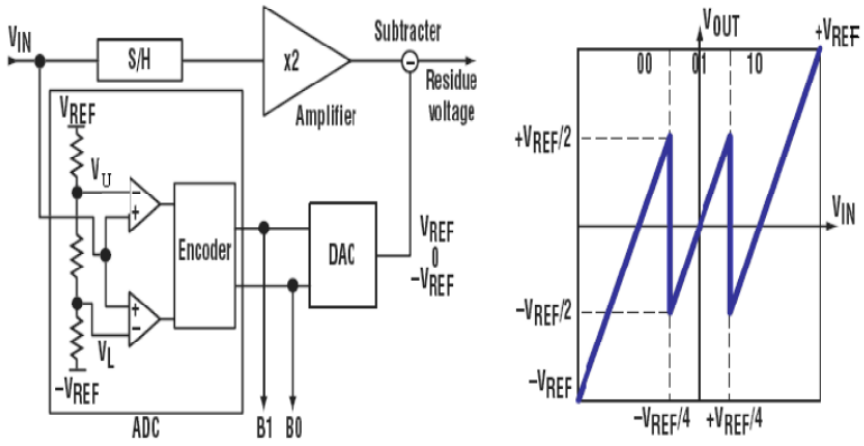


Fig 2.3: Single stage of pipelined ADC. Here reference signals vu = +vref/4 and vl = -vref/4

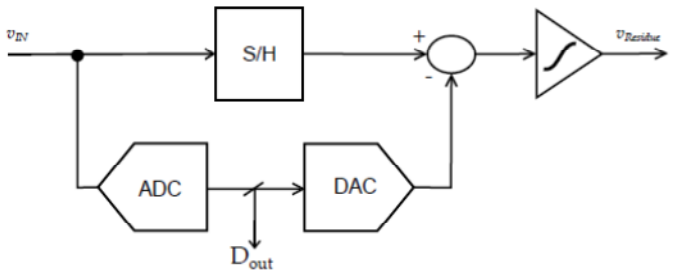


Fig 2.4: Basic block of pipelined where sample and hold, subtraction and amplification were done by opamp and switched capacitors as shown below

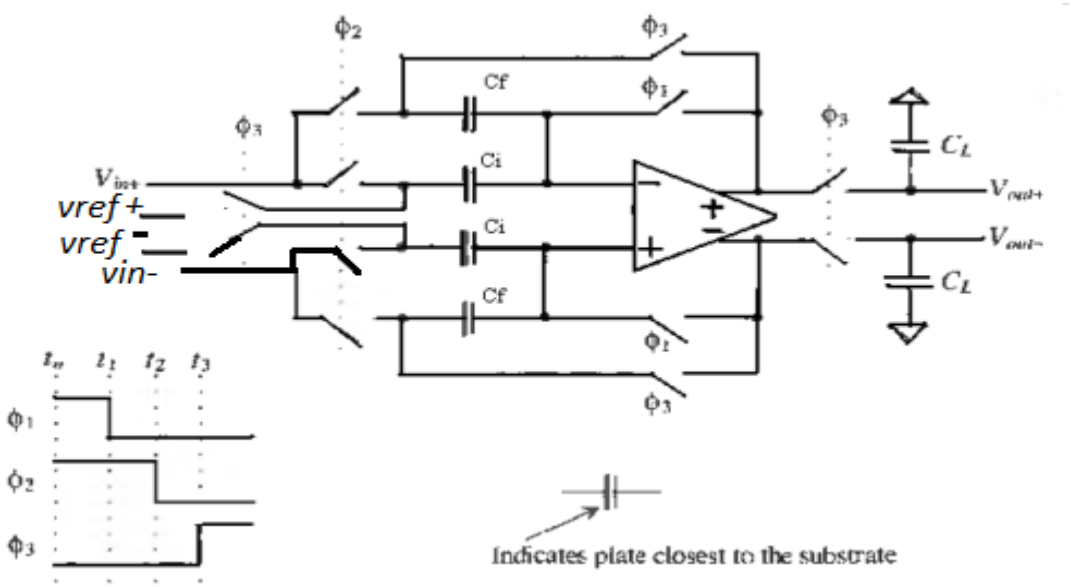


Fig 2.5: Switched capacitor implementation of S/H, subtraction and amplification

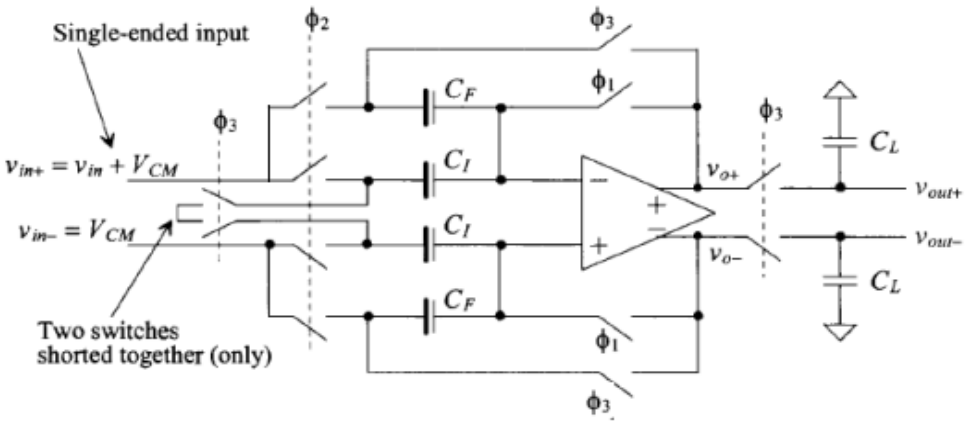


Fig 2.6: Input stage of pipelined ADC, this block converts single ended input to differential input

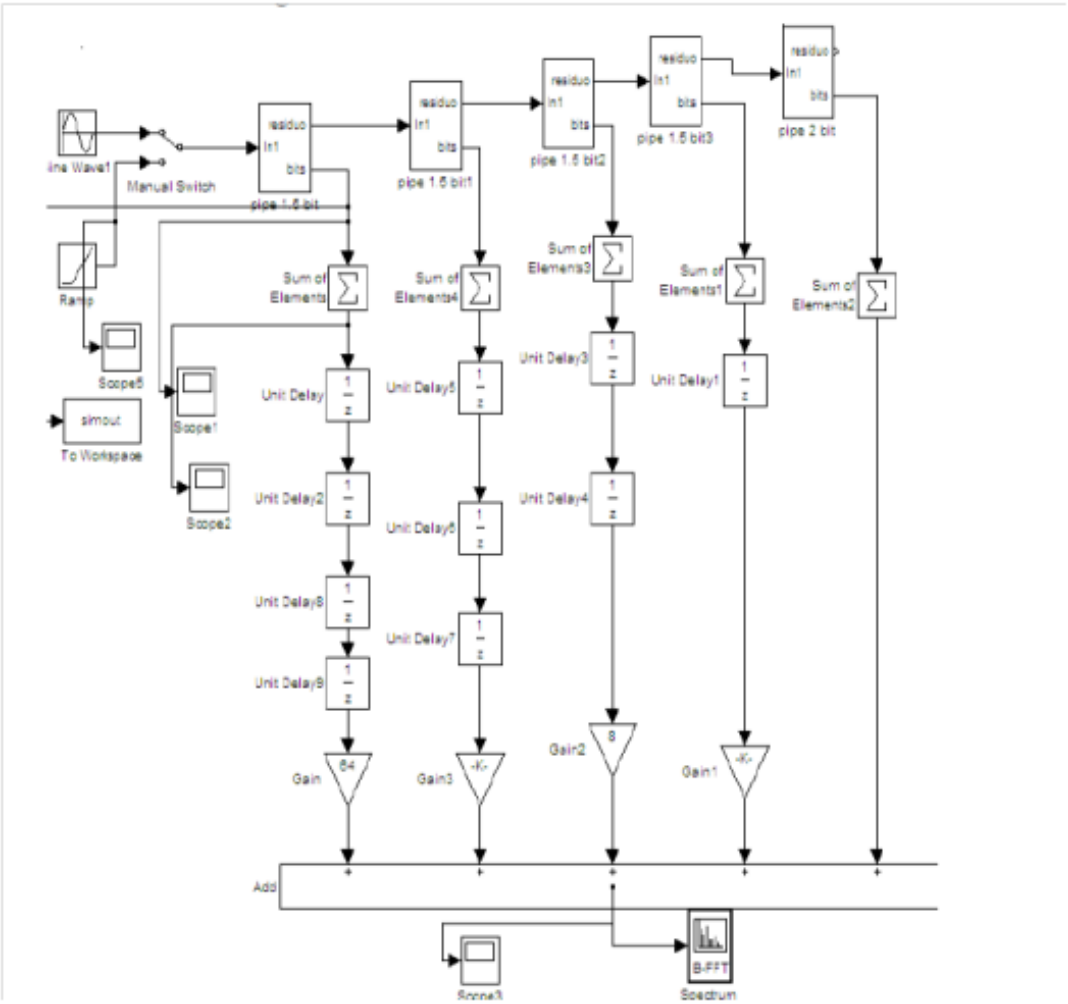


Fig 2.7: Array of D latches in order to get output bits of a sample at the same time

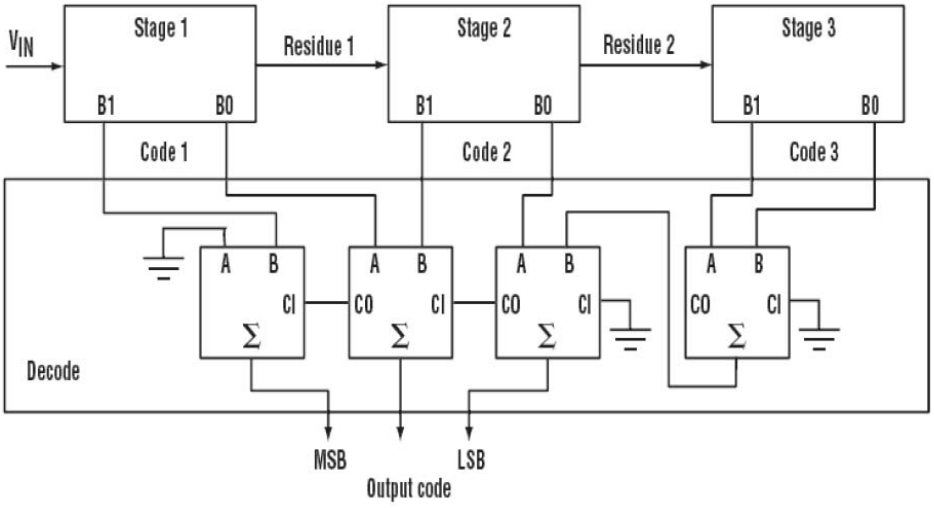


Fig 2.8: Digital error correction circuitry

Chapter 3: Block Level Design

1) Comparator Design:

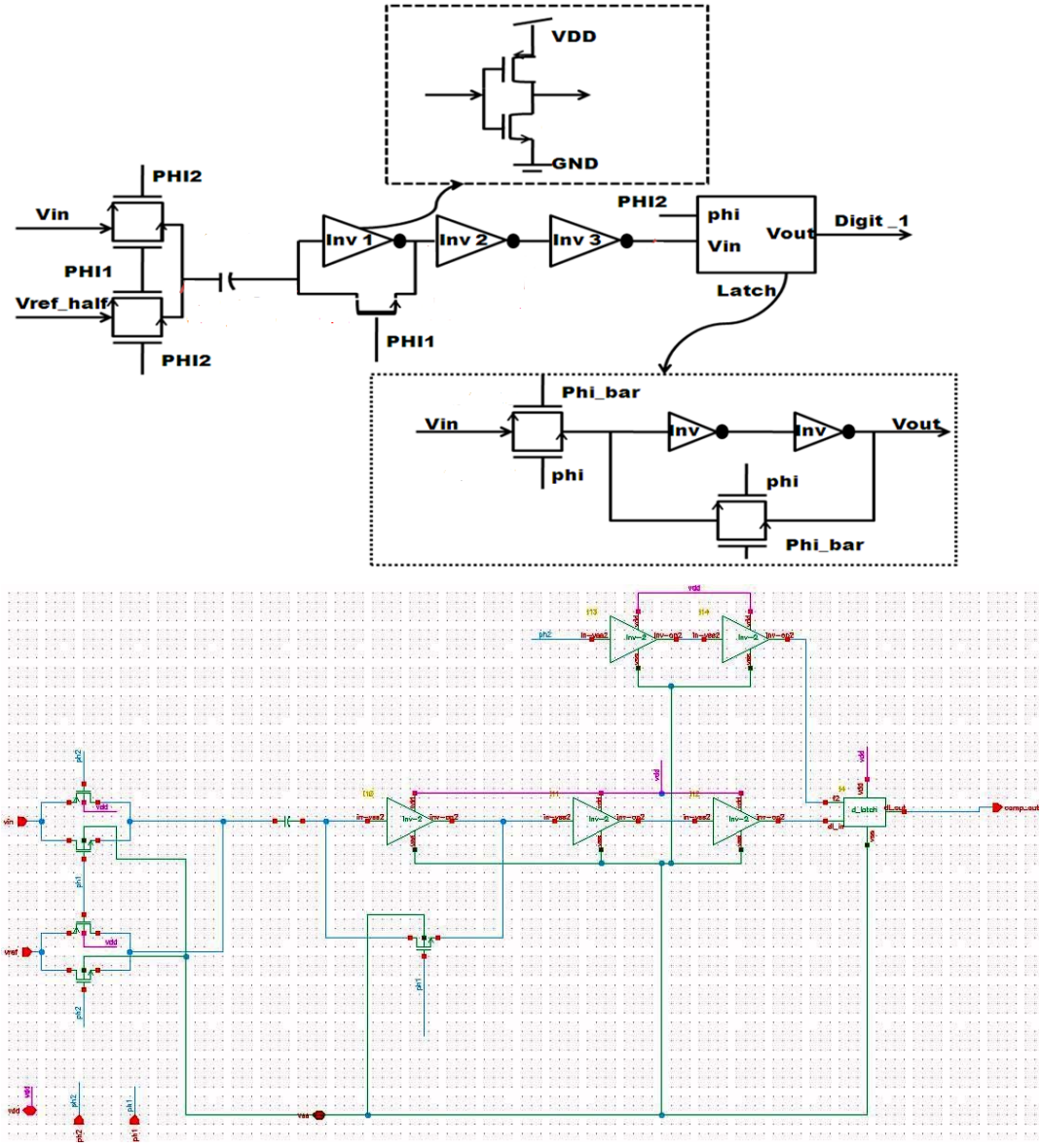


Fig 3.1: Comparator design

OPERATION:

1) During phi1, positive plate of capacitor would be charged to vin and negative plate of the capacitor would be charged to vdd-vss/2 since its input and output are shorted.

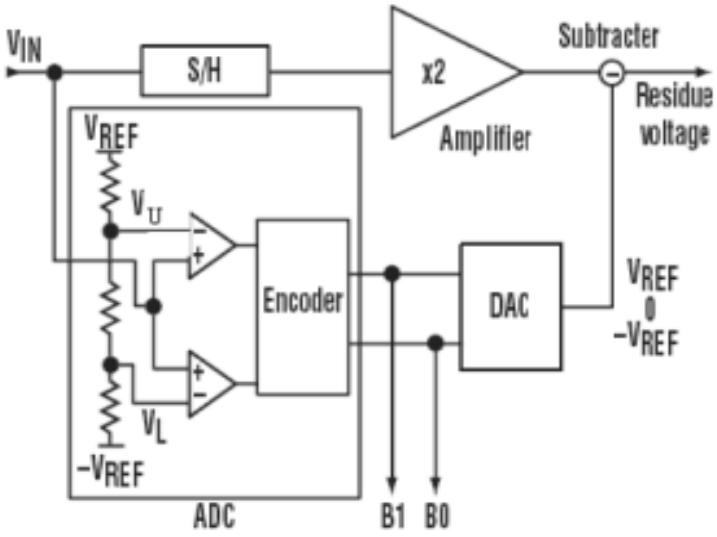
2) During phi2, positive plate of capacitor would be charged to vref and negative plate of the capacitor would retain its charge as it is.

Difference in charge across capacitor is C(Vref-Vin) would transfer to capacitor (Cgs) at inverter1 input. Depending on voltage corresponding to C(Vin-Vref), output of inverter1 may

go to vdd or it may go to vss in phase, phi2 . Since, this is followed by two more inverter, so output will be 1(vdd) else 0(vss) depending on if V= [C(vin-Vref)/ Cgs] > 0 (VIL)

3) Output of comparator is given to d-latch which passes output bit in phase phi2 to encoder and holds output bit during phi2bar

2) ADC Design:



Operation:

B1 and B0 are MSB and LSB respectively. Thermometer code (A1 and A0) which is obtained at the output of 2 bit flash ADC is converted to binary code B1 and B0 using an encoder.

Analog input is compared with two reference voltages Vref/4 and –Vref/4

Suppose Vu = Vref/4 and Vl = - Vref/4

If Vin > Vl and vin >Vu output bits (A1A0) = 11

Vin <Vl and vin >Vu output bits (A1A0) = 01

Vin < Vl and Vin <Vu output bits (A1A0) = 00

Using encoder we convert the above thermometer code 00, 01, 11 to 00 , 01 , 10 respective

Here, suppose b0 is LSB and b1 is MSB

B1 = A1; B0 = A1bar. A0

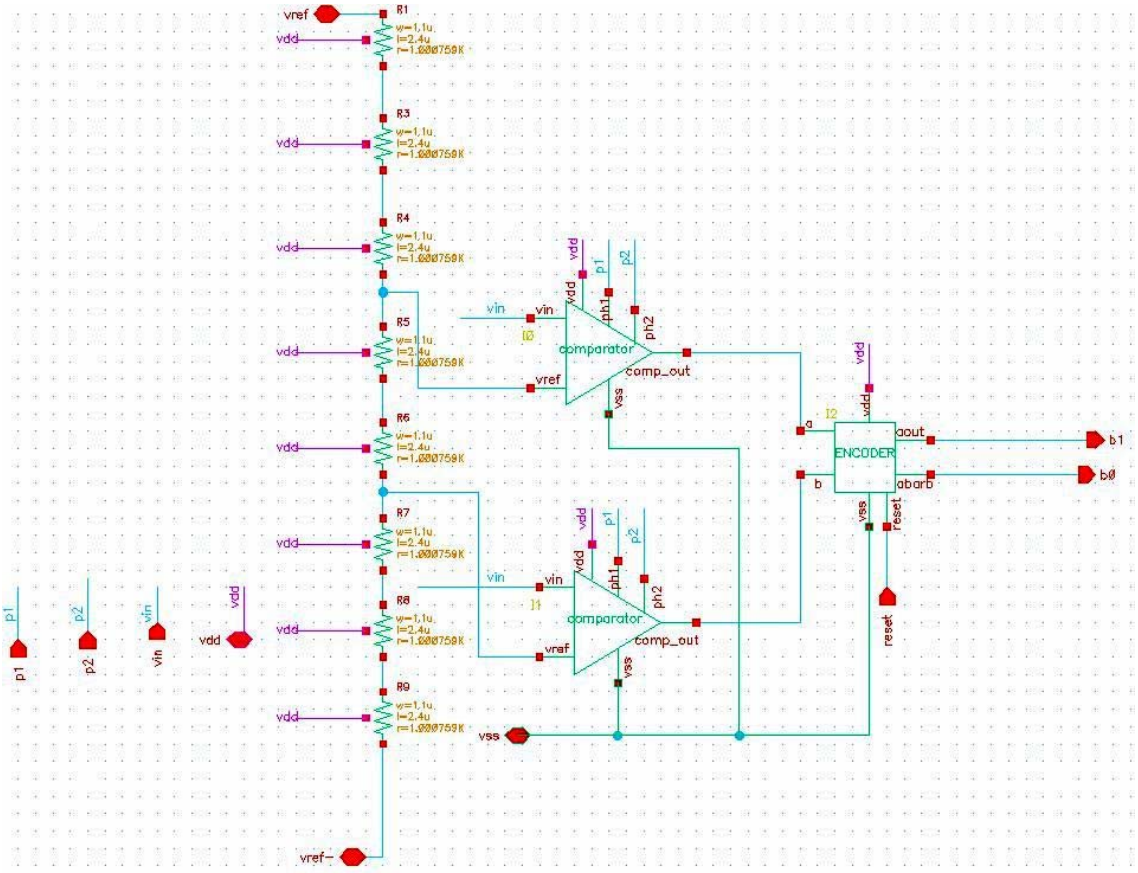


Fig 3.2: ADC Design

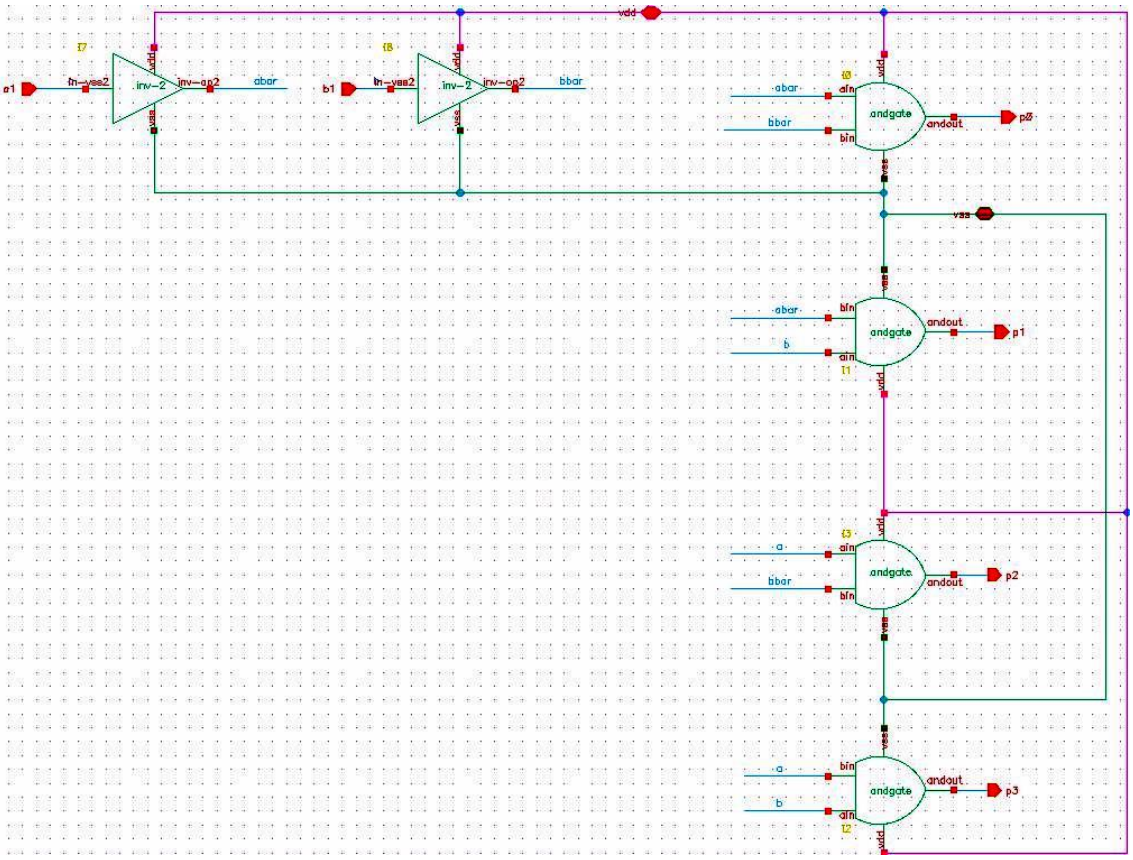


Fig 3.3: Encoder cell design

Here, in digital to analog conversion, digital bits are taken as selection to multiplexer and an analog input is selected as shown below. B1,B0 are selection lines for multiplexer

B1	B0	Output
0	0	-vref
0	1	0
1	0	+vref
1	1	Don’t care

DAC DESIGN

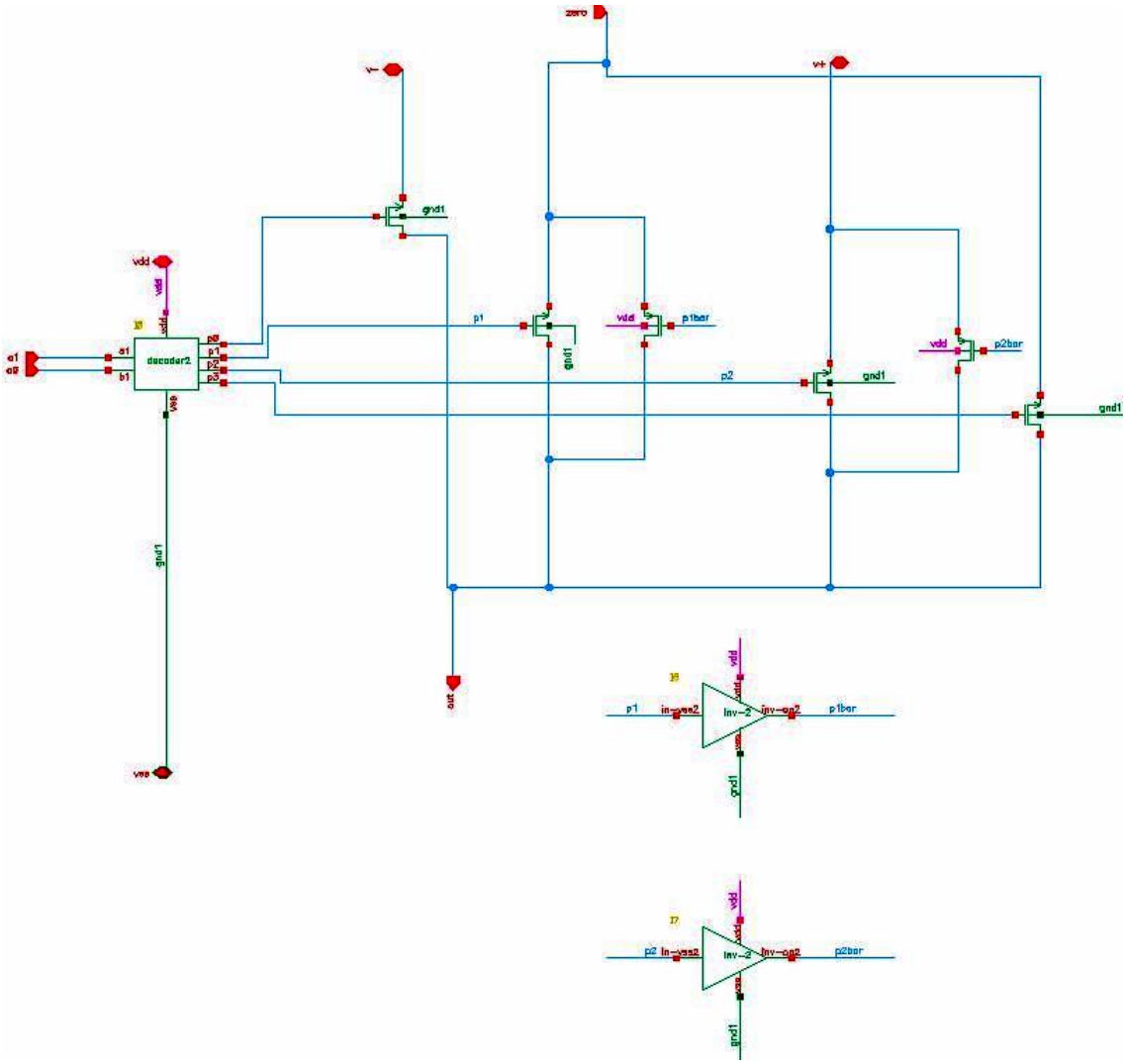


Fig 3.4: DAC cell design

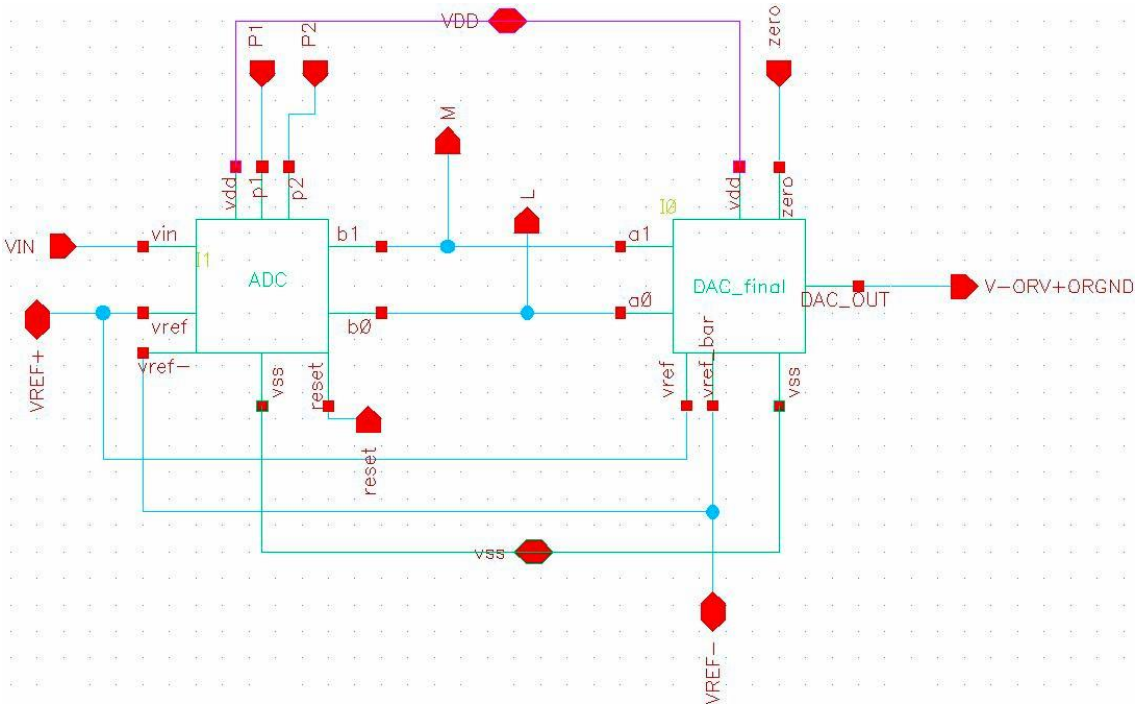
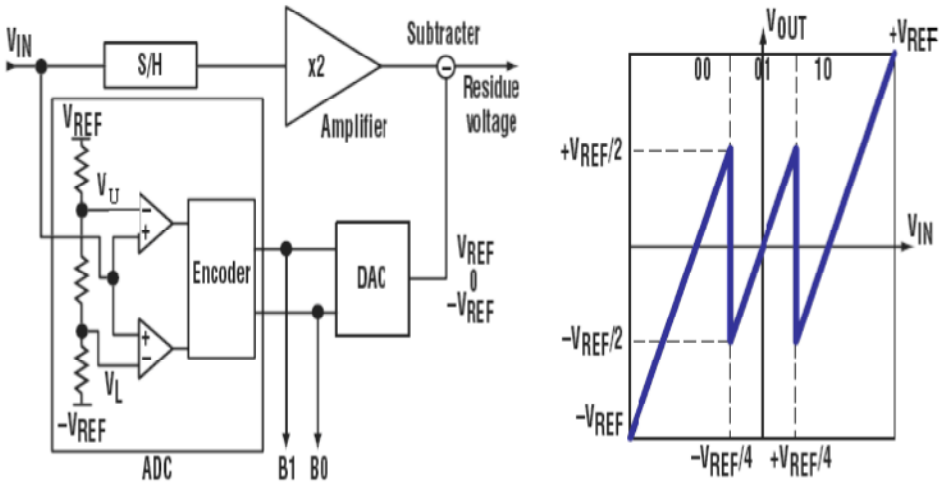


Fig 3.5: Combined DAC and ADC with reference voltage as output

Figure shown above is complete digital architecture which include both ADC and DAC. This output is used for residue calculations

3) Residue Calculation :



Operation:

Figure shown above is the input output characteristic of PADC

Conditions--

Vin < -Vref/4 output residue = 2Vin+ Vref

-Vref/4 < Vin <Vref/4 output residue = 2Vin

Vin > Vref/4 output residue = 2Vin- Vref

Vin	**Range**	**B1**	**B0**	**DAC o/p**	**Analog residue output**
Vin > Vu	UPPER	1	0	Vref	2vin-vref
Vl<Vin<Vu	MIDDLE	0	1	0	2vin
Vin < Vl	LOWER	0	0	-Vref	2vin+vref

Note: Reference voltage should be available to the residue calculator before the input is sampled. But input voltage is given at the same time to both Analog and digital blocks at the same time -

Fully differential opamp design with dynamic common mode feed back

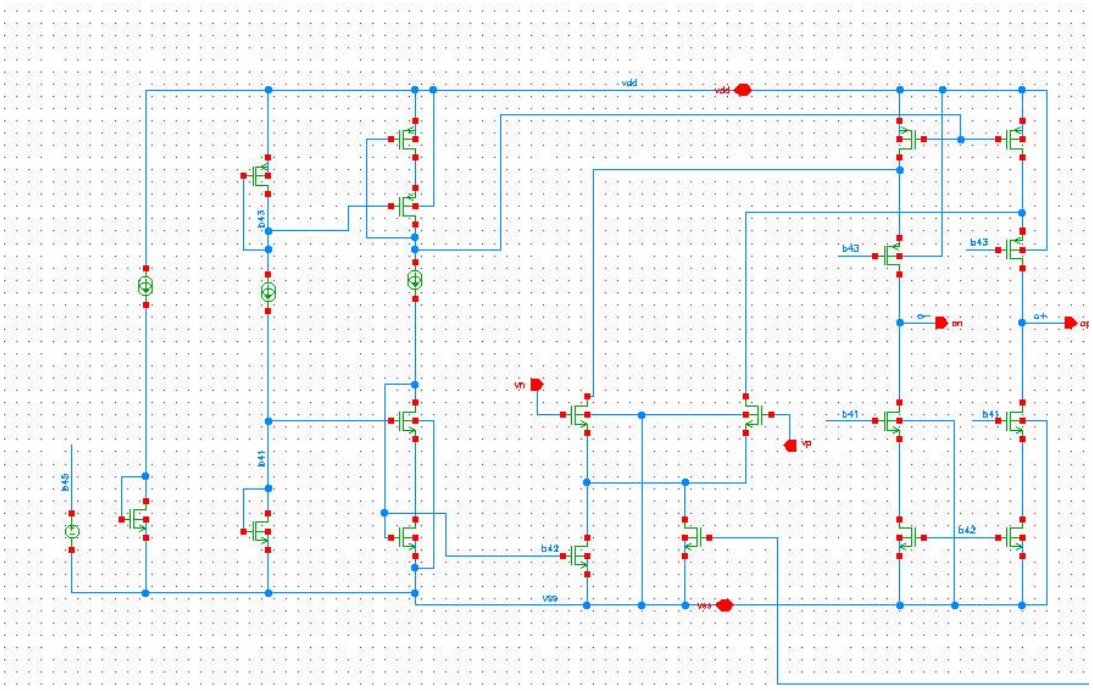


Fig. 3.6 Fully Differential OPAMP Without Common Mode Feedback

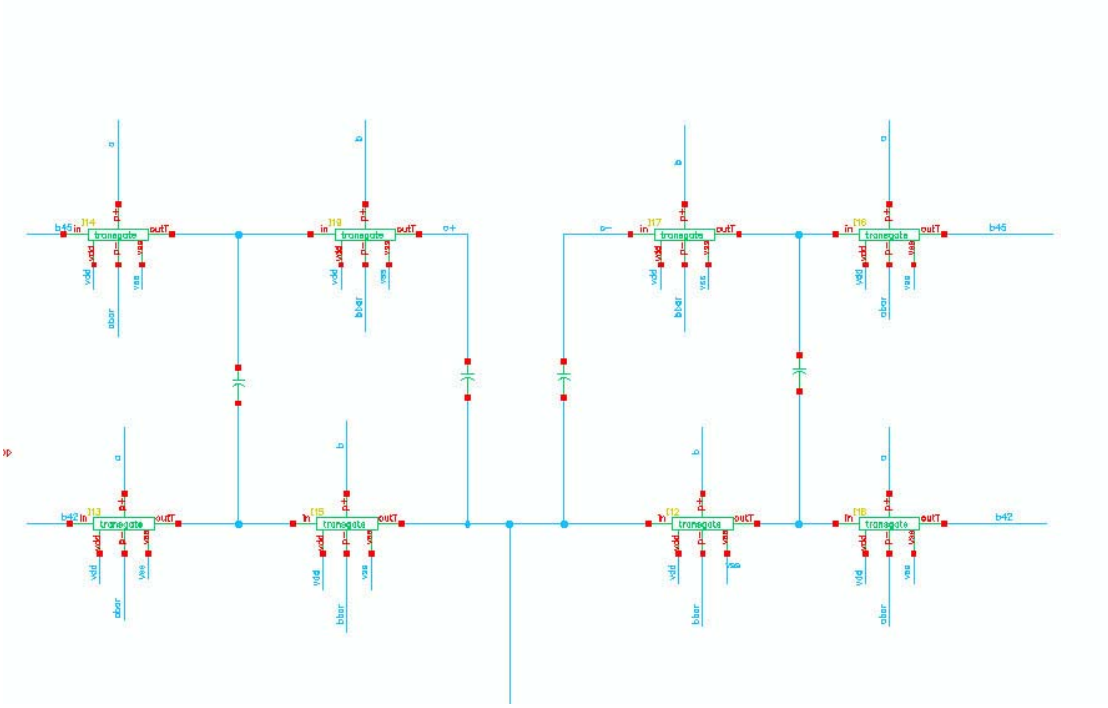


Fig. 3.7 Switched capacitor common mode feed back

Design specifications:

UGB: 100 Mhz ;

Gain: 80dB ;

Load capacitor = 1pf

Calculations:

gm/2*pi*cl = 100Mhz , this gives gm = 614uA/V

b) Gain = 80 dB , this gives gm/id = 2

Assume gm/Id = 8, this gives Id = 80um

Idn (W=1um, L=1um)= 1.538um, So for Id = 80u , we get (w/l)n =52um

Similarly Idp (W=1u,L=1u)= 0.37um, So for Id = 80u, we get (w/l)p =216um

Obtained results:

UGB = 25 MHz and gain = 75db
UGB decreased since We have assumed gm/id = 8 instead of taking 2.

We need to increase UGB. We know UGB = Vov /L^2 .

So we scale L of all NMOS and PMOS to 0.5um

Effects of decreasing L

1. Gain will decrease because ro decreases
2. Vov. decreases
3. UGB may increase approximately by 4 times

Finally obtained results for OPAMP:

UGB = 69 M Hz;

Gain = 65dB;

Phase margin = 72 degree

Settling time = 30nsec

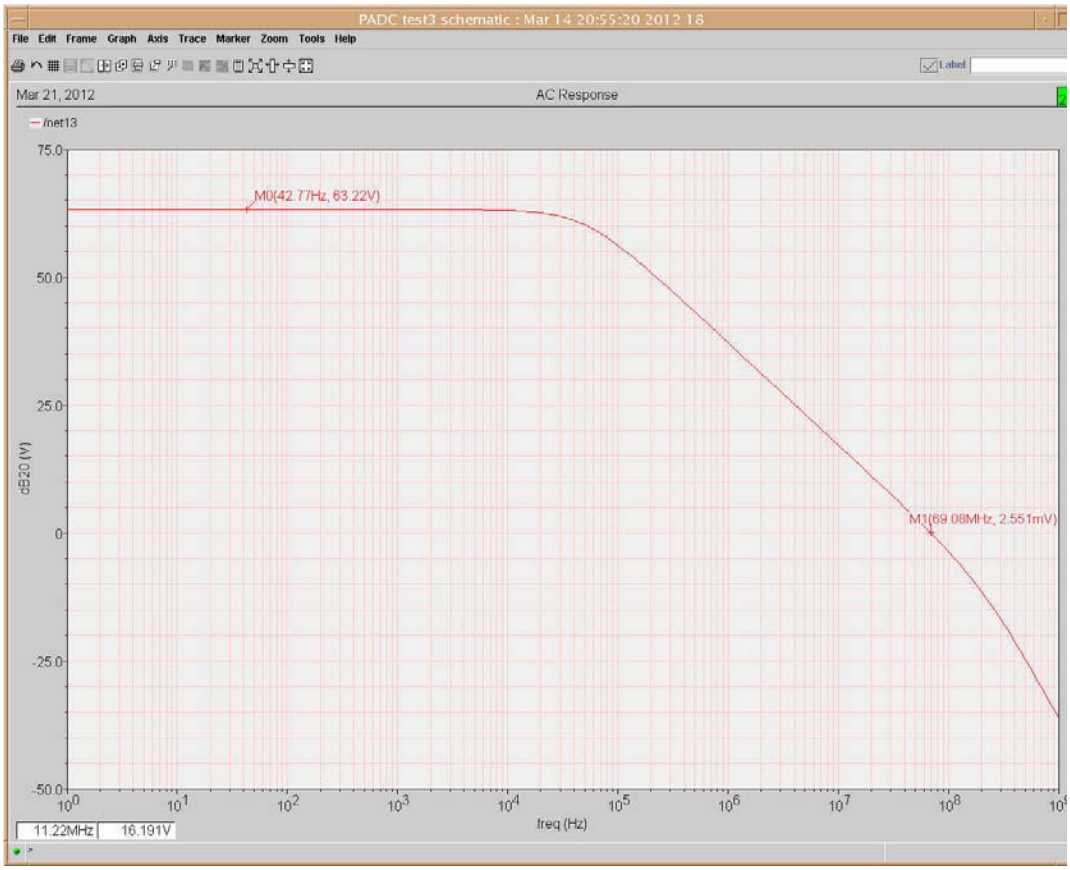
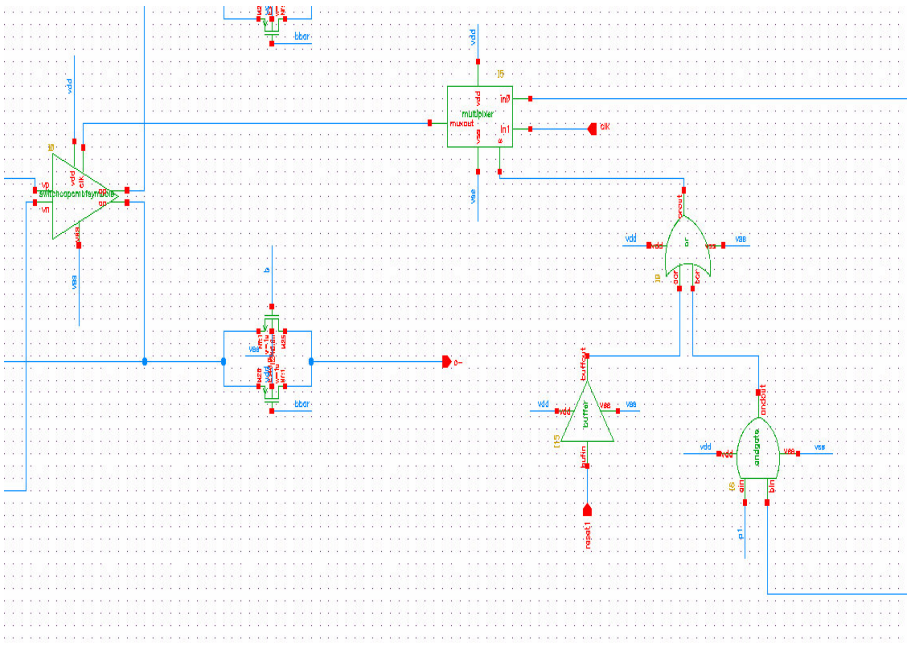


Fig. 3.8 frequency response of OP AMP

Circuit for stabilizing CMFB circuit of OPAMP



Clock is allowed to opamp only during reset or before opamp tracking input signal

Above circuit shows that clock is allowed to the circuit only during Reset+ a.p1

P1 is when request to digital block

a is when request to digital block

Implementation of sample and hold, multiplication by 2 and subtraction is done using opamp with switched capacitor circuits

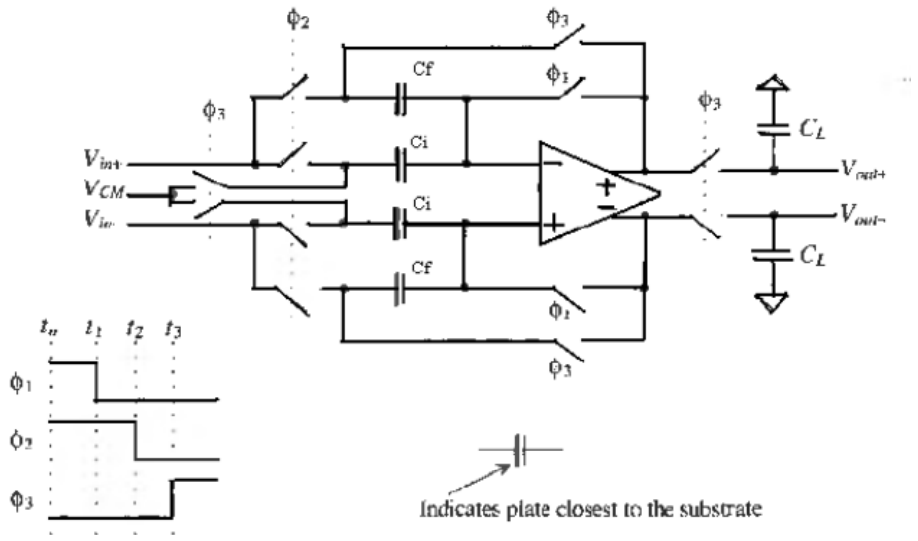


Fig 3.9 : Switched capacitor circuit

When phi1 and phi 2 switches are closed and phi3 open then the charge on Ci and Cf

Qi, f = Ci, f (vin – vcm + voffset)

When phi 3 goes high, the charge on Ci is

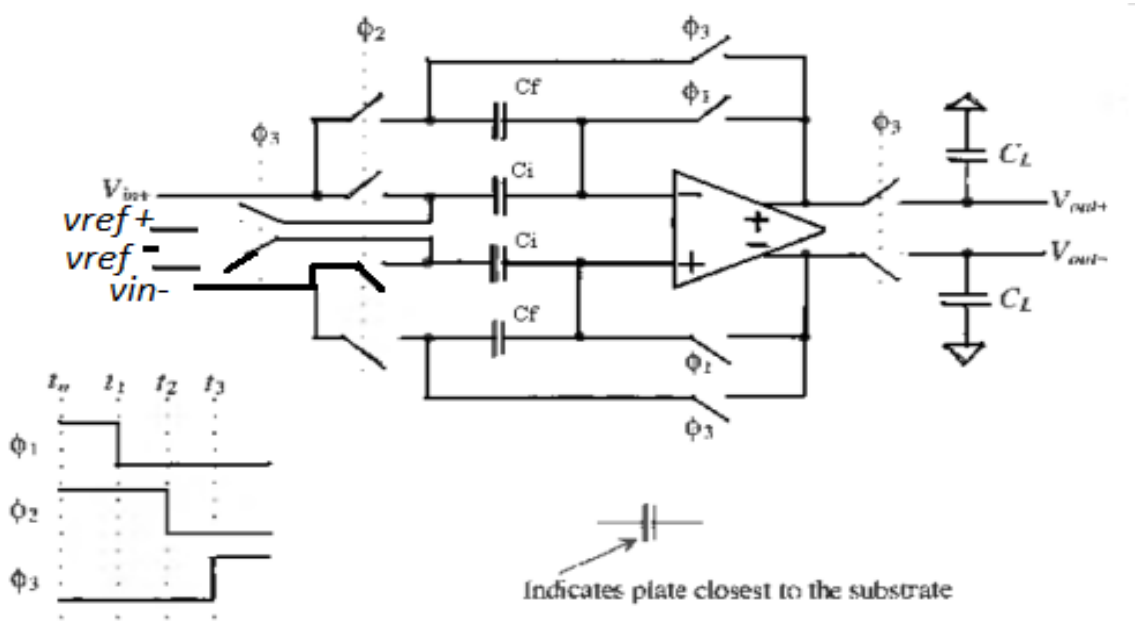
Qin = Ci (vcm – vcm ± voffset)

The difference between Qin (when phi1 is ON) and Qin(when phi3 is ON is transferred to Cf . when phi3 goes high. Since the charge must be conserved,

Cf (vout – vcm ± voffset) = Cf (vin – vcm ± voffset) + Ci (vin – vcm ± voffset)
+ Ci (vcm – vcm ± voffset)

when phi3 is on,Vout = [1+ Ci / Cf] vin – Ci / Cf vcm

Notice that the op-amp offset is automatically zeroed out.



,Vout+ = [1+ Ci / Cf] vin+ – Ci / Cf vref+

Vout- = [1+ Ci / Cf] vin- – Ci / Cf vref-

If Ci = Cf

Then

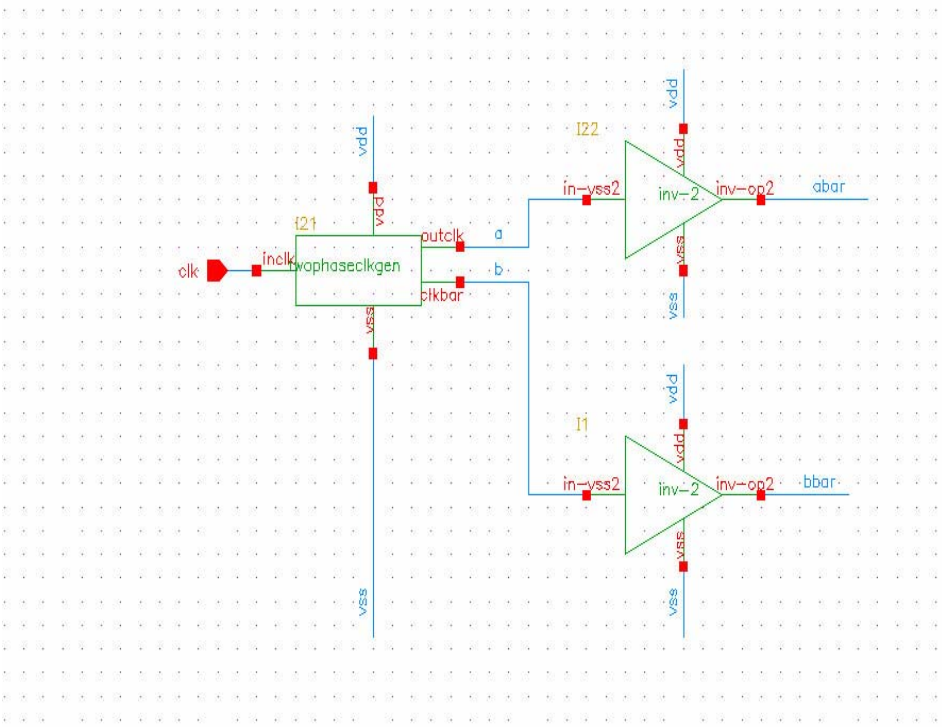
Vout+ = 2 vin+ – vref+

Vout- = 2vin- – vref-

This is how residue is calculated. Here vref+,vref- may be + vref ,zero,-vref

Depending on B1 B0.

Two phase clock generation circuit



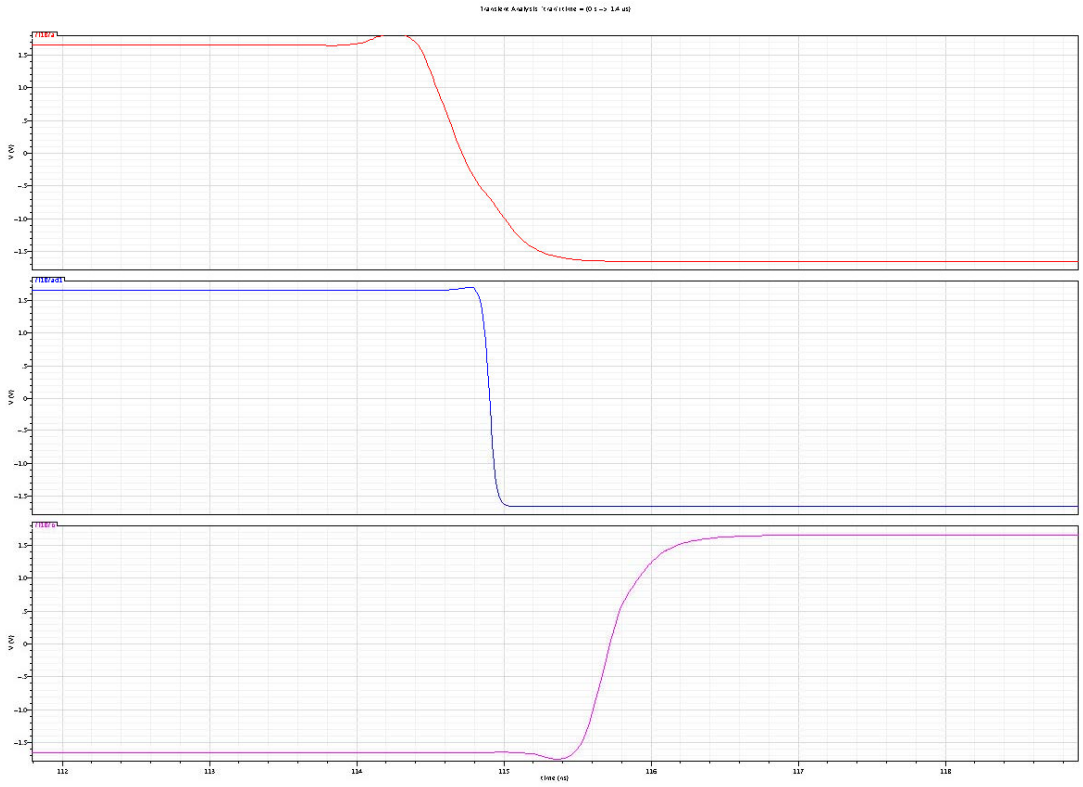


Fig. 3. 10 Two phase clock waveforms

Complete single stage 1.5 ADC

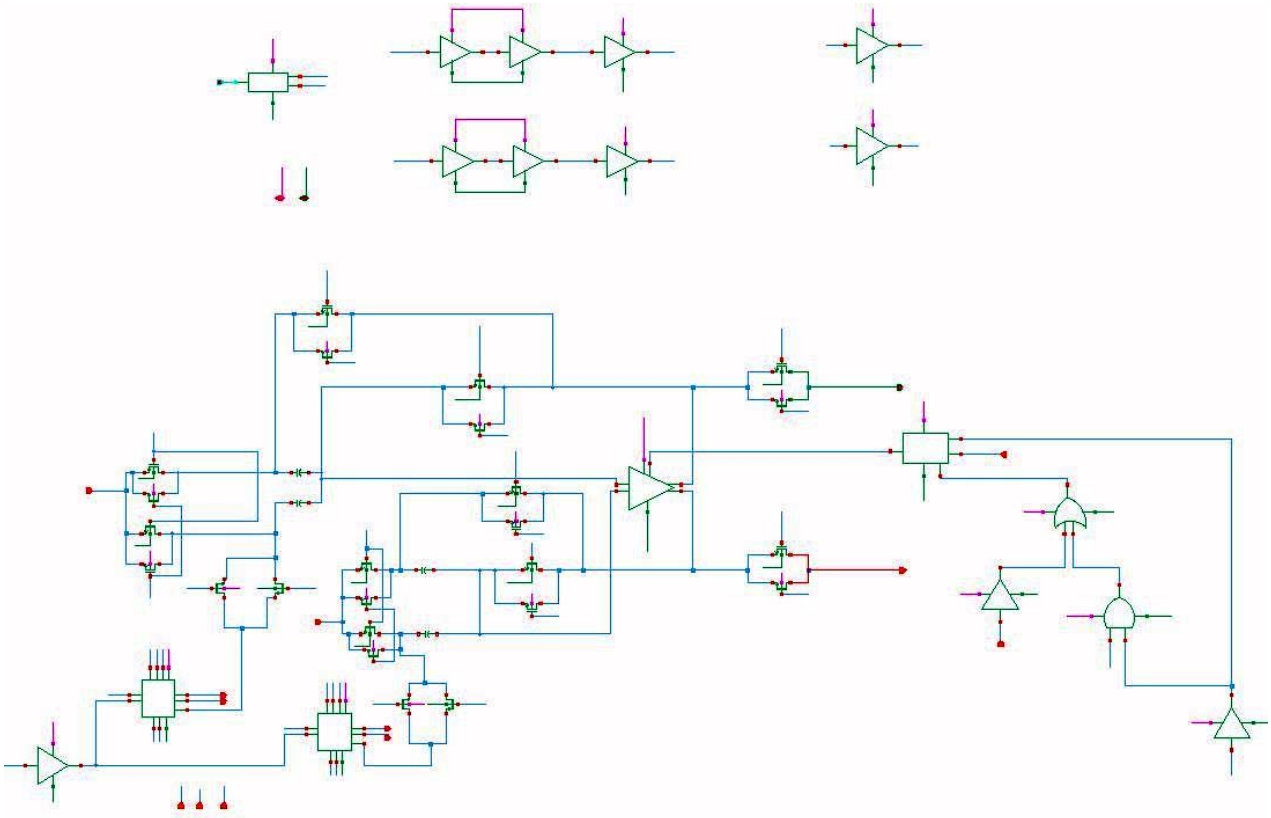


Fig 3.11 Complete single stage 1.5 ADC

This figure shows the implementation of fully differential opamp with switched capacitor as shown in the above figures. Phi1 and phi2 of switched cap is delayed from clock phases of digital circuitry

4) Muller C element

The concept of indication or acknowledgement plays an important role in the design of asynchronous circuits. Signal transitions that are not indicated or acknowledged in other signal transitions are the source of hazards and should be avoided. A circuit that is better in this respect is the Muller C-element shown in figure 3.12. It is a state-holding element much like an asynchronous set-reset latch. When both inputs are 0 the output is set to 0, and when both inputs are 1 the output is set to 1. For other input combinations the output does not change. Consequently, an observer

seeing the output change from 0 to 1 may conclude that both inputs are now at 1; and similarly, an observer seeing the output change from 1 to 0 may conclude that both inputs are now 0.

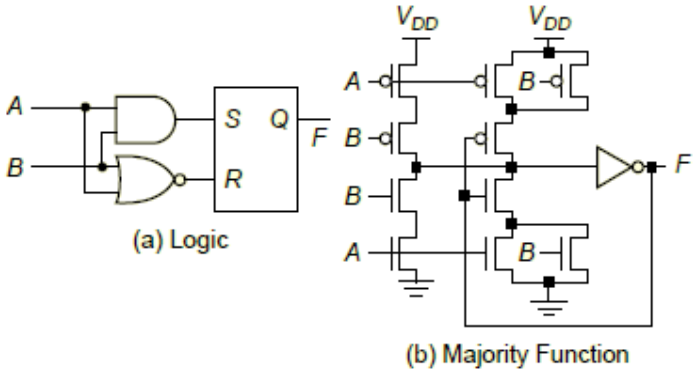


Fig 3.12 Muller C Element

Figure 14 shows a circuit that is built from C-elements and inverters. The circuit is known as a Muller pipeline or a Muller distributor. Variations and extensions of this circuit form the (control) backbone of almost all asynchronous circuits. It may not always be obvious at a first glance, but if one strips off the cluttering details, the Muller pipeline is always there as the crux of the matter. The circuit has a beautiful and symmetric behavior, and once you understand its behavior, you have a very good basis for understanding most asynchronous circuits.

The Muller pipeline in figure 15 is a mechanism that relays handshakes. After all of the C-elements have been initialized to 0 the left environment may start handshaking. To understand what happens let's consider the ith C element, C[i]: It will propagate (i.e. input and store) a 1 from its predecessor, C[i-1], only if its successor, C[i+] is 0. In a similar way it will propagate (i.e. input and store) a 0 from its predecessor if its successor is 1. It is often useful to think of the signals propagating in an asynchronous circuit as a sequence of waves, as illustrated at the bottom of figure shown below . Viewed this way, the role of a C-element stage in the pipeline is to propagate crests and troughs of waves in a carefully controlled way that maintains the integrity of each wave. On any interface between C-element pipeline stages an observer will see correct handshaking, but the timing may differ from the timing of the handshaking on the left hand environment; once a wave has been injected into the Muller pipeline it will propagate with a speed that is determined by actual delays in the circuit.

Fig 3.13 Muller C element truth table:

A	B	OUTPUT
0	0	0
0	1	Previous state
1	0	Previous state
1	1	1

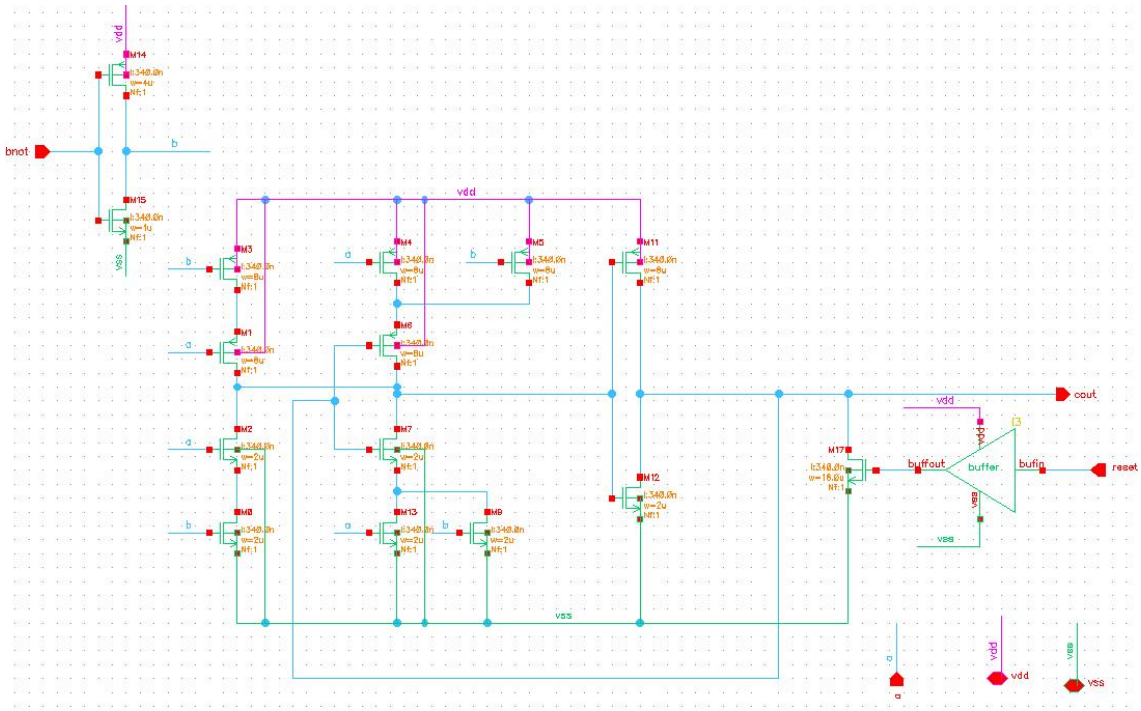
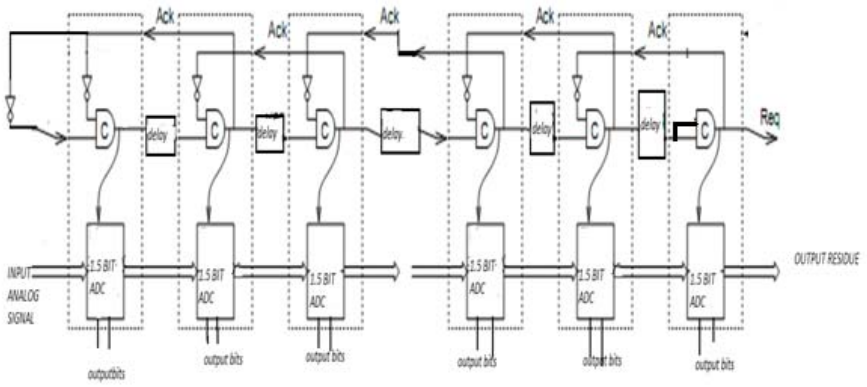


Fig 3. 14: Muller C element implementation

Fig. 3.15 4 phase protocol

Here 4 phase protocol is used, request come backs to zero after Ack is set. We are going to provide a request to pipelined 1.5 bit ADC. After processing input analog signal it sends ACK signal back .

5) Muller C element Chain:



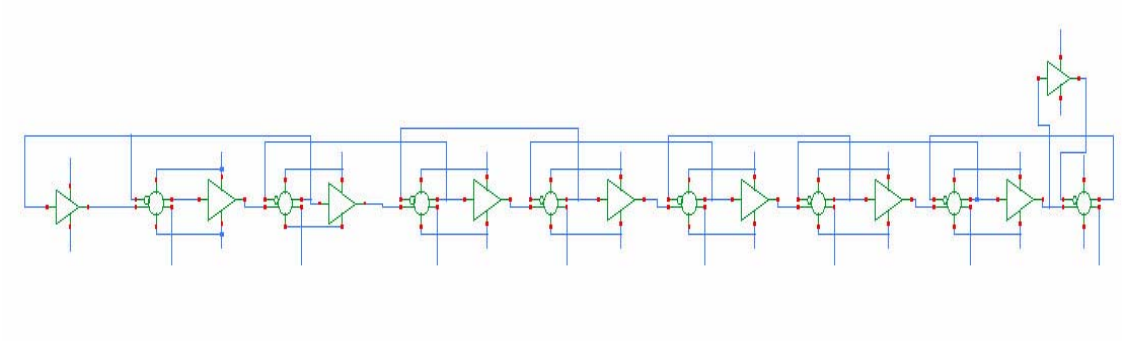


Fig. 3.16: Architecture of Muller C element chain

Suppose there are eight stages as shown in previous diagram. All Muller c outputs are initially set to zero. Suppose T is the delay caused by the delay element. We can conclude that output of every Muller C element has a frequency of 1/2T and initial delay of each Muller C element stage output will be increasing as shown in the table

All Muller C element chain outputs are

TIME	**Muller C element output**
0(reset)	0 0 0 0 0 0 0 0
T	1 0 0 0 0 0 0 0
2T	0 1 0 0 0 0 0 0
3T	1 0 1 0 0 0 0 0
4T	0 1 0 1 0 0 0 0
5T	1 0 1 0 1 0 0 0
6T	0 1 0 1 0 1 0 0
7T	1 0 1 0 1 0 1 0
8T	0 1 0 1 0 1 0 1
9T	1 0 1 0 1 0 1 0
10T	0 1 0 1 0 1 0 1
11T	1 0 1 0 1 0 1 0
12T	0 1 0 1 0 1 0 1
…	…
…	…

During ‘zero’ phase analog signal is sampled and during ‘one’ phase sampled data is been held. So, during time instance zero 1st block samples input signal. At T instant 1st block holds the data and 2nd block samples output of 1st block. At 2T, 1st block samples next signal and 2nd block holds the previous data. This goes on, this is known as pipelining and totally this is clock less pipelined ADC.

Wave form outputs

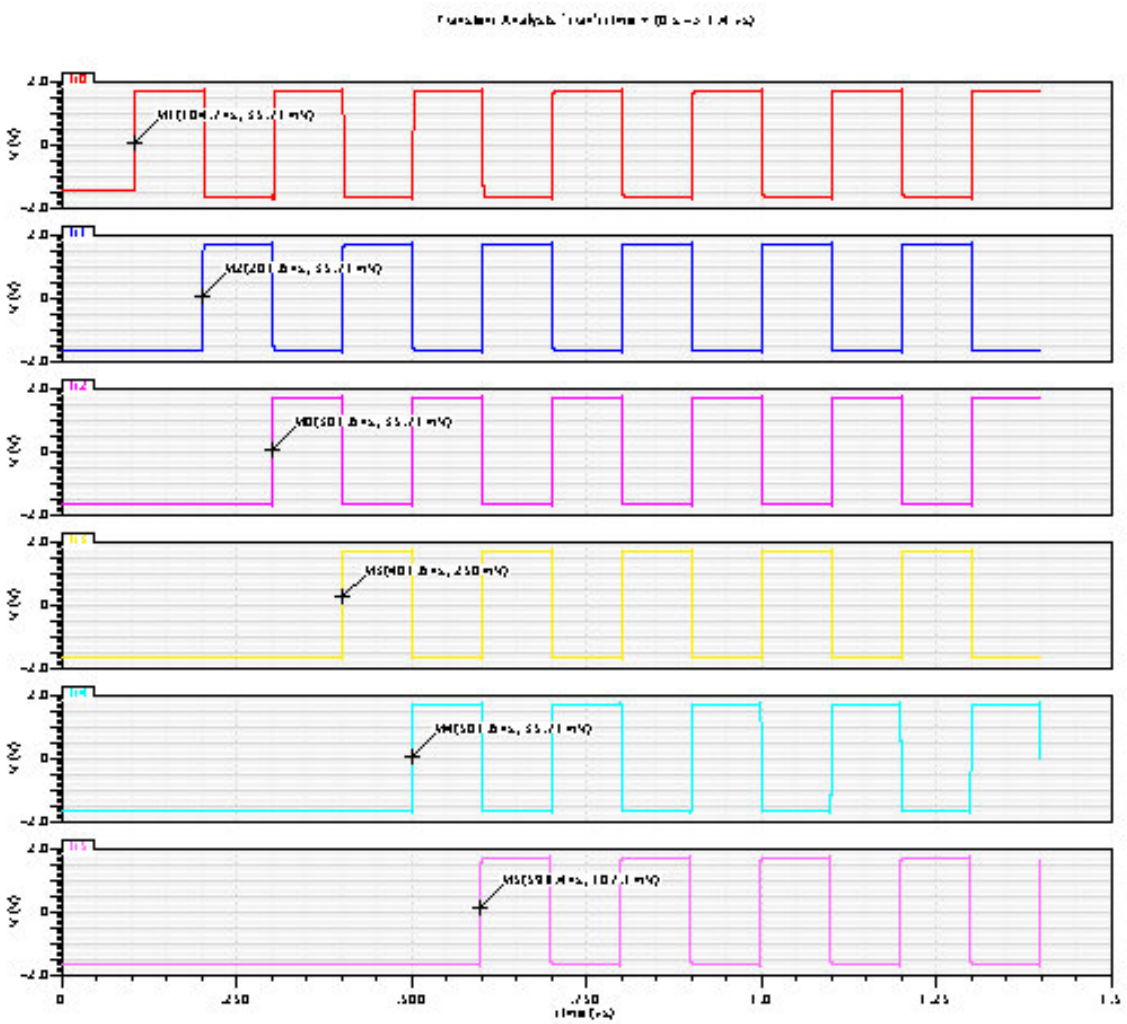


Fig. 3. 17 Wave form output

6) Digital error correction circuit:

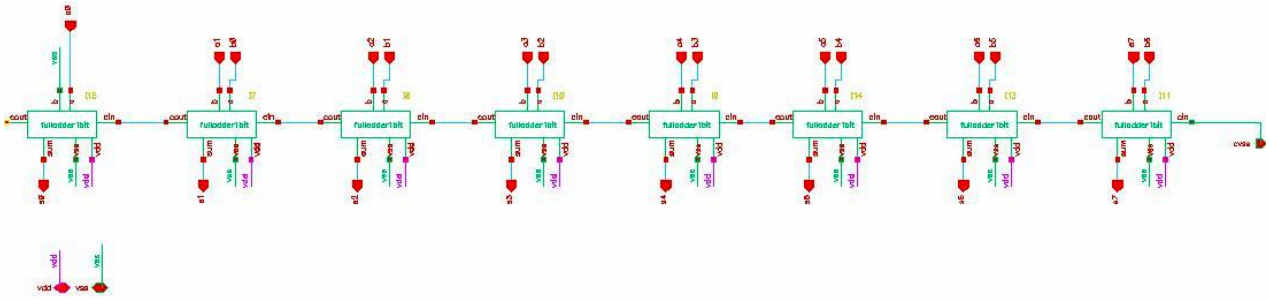


Fig. 3.18 Circuit to calculate effective single ended output

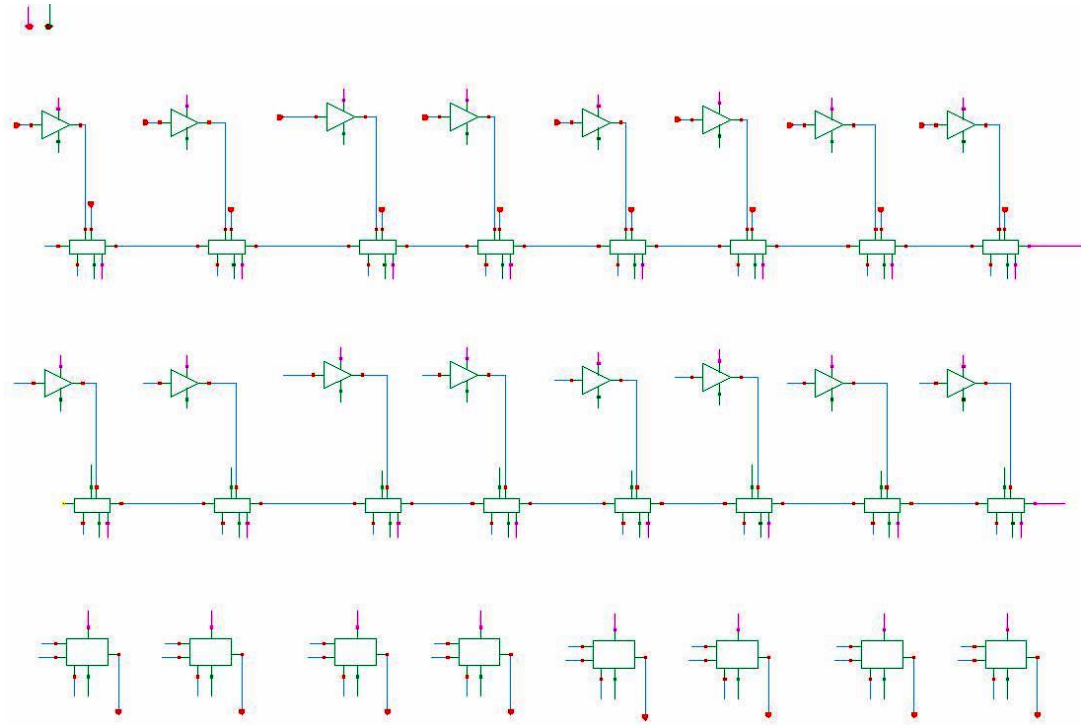


Fig. 3.19 Circuit to perform signed addition for both differential output bits

Operation of digital error correction circuit

Suppose input voltage is 0.8v and -0.8v

Output bits corresponding to 0.8 is

STAGES	**RESIDUE**	**OUTPUT BITS**								
1ST STAGE	0.8V	1	0							
2nd STAGE	0.6		1	0						
3rd STAGE	0.2			0	1					
4th STAGE	0.4				1	0				
5th STAGE	-0.2					0	0			
6th STAGE	-0.4						1	0		
7th STAGE	0.2							0	1	
8th STAGE	0.4								1	0
OUTPUT bits for 0.8 v		1	1	1	0	0	1	1	0	0

Output bits for -0.8 v

STAGES	RESIDUE	OUTPUT BITS								
1ST STAGE	-0.8V	0	0							
2nd STAGE	-0.6		0	0						
3rd STAGE	-0.2			0	1					
4th STAGE	-0.4				0	0				
5th STAGE	0.2					0	1			
6th STAGE	0.4						1	0		
7th STAGE	-0.2							0	1	
8th STAGE	-0.4								0	0
Output bits for -0.8 v		0	0	0	1	1	0	0	1	0

Verification:

Input is 0.8-(-0.8) = 1.6v

= 11100110 – 00011001 (after discarding last bit)

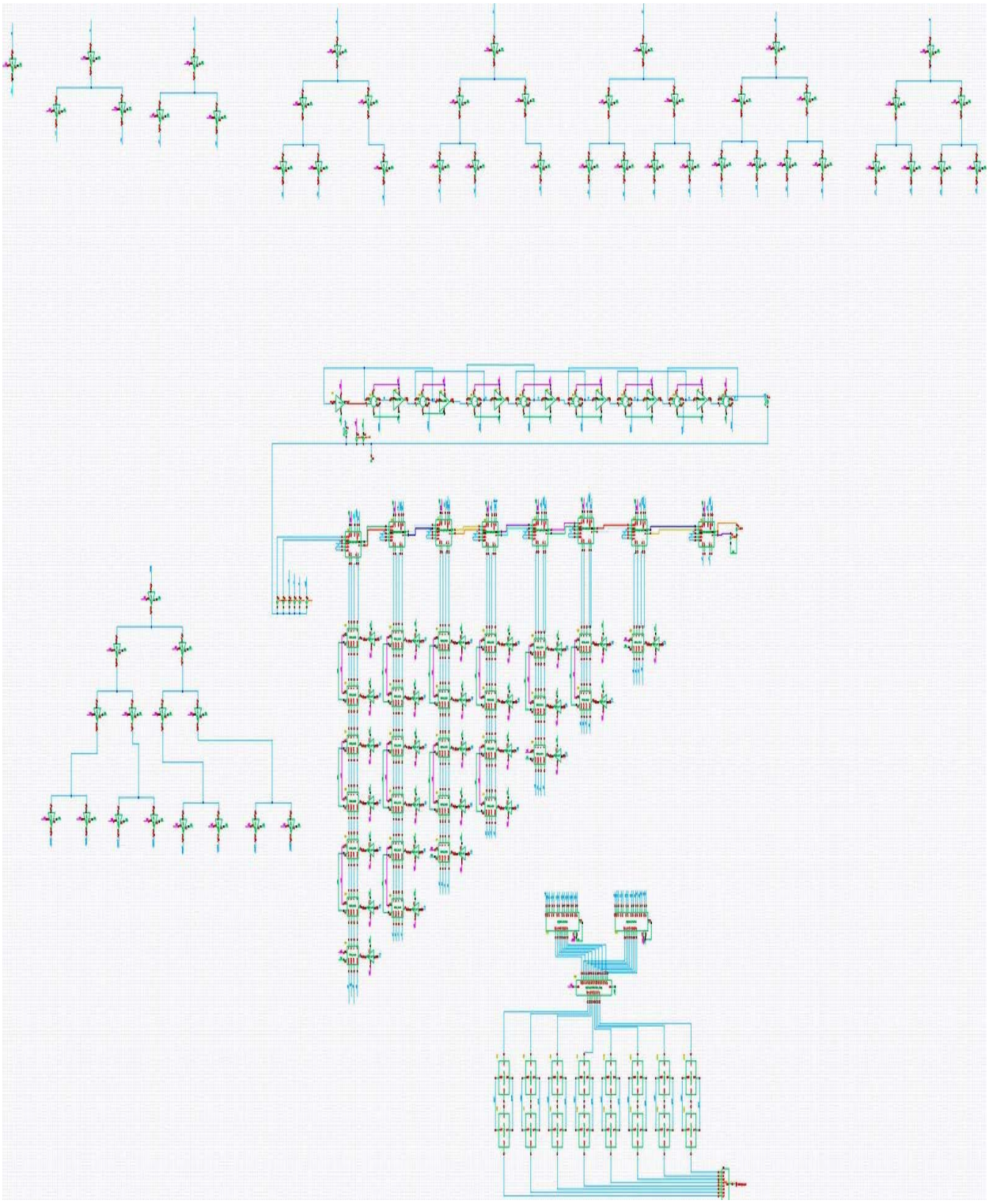
= 11100110 +11100110 (2s complement addition)

= 11001100

1 LSB = $2/2^8$ = 7.8125mv

[$1*(2)^7+1*(2)^6+0*(2)^5+0*(2)^4+1*(2)3+1*(2)^2+0*(2)^1+0*(2)^0$] * LSB =204 LSB= 1.59375V

Complete digital error correction circuit



Chapter 4: Results

1) Residue output f or DC input of 0.8 and -0.8

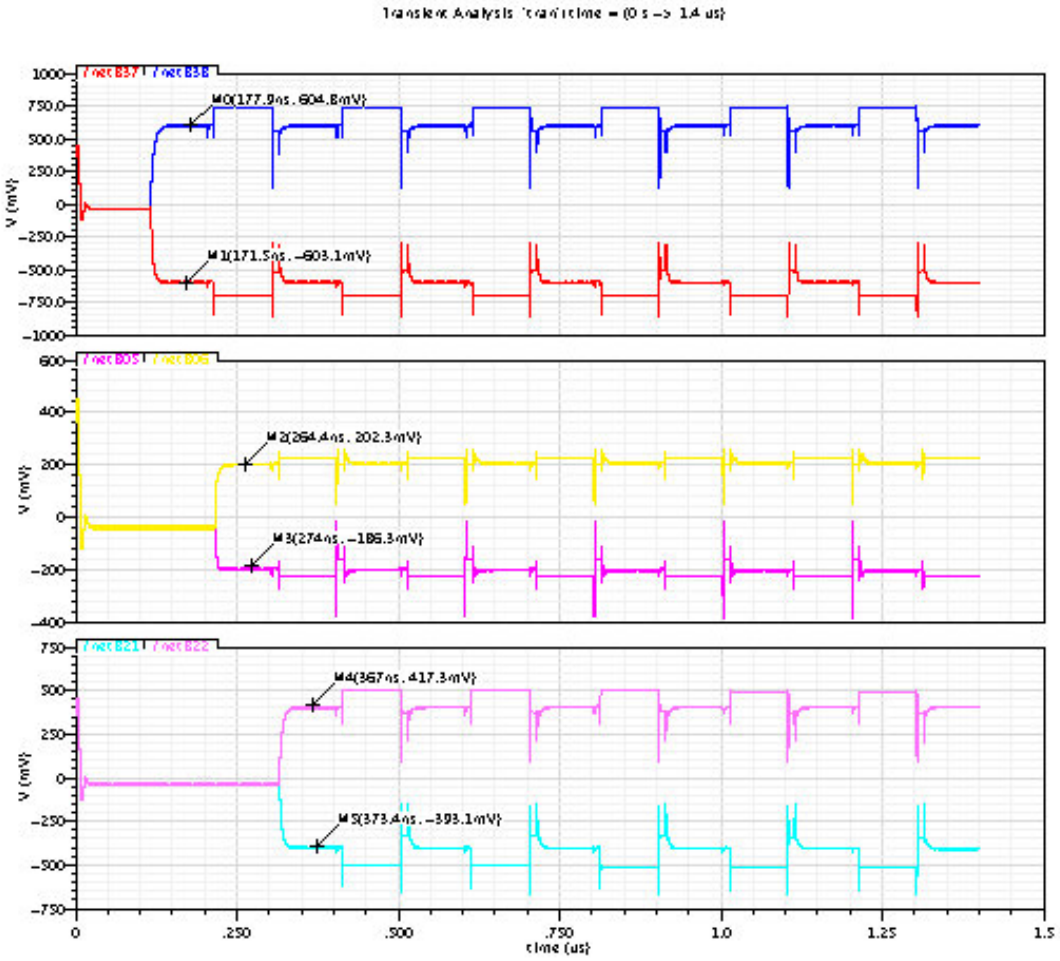


Fig 4.1: Residue output of first 3 stages of pipelined ADC

The output residue of each 1.5 bit ADC is shown in the above graph.

Here delay element is 100ns .We have made reset signal active till 100ns. Here, we represent 100ns as T.

So till 100ns, 1st stage samples input signal and after 100ns.

As can be seen in the above figure that 1st stage is in hold mode and second stage will come to sampling mode.

After 200ns 2nd stage comes to hold mode as shown in the above figure and 1st will be tracking next input. Since, here input is constant dc of 0.8 volts, so output 1st stage and above process continues till 8th stage

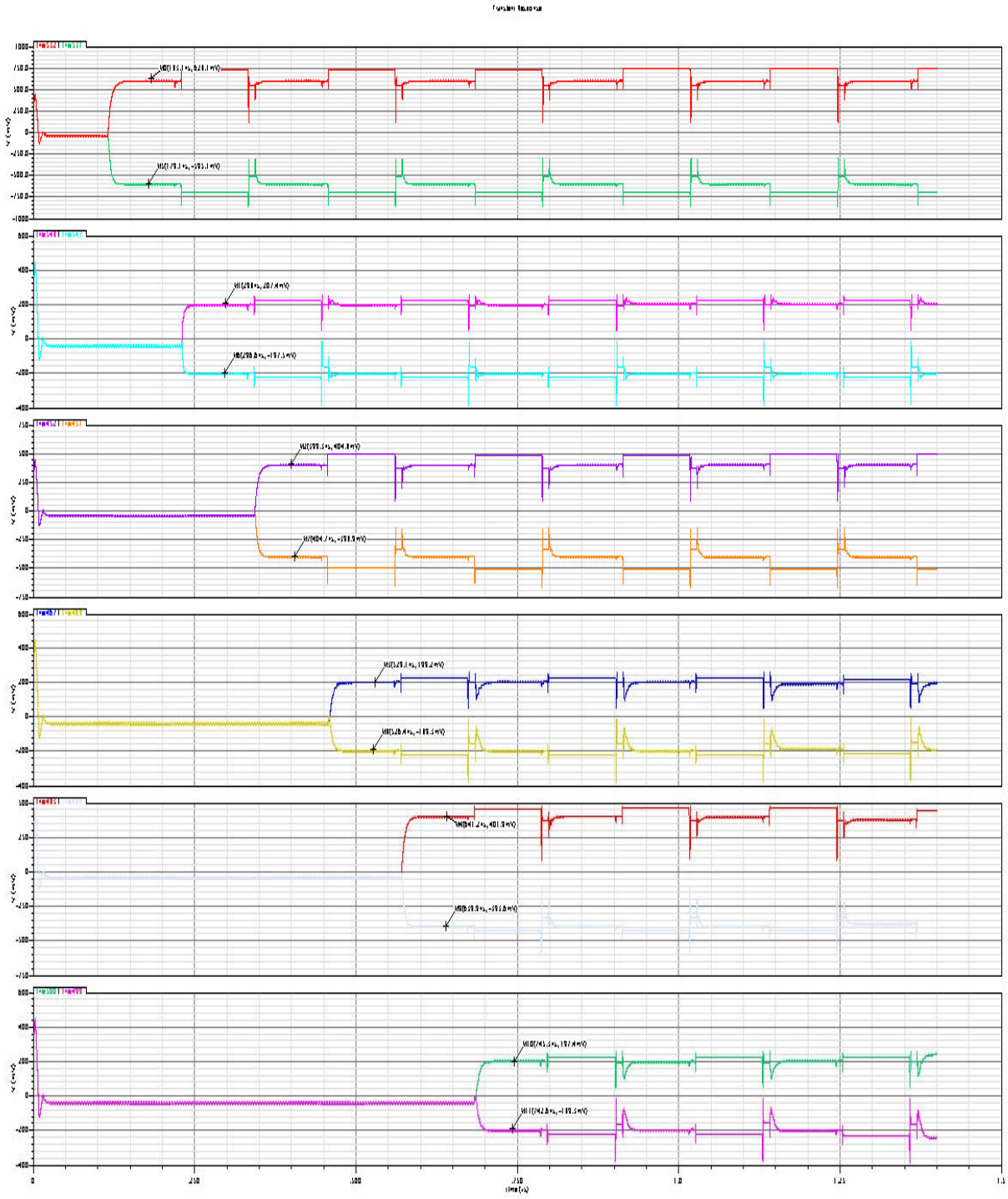


Fig 4.2: Residue output of all the stages of pipelined ADC

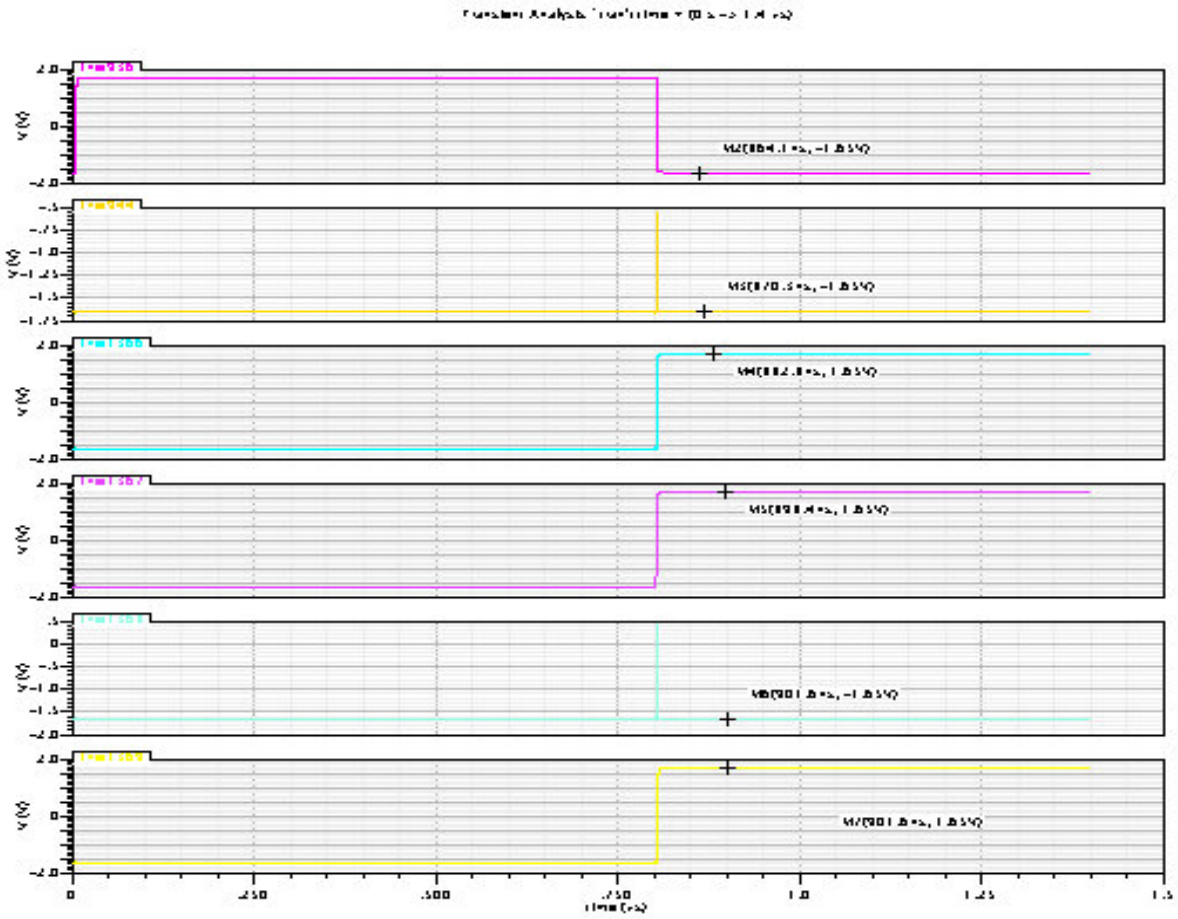


Fig 4.3: Digital output of pipelined ADC after 800ns

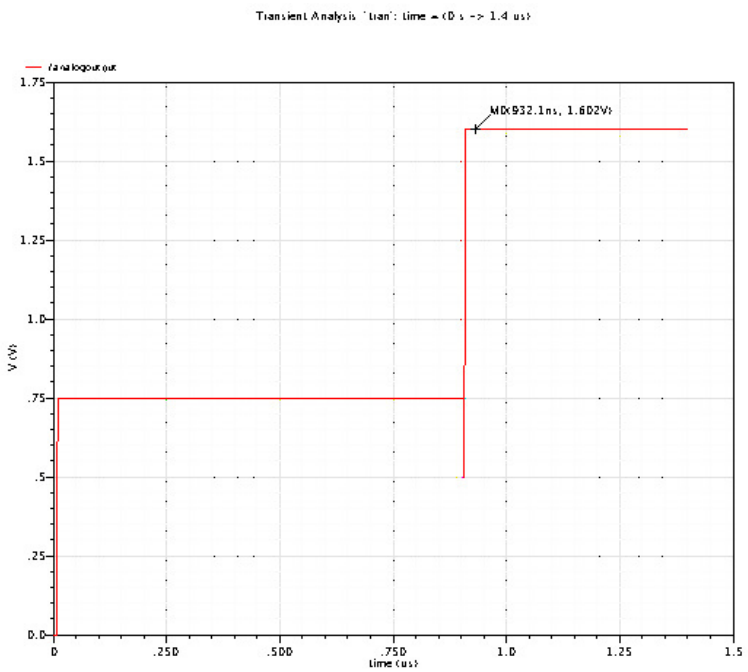


Fig 4.4: Digital output converted to Analogue using an ideal DAC

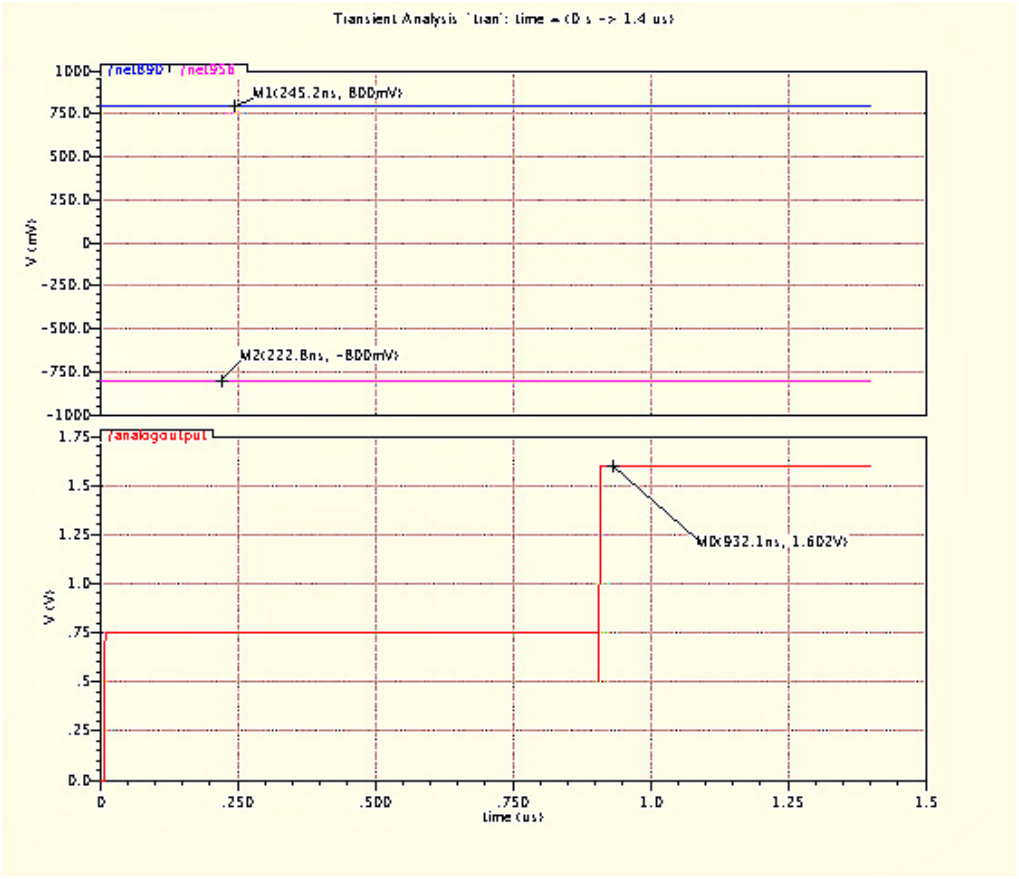


Fig 4.4: Analog input (0.8 and -0.8) with analog output (seen after 800ns)

b) Output for Sinusoid input:

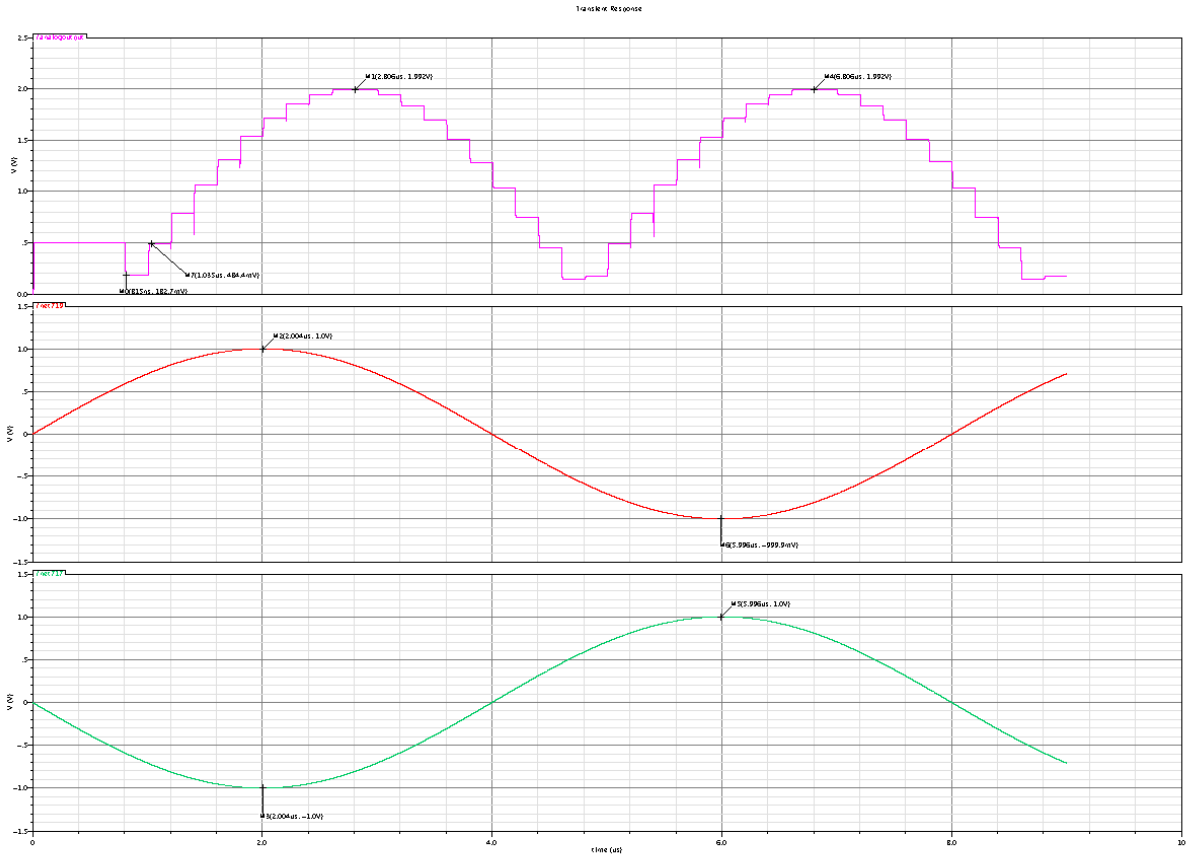


Fig 4.5: Input signal of 1Vpp in phase is given at positive input terminal and out of phase is given at negative terminal .Analog output of 2 Vpp is obtained at the output

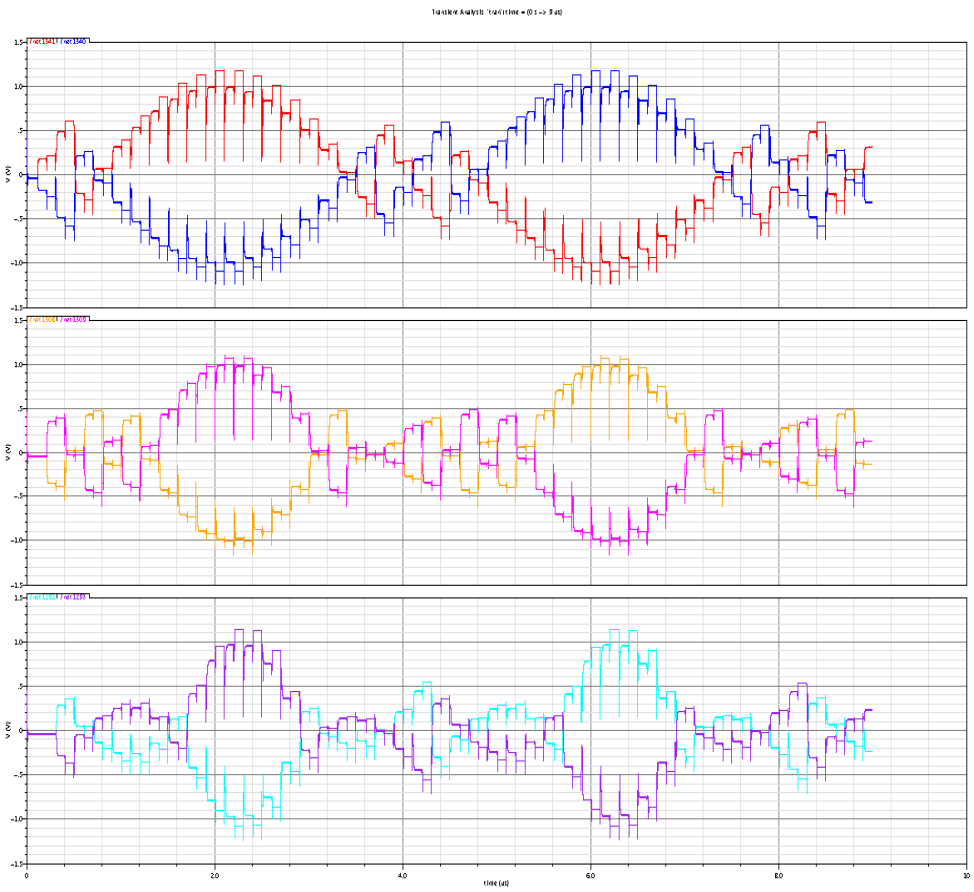


Fig 4.6: Residue output of first three stages of opamp

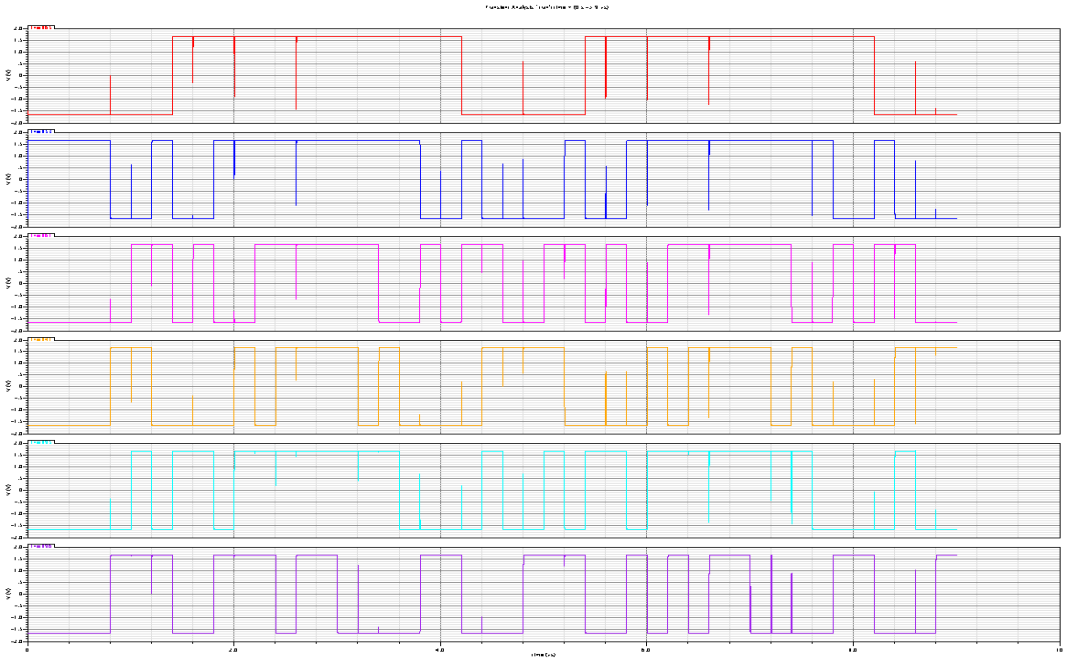


Fig 4.7: Digital output of for sine wave input

Chapter 5

Conclusion

We have completed the circuit design of a self triggered analog to digital converter suitable for low power self trigger-able space and medical applications Main drawback of this above circuit is it is temperature variant. Input signal is sampled at the rate of 10 M samples per second which varies +10% or -10% at different process corners

Tasks to be completed

1. Need to verify INL, DN, SNDR, Effective No of BITS etc
2. Mismatch analysis – Monte carlo Analysis and layout completion
3. Prototype development and testing

References

1. R. Jacob Baker, CMOS mixed signal circuit design, 2nd , IEEE press, 2003.
2. CMOS: Circuit Design, Layout, and Simulation by R. Jacob Baker
3. Digital integrated circuits 2nd edition JAN M.Rabaey
4. International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011 A 80Ms/sec 10bit PIPELINED ADC Using 1.5Bit Stages And Built-in Digital Error Correction Logic