

# *Design of OP-AMP using CMOS Technology & Its Application*

Arun Katara<sup>1</sup>Asst.Prof.,Dept. of  
ElectronicsDatta Meghe Institute of  
Engineering, Technology &  
Research

Wardha, India

arunkatara@gmail.com<sup>1</sup>Riya Balwani<sup>2</sup>Student of VIII Sem.,Dept. of  
ElectronicsDatta Meghe Institute of  
Engineering, Technology &  
Research

Wardha, India

balwanirya.22@gmail.com<sup>2</sup>Priya Wagh<sup>3</sup>Student of VIII Sem.,Dept.  
of ElectronicsDatta Meghe Institute of  
Engineering, Technology &  
Research

Wardha, India

piyuwagh20@gmail.com<sup>3</sup>Prachi Salankar<sup>4</sup>Student of VIII Sem.,Dept. of  
ElectronicsDatta Meghe Institute of  
Engineering, Technology &  
Research

Wardha, India

prachisalankar@gmail.com<sup>4</sup>

**Abstract**—In this paper a CMOS operational amplifier is presented. A CMOS operational amplifier is presented here which is operating at 2V power supply and 1microamp input bias current at 0.8micrometer technology using nonconventional mode of MOS transistors and whose input is dependent on bias current. The unique behavior of the MOS transistors in sub threshold region allows a designer to work at low input bias current. It also allows operating at low voltage. While operating the device at weak inversion results low power dissipation but dynamic range is degraded. Optimum balance between power dissipation and dynamic range results when the MOS transistors are operated at moderate inversion. In comparison with the reported low power, low voltage op-amps at 0.8micrometer technology, this op-amp has very low standby power consumption with a high driving capability and operated at low voltage. operating the device in moderate version is a good solution. Also operating the device in sub threshold region not only allows lower power dissipation but also a lower voltage operation is achieved. The proposed op-amp is a simple two stage single ended op-amp. The input stage of the op-amp is a differential amplifier with an NMOS pair. Operational Amplifiers, or Op-amps as they are more commonly called, are one of the basic building blocks of Analogue Electronic Circuits. Operational amplifiers are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation.

**Index term**—MOS transistor, Amplifier, Operational amplifier, Integrated circuit, Differential amplifier, Logic gates.

## I. INTRODUCTION

VLSI design is one of the technique of placing hundreds or thousands of electronic components on single chip. The VLSI design may consist of mixed signals, high power and small chip area. The design of CMOS power amplifier which is applicable for wireless communication system. Operational

amplifier is one of the most widely used building blocks for analog systems. One electronic device which can be used to construct arithmetic circuits is called as operational amplifier. Silicon technology continues to scale down to ever smaller transistor sizes to supply the market need, so as to accommodate more and more transistors in IC. To develop efficient portable electronic equipment the semiconductor industry has pushed the circuit designers towards low voltage power supply and low power consumption of circuits.

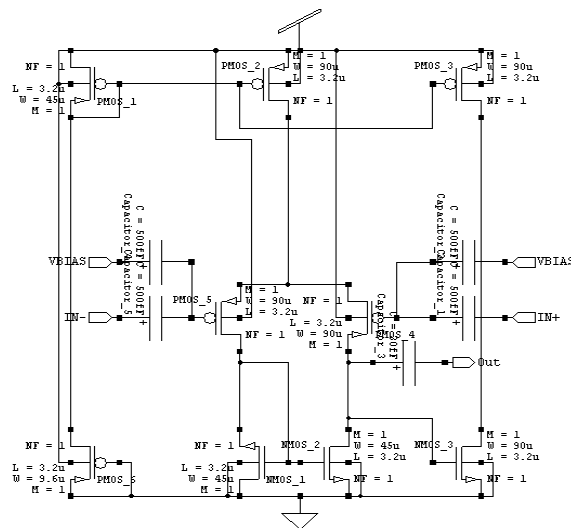
Power dissipation in a circuit can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. Op-amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high speed amplification or filtering. Operational amplifier controls the voltage. There are three types of parameters they are Area, Delay, Gain. In operational amplifier we can control only two parameters at a time. Hence, when we controlled these two parameters then automatically third one will be increased.

An Op-amp is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the result operation of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of “Operational Amplifier”. Furthermore, the rapid growth of portable applications promotes battery operation which favors low voltage and low power circuits. As a result, many suggest that future implementation of mixed analog –digital circuits using standard CMOS will have power supplies.

## II. OPERATIONAL AMPLIFIER DESIGN

Operational amplifiers have sufficiently high voltage gain so that when the negative feedback is applied, the closed-loop transfer function can be

made practically independent of the gain of the op-amp. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement the negative feedback concept. One of the popular op-amp is a two stage op-amp. The differential pair in Fig.2 is formed by p-channel MOSFETs, PMOS\_4 and 5. The first stage gives a high differential gain and performs the differential to single ended conversion. This first stage of op-amp also had the current mirror circuit formed by an n-channel MOSFETs, NMOS\_1 and NMOS\_2. The transistor PMOS\_3 serves as a p-channel common source amplifier which is the second stage of op-amp and is aided by current load NMOS\_3. The bias of the op-amp circuit is provided by PMOS\_1 and 5 transistor. To sustain a constant transconductance from a simple differential pair, we must ensure that the common mode input voltage stays adequately



**Fig2:** Two-stage CMOS operational amplifier Which allows having a phase margin of -111degree?

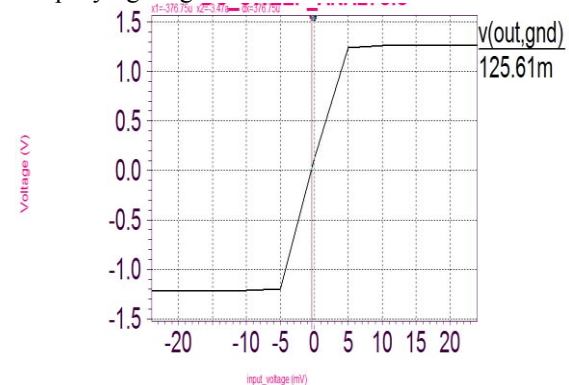
#### (a) DESIGN OF CHARACTERISTICS OF OP-AMP

Figure3., shows the transfer characteristics obtained from DC sweep analysis. The input offset voltage is approximately 0.376 mV. Figure 4 shows the transient analysis of operational amplifier.

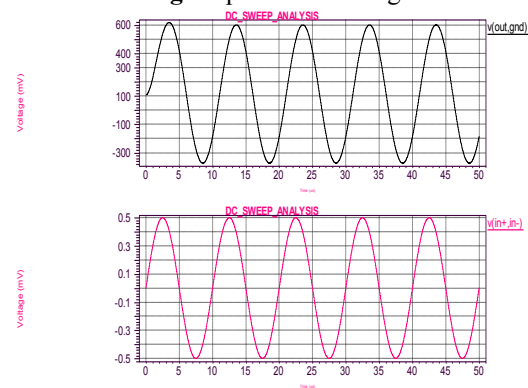
far above ground so that the gate-to-source voltage of the input transistors is large enough to pass a significant fraction of  $I_b$ .

The operational amplifier is made stable by using the compensation capacitor. The capacitor introduces a dominant pole and decreases the gain so that the phase margin is positive. Phase margin is defined as how far the phase of the circuit is away from 180degree at a gain of 0 dB. A negative phase shift implies that a negative feedback loop acts as positive feedback loop and hence making the loop unstable. In this design, the capacitor introduces a dominant amplitude modulators each followed by a conventional delta-sigma modulator. The modulator outputs are then filtered, demodulated, and summed together to produce a single digital output sequence pole.

Amplifying signal from 0.5mV to 600 mV.

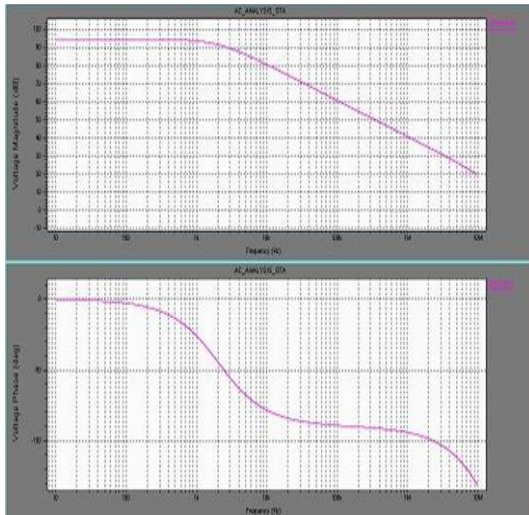


**Fig3:** Input offset voltage



**Fig4:** Transient analysis of op-amp circuit

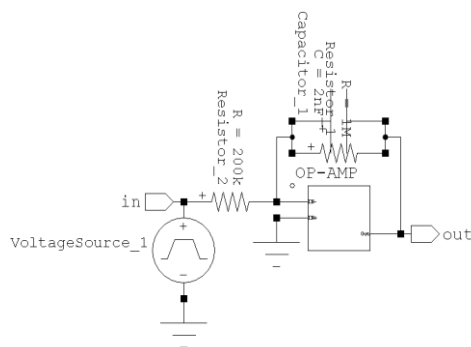
Characteristics. The DC gain of the amplifier is 94.64 db. The unity gain bandwidth of the amplifier obtained is approximately 14 MHz. The integrator is design by the op -amp and resistor, capacitor combination. Fig 5. Shows the a.c analysis.



**FIG.5: AC Analysis**

### (b) DESIGN OF INTEGRATOR BY USING OF OP-AMP

The integrator circuit shown in fig 6.

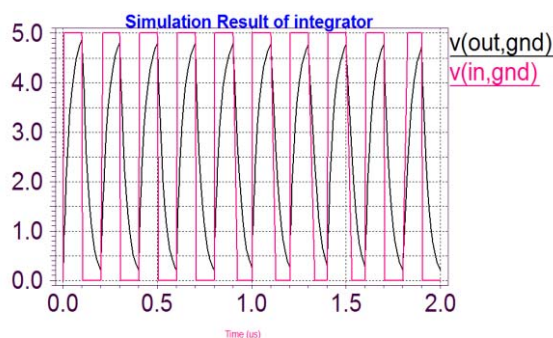


**Fig6: Integrator circuit**

The output of the integrator is shown in fig 7.

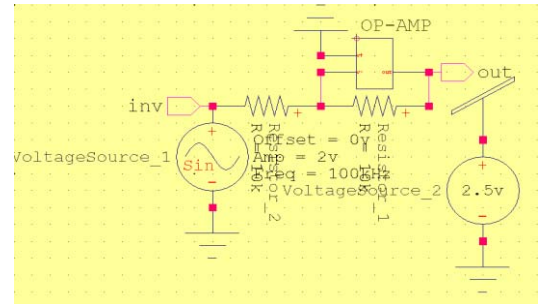
$$V_{out} = -1/RC \int V_{in} dt$$

Here  $R=200K$  &  $C=2nf$

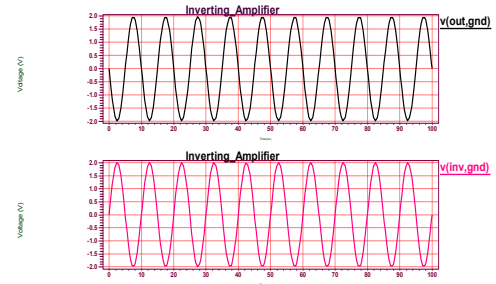


**Fig 7: Simulation result of integrator**

### (C) DESIGN OF INVERTING-AMPLIFIER BY USING OF OP-AMP

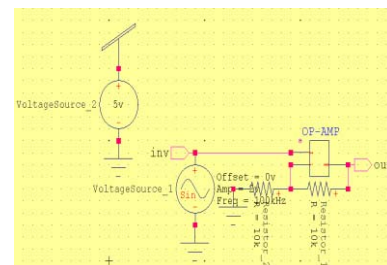


**Fig 8: Inverting Amplifier**

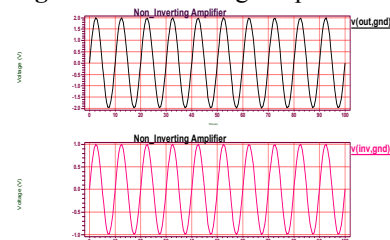


**Fig 9: Simulation result of Inverting Amplifier**

### (d) DESIGN OF NON INVERTING-AMPLIFIER BY USING OF OP-AMP



**Fig 10: Non-Inverting Amplifier circuit**



**Fig 9: Simulation result of Non-Inverting Amplifier**

## III. CONCLUSION

The amplifier presented in this paper operates at weak and moderate inversion and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. As the opamp works at weak and moderate inversion, low power as well as low voltage can be achieved. Moreover, best tradeoff among area, power

and speed is achieved when the transistors work in moderate inversion region. Its slew rate is higher than reported low power low voltage amplifiers at 0.65  $\mu\text{m}$  technology. Also its size is fairly small. The simulations and layout is done using professional software Mentor Graphics.

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