Low Power Dynamic Comparator Design for High Speed ADC Application

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***Abstract*- Comparator is the heart of Analog to Digital Converter (ADC). In order to design a ultra less power consuming, small delay ADC it force us to design a dynamic comparator to maximize power efficiency and speed. The main use of comparator in ADC be comparison of a given input continuous analog signal along with certain threshold signal to give a output signal depend on whether the analog signal is higher or lower than the threshold signal. Here paper designs a pre-amplifier based comparator utilizing cadence tool. In this proposed design the MOS transistor of length 180nm and width of 720nm and the power supply in the range 1.2V to 1.8V were used. Here the proposed deign has been implemented in various CMOS families using cadence virtuoso 180nm CMOS technology its performance has been simulated and compared to choose the best among them based on power consumption and delay. From the comparison table, it is concluded that the proposed dynamic circuit that is un footed consumes the least power of 51.3µW with the delay of 208pS.**

Keywords—ADC, Comparator, Delay, Power, signal

I. INTRODUCTION

In today's world everything is digitized for example mobile banking, debit card etc., but nature is analog. So it is needed to convert the analog into digital then only the day today work and all possible. For converting analog signal into a digital signal it require a ADC. In recent days less delay is required for high speed application high speed analog to digital convertor becomes a major requirement of day to day life. With only higher speed device no one can do anything though power consumption of high speed device should much lower for best performance. The need for low power consumption in all the devices one factor that can be modified be the area reduction or speed reduction. Reducing speed cannot be appreciable since everything moving towards high speed application. Thus this paper focuses on area reduction by utilizing dynamic logic which in turn reduces the feature size.

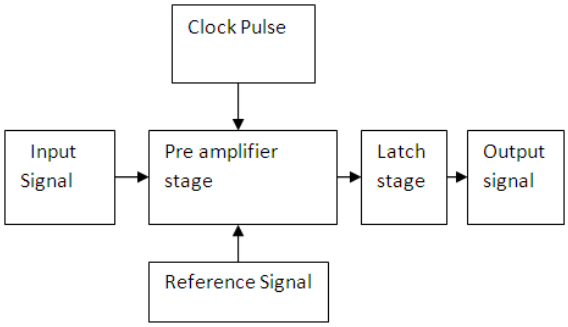

Fig. 1 Block diagram of comparator

The limiting blocks in reducing performance of an ADCs are typically inter stage gain amplifier and comparators in which comparators are the most important. The basic blocks of a comparator is shown in Fig. 1. Therefore, the various design issues related to gain, speed, power dissipation, are of consider being importance. Dynamic comparator is high speed, low power comparator having zero static power consumption gives full-swing digital output voltage in shorter time duration. The power consumption in dynamic comparator can be further reduced by using latch which is nothing but back to back connected inverter. But these input referred latches create many mismatches in comparator operation leading to use of many component to compensate such mismatches. As a result delay and power consumption become dominate. Practically says, the latched input signal can be replaced by utilizing pre amplifier with a regenerative output latch as shown in Fig 1. The pre amplifier is used in order amplify the small differential analog signal to large signal in order to overcome latching mismatch and also reduces

noise. Since CMOS transistor consumes low power compared to all other transistor technology this project focus on CMOS transistor for designing comparator.

Comparators are the most required component next to operational amplifier in the world of electronics. Comparators are also known as 1 bit analog to digital converter because of its function they are widely used in ADC too. Consider an ADC [1] the foremost job is to sample the input analog signal then the sampled signal is quantized and finally encoded to get a digital signal at the end. You may ask now it only Performing sampling quantizing and encoding in all the activities where the application of comparator be. The answer to this was, while quantizing the sampled signal the comparator is utilized for comparing the sampled input signal with those reference signal based on the comparison whether the input signal is higher or lower the reference signal the conclusion has been taken by the comparator. The symbol of basic comparator is shown in Fig. 2.

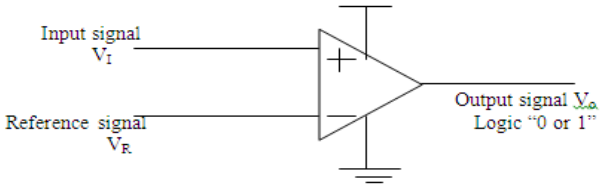

Fig. 2 Schematic of a comparator

Input signal is applied to positive terminal of the comparator and the reference signal is applied to negative terminal of the comparator, the applied reference signal is of DC signal consider for example 1.5V. When the applied the input signal less than the reference signal logic 0 is provide as output signal. In other way when the applied input signal is greater than the reference signal the logic 1 is provide as the output signal the ideal transfer characteristics of a CMOS comparator is shown in Fig. 3

The operation of a comparator can be mathematically written as

$$\text{If} \begin{cases} V_I \geq V_R, \text{ then } V_o \text{ be Logic 1} \\ V_I < V_R, \text{ then } V_o \text{ be Logic 0} \end{cases}$$

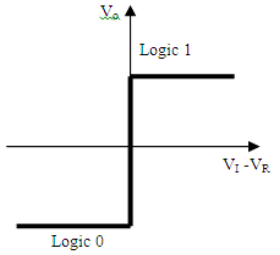

Fig. 3 The ideal characteristics of a comparator

II. RELATED WORKS

High speed comparators are highly used because of its need in high speed application. These high speed comparators mainly includes consist of three blocks first is the input stage second stage is of flip-flop at last a SR latch. The design approach was implemented in a 1.5µm CMOS technology operating at a frequency of 65MHz. The operating voltage is of 2.5 V [1]. The sampling frequency of 65 MHz, comparator, the clock and input signal of 32.5 MHz at a offset voltage of 3.3mV [2]. The total power consumption of a comparator is of 0.85mW.

The comparator in [3] deals with a preamplifier stage, comparing stage and finally a NAND gate. The pre amplifier stage is made of differential amplifier which helps in providing positive feedback to the non clocked circuit. The amplified signal is used to increase the accuracy of the comparator output. The pre amplifier compare the input signal with the reference signal [4] it amplify the result of comparison such that input offset and kickback noise get eliminated.

The resistive laddered ADC architecture has been implemented in a 0.35µm technology with 3.3V power voltage [5]. The total power consumption of above ADC be 759mW. The [6] comparator is mainly used for high speed ADC application, the comparator operates at a frequency of 45MHz with a supply voltage of 3.3V the total power consumption of the above comparator be 2mW.

The various application of comparator [7] include Null detector, Zero crossing detectors, Relaxation oscillator, Level shifter, ADC, Window detector importance of comparator are explained in brief. The main characteristics of Comparator include static and dynamic. Static characteristic include the gain, resolution, input offset voltage and noise has been discussed in deep [8] which will explained in brief here. First of all lets discuss about gain from the transfer characteristics of the comparator the gain is defined as the minimum change in input necessary to cause output to get vary between two logic states either logic zero or one. Second thing is of resolution [9]which defines how accurate the change occur with the time i.e at one point of time both the input as well as output should irrespective of external environment. Input offset voltage has been categorized into two one is systematic offset and another one is random offset. The offset mainly defines how much voltage is at the terminal of the output when there is no voltage in the input terminal. Zero offset is mainly preferred for proper functioning of all electronic devices.

The dynamic property [10] includes speed and power consumption. The speed of the device is defined with the help of propagation delay. Speed and delay is inversely

proportional so reducing the propagation delay one can increase the speed of the device thus the design of high speed comparator require a ultra low propagation in the range of Pico second. The power consumption is an main characteristics. Increase in speed ultimately increases the power. Power and speed are the important factors to be considered while designing comparator. [11] Since the static characteristic has some impact on device performance but it won't affect operation of device. But change in dynamic characteristics leads to improper functioning or the device may become dead. In this paper the designed comparator is meant for ADC application. Here the power and delay are the main characteristics to be determined in order to predict the performance of the comparator.

III. PROPOSED COMPARATOR AND ITS OPERATION

In the design of comparator circuit, the preamplifier and the decision circuit are the major block to be considered because the main problem in the comparator is input offset voltage which has a impact on the speed and resolution. The widely used preamplifier circuit is the differential amplifier. [12] The basic circuit diagram of the differential amplifier circuit is shown in Fig. 4

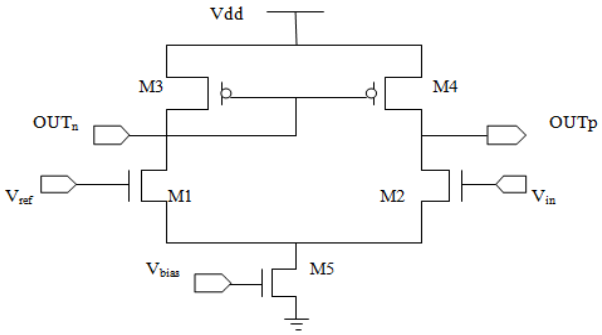

Fig. 4 Pre amplifier circuit

On observing the above pre amplifier circuit, M3 and M4 are the pull up transistor they are initially made to conduct my making their gate supplied with zero potential. Since they are controlling the operation of the entire amplifier it is otherwise said to be a controlling transistor. Then the input analog signal is applied to input terminal of M2 and the reference signal is given to the gate of M1

Operation of the circuit can be explained in two cases
Case1: If the input signal is less than the reference signal which makes M1 to turn ON and M2 OFF. M1 cause the M3 to be at cutoff state while M4 is in saturation state causes the output OUT_p logic high. Since M3 is in cutoff state and M1 pulls the OUT_n to logic low signal.

Case2: If the input signal is greater than the reference signal cause the M2 to turn ON and M1 to turn OFF which in turn cause the M3 to be saturated state providing logic high output at OUT_n and M4 is cutoff state makes OUT_p logic Low. OUTp is real value of the comparator. OUT_n is just inversion of the OUTp. In order to get a more accurate decision the output of the pre amplifier OUT_P is given to transistor M7 has shown in Fig. 5

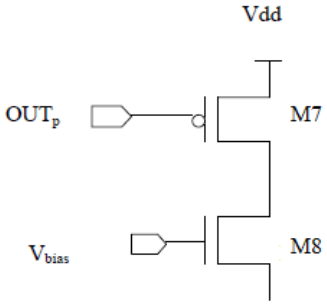

Fig. 5 Amplifier circuit

The output OUT_p is taken for the next stage of design of comparator. The OUT_p from the pre amplifier is taken and it is given to the PMOS M7 which act as pull up circuit that provides an exact logic '1'from the inputs. The biased NMOS transistor M8 is act as the pull down circuit which is give exact '0'. The circuit diagram is shown in the Fig. 5. A simple CMOS current mirror is also used in the proposed circuit shown in Fig. 6. The current mirror circuit is used in this comparator circuit because it provides a constant current independent of voltage applied such that the designed comparator works at a good speed irrespective of voltage supplied. Because of using current mirror circuit in this comparator the speed of the proposed circuit is high compared to the previous existing comparator circuit. The current mirror circuit is otherwise said to be independent ideal current source. The transistor M5 and M6 are identical NMOS transistors. Here the constant current I_{bias} i.e., the reference current is provided to the drain of M5 since the circuit named has current mirror output current at the drain of M6 is identical to input reference current. The current mirror circuit provides good biasing and plays vital role in the Analog Integrated circuit

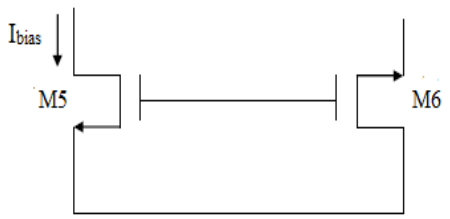

Fig. 6 Current mirror circuit.

Finally the comparator circuit ends with the output buffer which is mainly used for the Analog Integrated circuit to get a smooth output waveform. The function of the output buffer is to reduce the ripple in the output waveform. The

output buffer consist of two back to back connected inverter which can be used for two reason one to produce a smooth output waveform and second thing is produce a small delay. The output buffer is also capable of drive a variable load which is connected to the output of the circuit. The circuit diagram is shown in the Fig. 7.

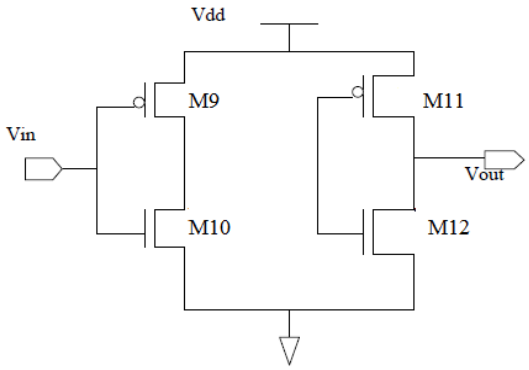

Fig. 7 Output buffer circuit

Thus the proposed comparator circuit consists of four main circuits 1. Pre amplifier circuit made of differential amplifier to provide difference of two voltages applied. 2. Amplifier circuit is added to provide an additional amplification required to take accurate decision by a comparator. 3. Current mirror circuit which is used to increase the speed of comparing operation. 4. Output buffer to provide a smooth of by eliminating the ripple in output waveform.

By connecting all these circuits together the proposed circuit. The proposed circuit is implemented in various CMOS families and their performances are measured to compare and find the best one among them.

IV. PROPOSED DESIGN IN DIFFERENT CIRCUIT FAMILIES

The CMOS families include many circuits among them this paper consider four major circuit 1. Static Complementary MOS circuit. 2. Ratioed circuit in which Pseudo NMOS circuit is considered here. 3. Dynamic circuit both footed and unfooted circuits are taken into consideration.

STATIC CMOS CIRCUIT

Static CMOS circuits can be abbreviated as SCMOS logic (Static Complementary Metal Oxide Semiconductor). From name it says that static which means no time varying component (Clock) involved in this circuit. Complementary indicates that NMOS transistor used in pull-down network is an exact opposite of PMOS transistor used in pull-up networks. The proposed circuit in SCMOS logic is shown in Fig. 8. [13] The SCMOS logic is preferred because it provides Low power consumption with finite speed, provides good noise margin and also easy to design.

The SCMOS logic of proposed circuit consists of preamplifier circuit made of differential amplifier. The output of differential amplifier is given to decision circuit which decides whether the exact logic high (VDD or 1) or logic low (ground or 0) has to be provided to output. The pull down network of the decision circuit is biased by the current mirror circuit. Whenever the input signal is greater than the reference DC signal the OUT_p becomes Logic low. The output OUT_p is given to decision circuit. The logic Low of OUT_p should be less than the v_{bias} provided by the current mirror circuit then M7 turn ON M6 turned OFF connecting VDD to the output. This output from the decision circuit is given to buffer made of back to back connected inverter provides Logic high (VDD or 1) to the output.

The exact opposite operation occur when the input signal is less than the reference DC signal the OUT_p becomes Logic high. The output OUT_p is given to decision circuit. The logic high of OUT_p should be thrice more than the v_{bias} provided by the current mirror circuit then only M7 turn OFF M6 turned ON connecting ground to the output. Thus the output from the decision circuit is given to buffer made of back to back connected inverter provides Logic Low (ground or 0) to the output.

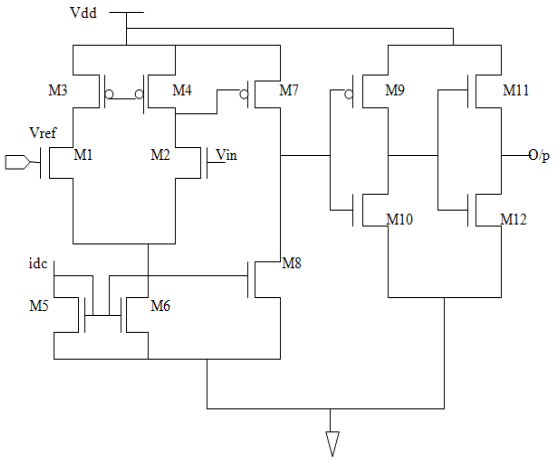

Fig. 8 SCMOS Configuration of proposed comparator

RATIOED CIRCUIT

A ratioed circuit in CMOS circuit families uses slightly weak pull-up network compared to that of pull-down network. The main purpose of ratioed logic is that the input capacitance is less compared to other CMOS logic families. Thus Ratioed logic has improved logical effort by eliminating large PMOS Pull up transistors loading the inputs, Ratioed circuits are not widely used because it require to find the exact ratio of pull up and pull down network to make them function correctly. The strength of pull up to pull down to chosen in such a way so that pull up network has less effect on pull down network during decision making. Suppose pull-up strength is too strong,

output becomes too high; so the low output does not turn ON the next stage. If the pull-up is too weak, the rising delay will be too slow. Ratioed circuits power dissipation is more compared to that of static when the output is low, because of these reason they are used in a limited application where they provide significant benefits.

Pseudo n-MOS

Pseudo NMOS is one type of ratioed circuit in which the pull-down network of the SCMOS remains the same, while the pull up network alone replaced by the single PMOS transistor with gate grounded. The Fig. 9 shows the Pseudo NMOS configuration of the proposed comparator circuit. [14] The grounded PMOS is always in turn ON condition. Whenever the pull down network dominates the pull up network i.e the input signal is less the reference signal the pull down network function making the output to logic Low. Otherwise the output is logic High. The width of PMOS transistor is selected to be ¼ the strength of the NMOS pull-down network which reduces noise with increase in speed; this best size is highly process-dependent, but is usually in the range of 1/3 to 1/6.

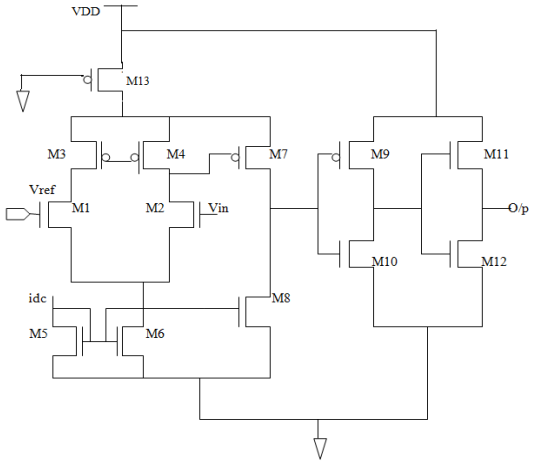

Fig. 9 Ratioed circuit configuration of proposed comparator

DYNAMIC CIRCUIT

The failure of ratioed circuits includes static power dissipation, non-zero output and slow rising transitions. Dynamic circuits neutralize these failures by using a clocked pull-up transistor rather than a PMOS which is in always ON condition. Dynamic circuit operation is divided into two modes.

One is precharge mode and second is evaluate mode. Since dynamic logic circuits operates under influence of cloak the two differ with the clock applied to the circuit. During negative half cycle of the clock input the pull network is turned ON such that the output is supplied with logic high output. This phase of the clock is said to be precharge i.e, whatever logic the output during negative half cycle of the clock the output becomes logic High.

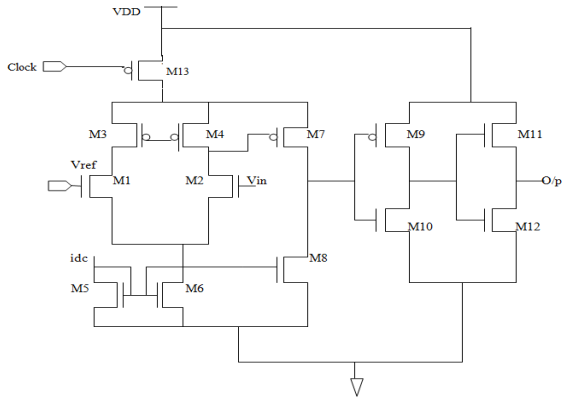

Fig. 10 Dynamic configuration of the proposed comparator

During positive cycle of the clock input pull up network turn OFF based on the logic in the pull down network the output may get pulled logic Low or its remains in logic High. Thus only one evaluation occur during evaluation phase. For the next evaluation to occur the precharge has to be done. The dynamic configuration of the proposed circuit is shown in Fig. 10. The main advantage of dynamic circuit is speed is very high by increasing the frequency of the clock signal applied the operation speed can be increased.[15] Dynamic footed circuit has both pull up and pull down network connected to clock input. Thus the extra pull down transistor in dynamic circuit is called a foot. The dynamic footed configuration of the proposed comparator circuit is shown in Fig. 11

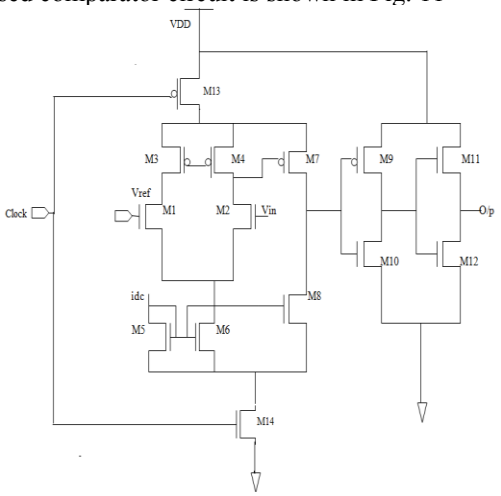

Fig. 11 Dynamic footed configuration of proposed comparator

V. EXPERIMENTAL RESULTS

The proposed comparator circuit is implemented using cadence 180nm CMOS technology and the spectre tool is utilized for simulation, The simulated results of proposed dynamic comparator is shown in Fig. 12. Here the input signal of 1.25V and the reference signal of 500mV is

applied to proposed circuit. The proposed comparator is examined for power and delay variation. The result of the various logic families has been tabulated and compared. The comparison of various logic families has been shown in the table I

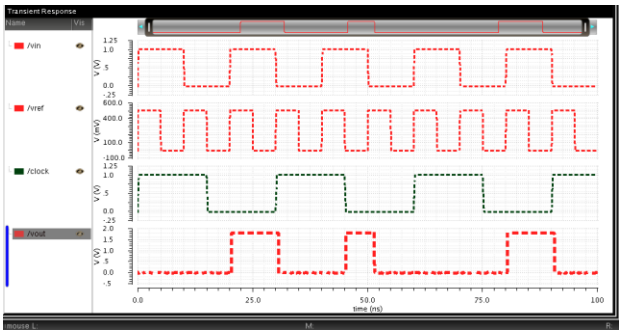

Fig. 12 simulation result of dynamic comparator

VI. COMPARITIVE ANALYSIS

Table I Summary of Comparator analysed in Different Logic Families

	Static Circuit	Ratio Circuit	Dynamic Unfooted Circuit	Dynamic Footed Circuit
TRANSISTOR LENGTH (nm)	180	180	180	180
TRANSISTOR WIDTH (nm)	720	720	720	720
POWER AVERAGE (µW)	65.23	63.99	51.3	56.13
DELAY (ps)	195	193.8	207.8	654

Power supply should be in the range 1.2 to 1.8 V

VII. CONCLUSION

In this paper it is concluded that the proposed comparator circuit in various logic families has been implemented and simulated using cadence virtuoso CMOS technology in which the transistor of length 180nm and width of 720nm be used. The power supplied to circuit has been reduced to the range 1.2V to 1.8V. Through the usage of current mirror power dissipation and delay has been reduced as much as possible. The buffer provides good smoothened output and load bearing capacity. From the comparison table, it is concluded that the proposed dynamic un footed circuit shown it best performance. The reason for choose it because it could do both sampling and quantization, a 1-bit analog to digital converter be designed. In further it is planned to prepare a layout for the proposed comparator IC and check the same performed is obtained after post layout simulation.

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