Transistor Gating: Reduction of Leakage Current and Power in Full Subtractor Circuit

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***Abstract*— In this paper low-power design techniques proposed to minimize the standby leakage power in nanoscale CMOS very large scale integration (VLSI) systems by generating transistor grating technology. In low-power design for circuit to reduce the power supply voltage and this requires the transistor threshold voltages to also be reduced to maintain throughput and noise margins., this increases the subthreshold leakage current in p and n MOSFETs. this begins to increase the overall power in digital circuits. How-ever, this increases the subthreshold leakage current of p and n MOSFETs, which starts to set the power savings obtained from power supply reduction. In transistor grating technology two sleep transistors PMOS and NMOS are inserted in between the supply voltage and ground. A PMOS is inserted in between pull-up network and network output and a NMOS is inserted in between pull-down network and ground. During standby mode both sleep transistor are turned off. By applying this technique reduction in leakage current is 17.58% and power is 24.38% .The tool used is CADENCE VIRTUOSO for schematic simulation. The simulation technology used is 45nm.**

Keywords- CMOS; leakage current; low power; transistor grating; Full subtractor;

I. INTRODUCTION

In recent years, power consumption has become a critical design concern for many combinational circuit systems. the advantages of complementary metal-oxide semiconductor(CMOS) over competing technologies, such as transistor - transistor logic (TTL) and emitter coupled logic (ECL), has been its lower power dissipation [8]. to the growing need for low-voltage ,high-performance, low-leakage systems, a variety of leakage-control techniques have been developed. Some depend on the use of multiple-threshold voltages. Low-threshold transistors are used to improve performance. High-threshold devices are then used for leakage control. Multiple threshold CMOS (MTCMOS) [1], [2] isolates low-threshold circuits from power and ground rails using high-threshold devices. Lowering the supply voltage is the most effective way to achieve low-power performance because power dissipation in digital CMOS circuits is approximately proportional to the square of the supply voltage. From the point of view of applications to battery-powered mobile equipment, the supply voltage should be set at 1 V [4]. chip designers have relied on scaling down the transistor supply voltage in subsequent generations to reduce the dynamic power dissipation due to a much larger number of transistors on chip. Maintaining high transistor switching speeds, however, requires a commensurate down-scaling of the transistor threshold voltage giving rise to a significant amount of leakage power dissipation even when the transistor is not switching.

But as technologies scales down to the nanometer regime (Ultra Deep Sub-Micron (UDSM)), the dynamic power dissipation becomes more lagging than the static power consumption. And despite the aggressive downscaling of device dimensions and decreasing the supply voltages, which decrease the power consumption of the single transistor, with exponential increase of operating frequencies results in a steady increase of the overall power consumption. With downscaling technology, interconnect resistance and capacitance increase the propagation delay.

The two main effects that contribute to the total power dissipation on a chip are the active and static power dissipation. The expression to compute the total power is as follows

$$T_{total} = P_{dynamic} + P_{sc} + P_{static} \quad (1)$$

Dynamic dissipation power occurs when a transistor switches state and is due to capacitive charging and discharging associated with the output wiring. A small proportion of dynamic power arises from the short-circuit current that flows momentarily while the complementary devices (push/pull) in a circuit are simultaneously conducting during a change in the output state. The dynamic power consumption (*Pdyn*) is given by

$$P_{dyn} = Kcv^2_{dd}f_{sw} \quad (2)$$

Where

k = technology factor,

C = capacitance of switching nodes,

Vdd = supply voltage and fsw is the effective switching frequency.

While which leads to short-circuit power dissipation (Psc) and given by

$$P_{sc} = I_{sc} . V_{dd} . t_s f_{sw} \quad (3)$$

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Where

Isc = short circuit current,

ts = switching delay.

In Nano CMOS circuits, Sub-threshold and Gate Leakage currents are proven as the dominant factors in deciding the Static Power and contribute significantly to overall power consumption. Sub threshold or weak inversion conduction current between source and drain in a MOS transistor occurs when gate voltage is below the transistor threshold voltage. The Sub threshold or weak inversion current I_{ds} can be expressed as:

$$I_{ds}=I_{dso}\, e^{V_{gs} - V_t / nvT} [1 - e^{-V_{ds}/V_T}] \quad (4)$$

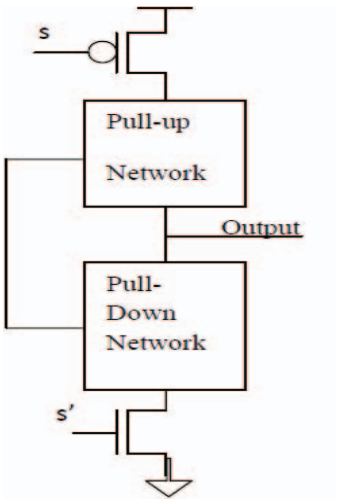
$$I_{dso} = \mu_{eff}\, c_{ox} (W/L) V_T^{\,2} \quad (5)$$

Where μ_{eff} is the charge carrier mobility, C_{ox} is the gate capacitance /unit area, W/L are width to length of channel ratio respectively, V_t is the threshold voltage, V_T is the thermal voltage, n is the sub-threshold swing coefficient, V_{gs} is the transistor gate to source voltage and V_{ds} is the drain to source voltage. Transistor gating proposed technique has been defined, in this technique we used two sleep transistors NMOS and PMOS are inserted in the circuit. The PMOS sleep transistor (S) is added in between the pull-up network and network outputs and NMOS sleep transistor (S') is added in between the pull-down network and ground. This technique applied on full subtractor circuit.

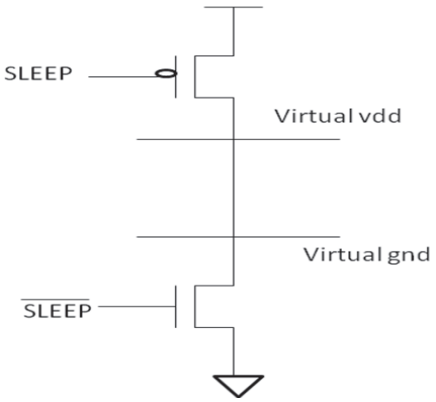
II. REVIEWS OF PREVIOUS WORK

This section reviews different approaches for sub-threshold leakage current reduction techniques. A technique for leakage power control is Power gating [2][3], which turns off the devices by cutting off their supply voltage. Power gating uses low-leakage PMOS transistors as header switches to turn off power supplies to parts of a design in standby or sleep mode. NMOS as footer switches can also be used as sleep transistors. Inserting the sleep transistors divides the chip's power network into pull up network connected to the power supply and a pull down network that drives the cells and can be turned off. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To turn off the block for small intervals of time, internal power gating is more appropriate. CMOS switches which provide power to the circuit are controlled by power gating controllers.

The multi threshold CMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for well-organized power management. Second, two dissimilar threshold voltages are used for N channel and P channel MOSFET in a single chip [10]. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt).



Power gating technique



MTCMOS technique

III. IMPLEMENTATION OF FULL SUBTRACTOR

A full subtractor is a combinational circuit that performs a subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs such as A, B and C denotes the inputs, difference and borrow are outputs respectively.

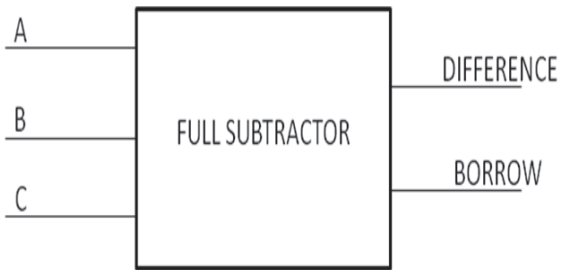


Figure 1. symbol of full subtractor

The two outputs represent the difference and borrow, respectively. The symbolic circuit for full subtractor is shown in Figure. The truth table for full subtractor is shown below.

TABLE1-TRUTH TABLE 1OF FULL SUBTRACTOR

A	B	C	DIFFERENCE	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The simplified logic equations from truth table are

$$DIFFERENCE = A'B'C + A'BC' + AB'C' + ABC$$

$$BORROW = A'B'C + ABC + A'B$$

Where A, B, C are the inputs. Outputs are denoted by difference Y and borrow as shown in waveform of full subtractor.

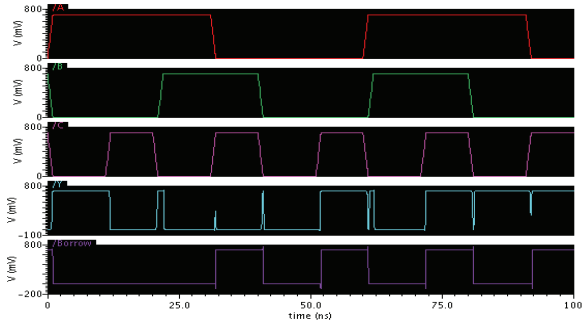


Figure 2. waveform of full subtractor

IV. PROPOSED TECHNIQUE ON FULL SUBTRACTOR

In this paper a new technique of leakage reduction - "TRANSISTOR GATING TECHNIQUE" has been demonrasted. In this technique leakage current is reduced by inserting extra sleep transistors between power supply and ground. A PMOS sleep transistor (s) is inserted in between pull-up network and the network output and an NMOS sleep transistor (s') is inserted in between the pull-down networks and the ground as shown in "Fig.3"

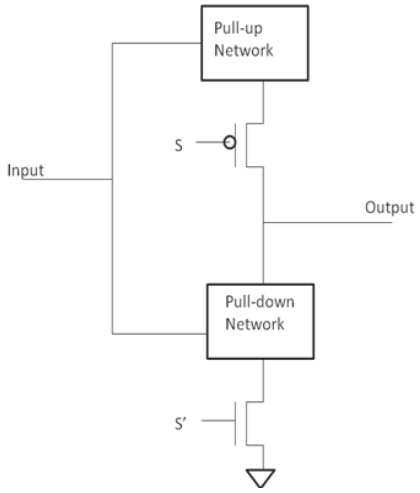


Figure 3. Transistor gating technique

In active mode, both sleep transistors are turned on by applying the gate input voltage i.e. high (0.7v) for NMOS and low (0v) for PMOS, to reduced the resistance of the conducting paths from power supply to ground, thereby reducing performance. Both sleep transistors are turned off during standby mode by applying the gate input voltage i.e. low (0v) for NMOS and high (0.7v) for PMOS which reduces leakage current by increasing resistance of the path from power supply .to ground.

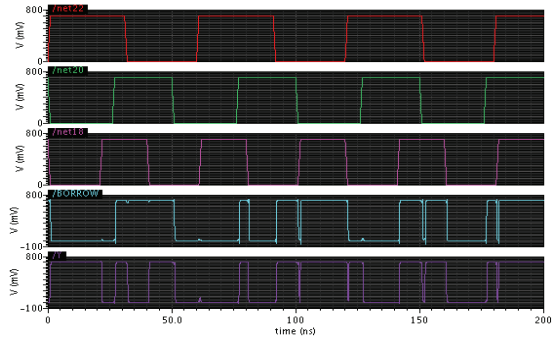


Figure 4. waveform of proposed full subtractor

V. SIMULATION RESULT

In this paper we analyze reduction of leakage on the Full subtractor under the influence of transistor gating technique in nanometer CMOS technology. Here the Full subtractor circuit is simulated using cadence simulation tools in 45nm CMOS technology. In 45nm technology when supply voltage is applied on full subtractor is 0.7V, leakage current & leakage power is reduced by17.58% and 24.38%.

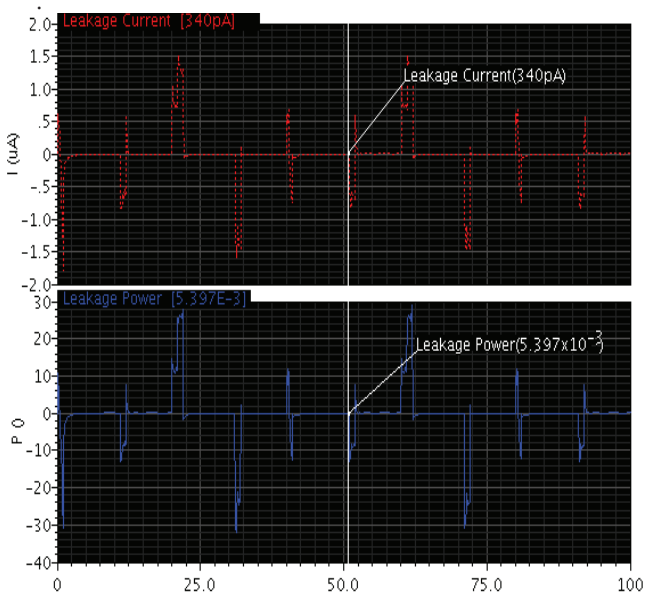


Figure 5. waveform of leakage current and power

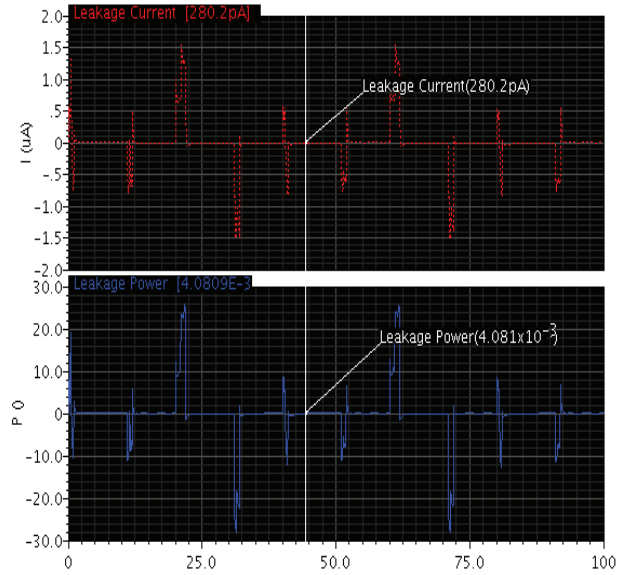


Figure 6. Waveform of proposed leakage current and power

VI CONCLUSION

In this paper we proposed a transistor gating technique that reduces the power dissipation of the full subtractor. CMOS technology improves the performance and reduces power consumption. From the simulation result it is cleared that after applying this technique we have reduced17.58 % in leakage current and 24.38 % in leakage power. Simulation of results for full subtractor is done by Cadence simulation tool in 45nm CMOS technology at 0.7 supply voltage.

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