8-Bit, 2 MSPS, 1.8 V Pipelined Analog-to-Digital Converter with Digital Error Correction Circuit for Data Communication

N. Idros, ZAA. Aziz, A.Rosli
Collaborative Microelectronic Design Excellence Centre (CEDEC)
Sains@USM, Level 1, Block C, No 10, Persiaran Bukit Jambul, 11900 Bayan Lepas, Pulau Pinang, Malaysia
miza_kakcik@yahoo.com, eezulfiq@usm.my, aliarosli@outlook.com

***Abstract* − This paper presents the design of 8-bit pipelined analog-to-digital converter (ADC) with digital error correction circuit operates at the sampling frequency of 2 MHz. This work is implemented by 1.5-bit slice for the first 7-stages and followed by a simple flash ADC. Each 1.5-bit slice comprises a 2-bit comparator, a logic circuit and a residue amplifier. The residue amplifier consists of an operational amplifier with a gain-boosting technique to boost the overall open-loop DC gain. The technique incorporates isolation of the input differential pair by a pair of NMOS devices and a pair of OTA at the cascode stage of the core amplifier. Each stage provides 2-bit digital code that is aligned and added by the digital error correction circuit after all the operations complete. The conversion for the differential analog input is ranging from ±900 mV. Post layout simulation results show that, the ADC is able to work functionally at 8-bit resolution with differential non-linearity (DNL) and integral non-linearity (INL) errors, ±0.5 and ±2 LSB, respectively. The ADC consumes 32 mW for the conversion. The dimension of the layout is 1800 µm × 800 µm and is fabricated using Silterra 0.18 µm CMOS process technology.**

Keywords − ADC, pipelined architecture, medium resolution, gain-boosting technique

I. INTRODUCTION

Nowadays, mobile communication is moving towards electrical devices with high speed and lower power dissipation. Bluetooth system is one promising wireless technology for connecting digital equipment such as mobile computers, handheld devices and mobile phones worldwide. Bluetooth enables the communication between those equipment and makes information transmission more efficient [1].

Analog-to-Digital Converter (ADC) is an important device for interfacing analog signal before computers can process it digitally for various purposes. This is because analog signal is more difficult to be measured or verified directly [2]. Apart from that, data processing is more convenient to be done in digital domain.

High speed medium accuracy ADC is widely used for application in data communication, specifically adoption in Bluetooth application. Considering such application, pipelined architecture is the most suitable among the available architectures [3]. More time can be saved since pipelined ADC enables the operation to take place concurrently. The MSB and LSB parts implement the concept of 1.5-bit slice and flash ADC, respectively. Pipelined architecture results in high throughput rate from the concurrent operation of stages [4].

This paper discusses the architecture of pipelined ADC that uses an operational amplifier with gain-boosting technique as the core element. The operational amplifier is designed to have a very high open-loop DC gain and high unity gain frequency in order to achieve high accuracy and fast settling requirements [5]. However, both requirements lead to contradictory demands; hence, an operational amplifier with gain enhancement technique is to be implemented. The technique incorporates isolation of the input differential pair by a pair of NMOS devices and a pair of OTA at the cascode stage of the core amplifier.

The organization of this paper is as follows. Section II presents the design specifications in designing the pipelined ADC. Section III explains the working principles of pipelined ADC. Section IV describes the implementation of the designed pipelined ADC. In Section V, the post layout result is discussed. Finally, conclusion is made in Section VI.

II. DESIGN SPECIFICATIONS

The amplifier must amplify signals within 0.5 LSB of the ideal value [5] in the case of 8-bit resolution. The closed loop gain, A_{CL} of the amplifier is defined by (1);

978-1-5386-7269-3/18/$31.00 ©2018 IEEE

$$A_{CL} = \frac{AOL}{1+\beta A_{OL}} \quad (1)$$

where β and A_{OL} are the transconductance and open-loop DC gain, respectively.

The minimum open-loop DC gain required can be determined by (2);

$$|A_{OL}| \geq 2^{N+2} \quad (2)$$

The minimum unity gain frequency, f_u of the operational amplifier is given by (3);

$$f_u = \frac{f_{clk} \bullet ln 2^{N+1}}{2\pi\beta} \quad (3)$$

By assuming β = 0.5, (3) becomes (4);

$$f_u \geq 0.22\ (N+1)\ f_{clk} \quad (4)$$

where N is the number of bit of the pipelined ADC.

III. Methodology

Pipelined ADC is composed by 7-stages of 1.5-bit slice and a simple flash ADC. The injected differential input signal is ranging from ±900 mV. 2-bit output code generated at each stage is aligned at certain period and added by a digital error correction circuit to produce the real 8-bit digital code.

A. 2-bit Comparator

The fundamental task of the comparator is to amplify a big or small difference between its input terminals into a digital decision. The comparator is built with input differential pair where the difference is formed between the input value and the reference value. The differential pair is important to create some tolerance for the common-mode level of the input signal [6].

Differential input signal is injected to the source of nMOS devices in the switched-capacitor circuit before connecting to the comparator. The switched-capacitor circuit works at two different clock phases, p_1 and p_2 to fix the input voltage at a certain referenced point.

Each comparator, also known as a simple flash ADC, put together by preamplifier, latch and buffer [7], and generates 1-bit digital code. The operation takes place following the conditions in Table I.

TABLE I. Specification of the Comparator.

Differential Input Signal	Out_1	Out_0
Input < Reference voltage	0	0
- Reference voltage < Input ,< Reference voltage	0	1
Input > Reference voltage	1	1

B. Logic Circuit

Logic circuit, as displayed in Fig 1, comprises several digital gates that are derived from Table II. This circuit acts as switches receiving digital inputs from the comparator to enable the residue amplifier to operate. The logic's function is specified in Table II. 2-bit output, BIT[1:0] is the digital code generated at each stage based on the analog input injected at the current stage.

TABLE II. Specification of the Logic.

Input Out [1:0]	Outputs				
	BIT [1:0]	SRG3	SRG2	SRG1	SRG0
00	00	1	Ph2	0	Ph1
01	01	1	0	0	1
11	10	Ph1	0	Ph2	1

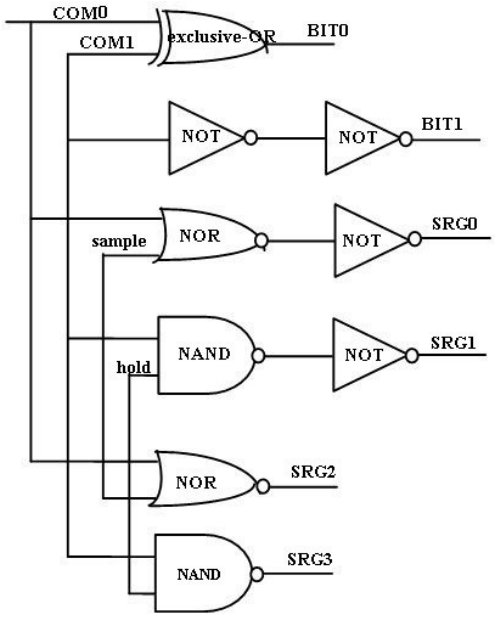

Fig 1: Logic Circuit.

C. Residue Amplifier

Residue amplifier is made up of an operational amplifier and switched-capacitor circuits, as illustrated in Fig 2. The residue amplifier works at two different phases, which are conducting and isolating phases. During the conducting phase, which is the switches S1 and S1' are closed, the signal on the capacitor follow the input signal, Vin+ and Vin-, while in the isolating phase, which is the switches S4 is closed, the signal level remains constant at its level at the moment of opening the S1 and S1' [6]. The operation takes place is based on the specifications in (5);

$$V_{out} = \begin{cases} 2Vin - Vref & ; \quad Vin \geq \frac{Vref}{2} \\ 2Vin & ; \quad -\frac{Vref}{2} \leq Vin \leq \frac{Vref}{2} \\ 2Vin + Vref & ; \quad Vin \leq -\frac{Vref}{2} \end{cases} \quad (5)$$

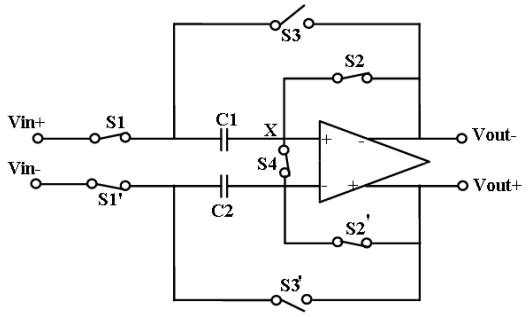

Fig 2: Residue amplifier.

Operational amplifier at the middle of the residue amplifier is the main element in building the pipelined ADC. This design incorporates fully differential inputs and outputs. The amplifier employs NMOS input differential pair for the purpose of achieving high gain and speed. Folded cascode topology is chosen for this work due to its high output swing [8]. Nevertheless, the implementation of common-mode feedback (CMFB) circuit is crucial due to the choice of folded cascode topology.

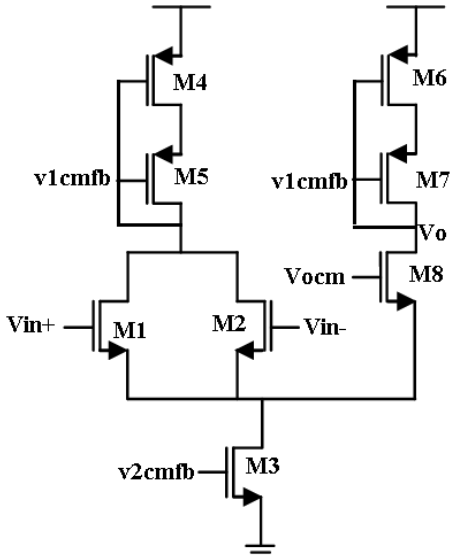

Fig 3: Common-mode feedback circuit.

Fig 3 illustrates the continuous-time CMFB realized in this work. Based on Fig 3, the input NMOS devices, M1 and M2 are assumed to operate in saturation region. They sense and amplify the common-mode signal only, ideally. The use of feedback between the CMFB circuit and operational amplifier enables the V_O and V_{OCM} to be equal. This task is accomplished by applying the V_O to a suitable internal node of the operational amplifier, basically to the node Vb2 of the main amplifier in Fig 4.

Fig 4 presents the overall amplifiers to be implemented in this work. The main amplifier provides high unity gain frequency whereas the pair of NMOS devices, M2 and M3 and the amplifiers, P1 and P2 at the cascode stage improve the open-loop DC gain without affecting the frequency behaviour. The employment of M2, M3, P1 and P2 enhance the overall open-loop DC gain, in a way of increasing the overall effective output resistance, R_{out}. Apart from that, the isolation by the NMOS devices is for the purpose of isolating the differential pair M4 and M5 from their current source loads formed by the PMOS devices, M0 and M1 [9][10].

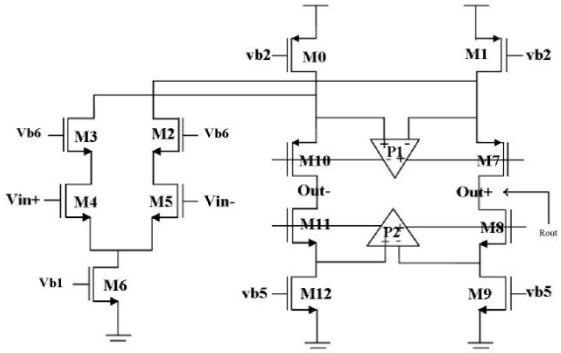

Fig 4: Operational amplifier with gain-enhanced amplifiers.

Adding M2 and M3 into the circuit introducing the resistance, R_{O2} or R_{O3}. Including M2 or M3 into equation, R_{out1} can be derived into (6);

$$R_{out1} = G_{M7} R_{O7} (R_{O1} \parallel R_{O2}) \parallel G_{M8} R_{O8} R_{O9} \quad (6)$$

Fig 5 illustrates the idea of gain-enhanced amplifier to be implemented at the cascode stage of the main amplifier. It is based on negative feedback loop to set the drain voltage of M1. Negative feedback drives the gate of M1 until V_X has the same value as V_{ref}, where V_X and V_{ref} are the voltage at the positive and negative inputs of the additional amplifier, respectively. Therefore, the variation of V_{out} has much less effect on V_X because of the gain-boosting amplifier. Due to that, variation of Vout has less effect on V_X. The almost constant value of V_X contributes to the less sensitivity of the output current, I_{out} to the V_{out}. Hence, the output impedance, R_{out2} can be defined by (7);

$$R_{out2} = [G_{M1} \bullet R_{O1}(A+1)+1]R_{O2} + R_{O1} \quad (7)$$

(7) can be reduced to (8);

$$R_{out2} \approx A \bullet G_{M1} \bullet R_{O2} \bullet R_{O1} \quad (8)$$

By now, the R_{out} is derived from R_{out1} and R_{out2}, as indicated in (9);

$$R_{out} = [A_{P1} G_{M7} R_{O7} (R_{O1} \parallel R_{O2})] \parallel (A_{P2} G_{M8} R_{O8} R_{O9}) \quad (9)$$

Due to the increment of the R_{out}, the overall open-loop DC gain of the amplifiers is increased, as indicated in (10);

$$A_V = G_{M5} \{[A_{P1} G_{M7} R_{O7} (R_{O1} \| R_{O2})] \| (A_{P2} G_{M8} R_{O8} R_{O9})\} \quad (10)$$

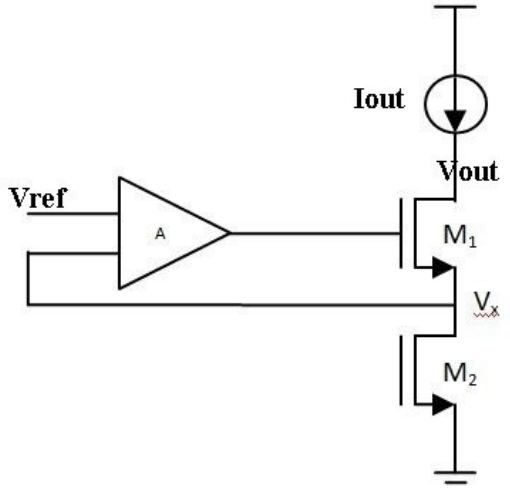

Fig. 5: Cascode stage with gain-boosted amplifier.

Switched-capacitor circuit functions to receive the digital codes from the previous block for the residue amplifier to do the operations specified in (5), depending on the voltage level of the current analog signal.

D. Pipelined Stages

Fig 6 depicts the pipelined stages for 8-bit ADC. Seven blocks of 1.5-bit slices are arranged in series to develop the pipelined ADC. Similar operation takes place at each stage except at the 8th-stage. The 8th-stage is made up of a flash ADC. The operation of the subsequent stage takes place after the output of the current stage is available. This process is delayed by half cycle from the previous stage. In short, the availability of the digital code at each stage is at different time.

E. Digital Error Correction (DEC) Circuit

DEC circuit receives 2-bit digital code generated by each pipelined stage. The 2-bit code splits into 1.5-bit and 0.5-bit, in which each represents the real digital code and the offset of each stage, respectively. This circuit is made up of arrays of D flip-flops and adders. The D flip-flops act as delay to align the digital codes generated by each 1.5-bit slice at certain time before they are added to realize the final 8-bit digital codes. The addition process done by the adders is from the final stage followed by the previous stage starts from the LSB until the MSB of the first stage. Fig 7 displays the implemented DEC circuit.

IV. Design Implementation

Pipelined ADC is constructed by 7-stages of 1.5-bit slice and a simple flash ADC, as depicted in Fig 8. Fig 9 shows the physical representation of the constructed pipelined ADC. All the biased voltages and clock frequencies are injected directly from the power source. The total area of the layout is 1800 µm × 800 µm and is fabricated using Silterra 0.18 µm CMOS process technology.

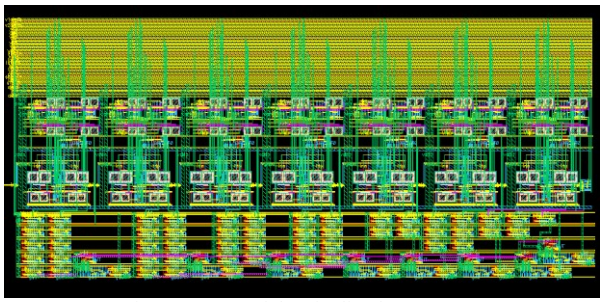

Fig. 9: Layout of the pipelined ADC.

V. Post Layout Simulation Results

The ADC is simulated in Silterra 0.18 µm CMOS process technology at the sampling frequency of 2 MHz. The first available digital data can be collected at 2.75 µs. The performance is depicted in Fig 10 and Table III. Based on Fig 10, the pre-layout and post-layout simulations' result is overlapping to each other. This proved that, the designed ADC is able to do the conversion properly at 8-bit resolution, with differential non-linearity (DNL) and integral non-linearity (INL) errors ±0.5 and ±2 LSB, respectively and consumed 32 mW for the conversion. For the digital data that contribute to the DNL error, this condition is resulted because of the amplifiers work at the edge of the saturation region, in which is close enough to the linear region. Nonetheless, the data conversion takes place without the DNL error and missing code as the amplifiers work stably in the saturation region.

Table III: Summary of Performace of the ADC.

Parameter	Typical Value	Unit
Resolution	8	Bit
DNL	±0.5	LSB
INL	±2.0	LSB
Sampling frequency	2	MHz
Static Power Consumption	32	mW

VI. Conclusion

8-bit pipelined ADC was designed by implementing the operational amplifier with gain-boosting technique as the core element. A DEC circuit is constructed to ensure the accuracy of the realization of the final 8-bit digital data. The post layout result showed the ADC worked functionally with for the differential analog signal ranging from ±900 mV. This ADC consumed 32 mW for the conversion. The full layout dimension was 1800 µm × 800 µm.

ACKNOWLEDGMENT

The research is supported by Talent Corporation Malaysia under the 3D (Demand, Driven, Development) Program collaborated with the industries and public universities of Malaysia.

REFERENCES

[1] P. Bai, J. Li, Y. Li, and X. Duan, "Application of Mobile Bluetooth Based on Human Physiological Parameters Wireless Sensor," in *2016 IEEE International Conference on Consumer Electronics-China (ICCE-China)*, 2016, pp. 1-3.

[2] M. B. Labhane and P. Palsodkar, "Various Architectures of Analog to Digital Converter " in *IEEE ICCSP 2015*, 2015.

[3] L. Weitao, L. Fule, Y. Changyi, L. Shengjing, and W. Zhihua, "An 85mW 14-bit 150MS/s Pipelined ADC with a Merged First and Second MDAC," *China Communications,* pp. 14-21, 2015.

[4] S. H.Lewis and P. R.Gray, "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits,* 1987.

[5] N. B. Mukahar and S. H. B. Ruslan, "A 93.36 dB, 161 MHz Gain Improved CMOS OTA for a 16 Bit Pipeline Analog to Digital Converter," in *International Conference on Science and Social Research (CSSR 2010)*, Kuala Lumpur, Malaysia, 2010.

[6] P. Marcel J.M., *Analog-to-Digital Conversion*: Springer Dordrecht heidelberg London New York, 2010.

[7] K. R. Kiran, A. Kumar, and A. S. Reddy, "A 5-bit, 0.08mm2 Area Flash Analog to Digital Converter Implemented on Cadence Virtuoso 180nm," in *International Conference on Emerging Trends in Engineering, Technology and Science (ICETETS), 2*016.

[8] I. S. Ishak, S. A. Z. Murad, M. F. Ahmad, and N. S. Chin, "Design of Folded Cascode Operational Amplifier (Op-Amp) with Common-Mode Feedback (CMFB) for Pipeline ADC," in *Proceedings of Malaysian Technical Universities Conference on Engineering & Technology (MUCET)*, Kuantan, Pahang, 2013.

[9] Z. Ali and A. Marzuki, "Residual Folding Technique Adopting Switched Capacitor Residue Amplifiers and Folded Cascode Amplifier with Novel PMOS Isolation for High Speed Pipelined ADC Applications," pp. 14-17.

[10] M. C. H. Cheng, "Cascoded Differential Pair Amplifier with Current Injection for Gain Enhancement," 1998.

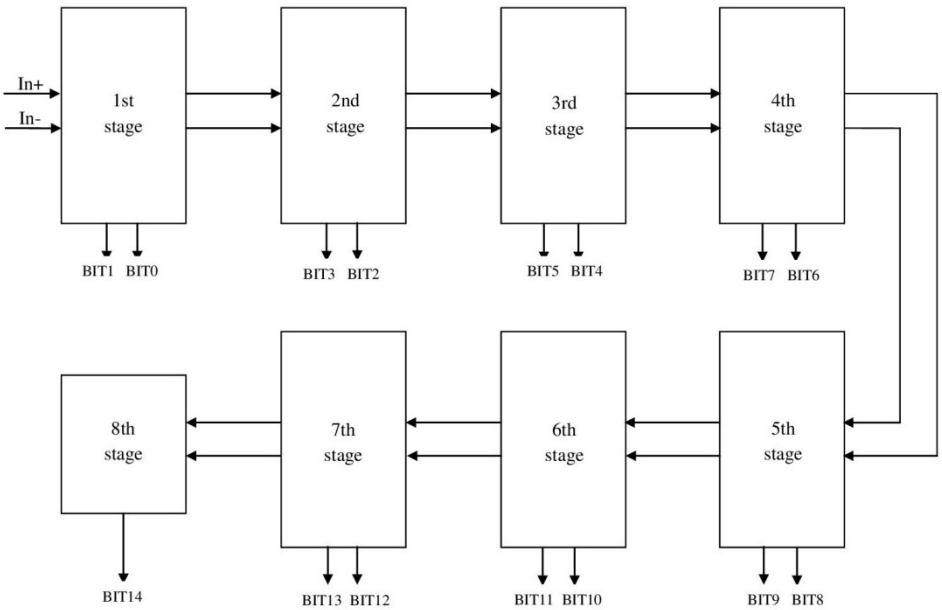

Fig 6: 8 stages of pipelined ADC.

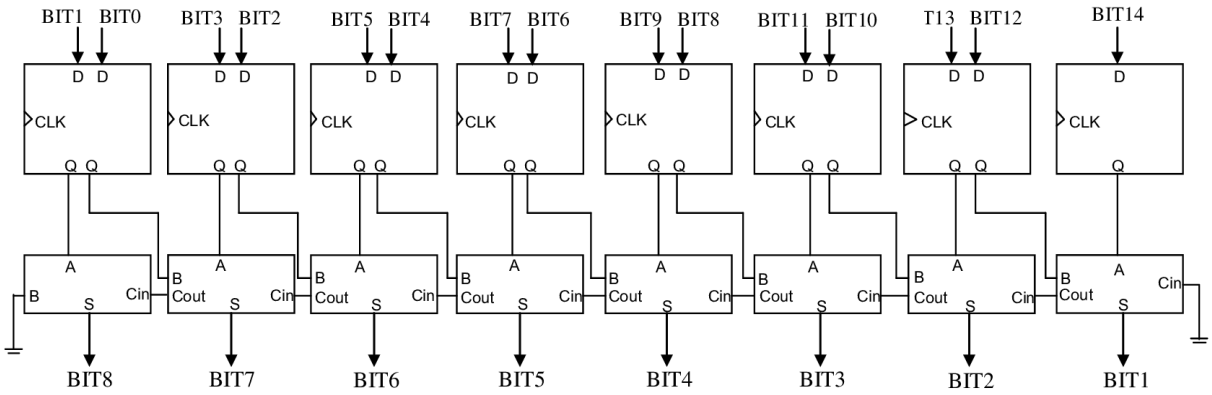

Fig 7: D flip-flops and adders in DEC circuit.

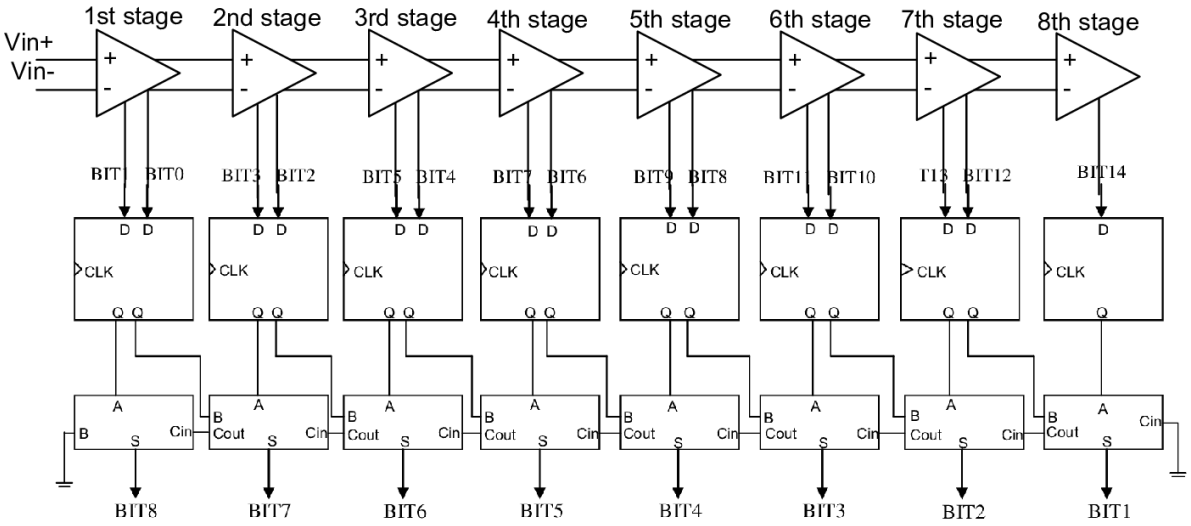

Fig 8: 8-stages of Pipelined ADC with DEC Circuits.

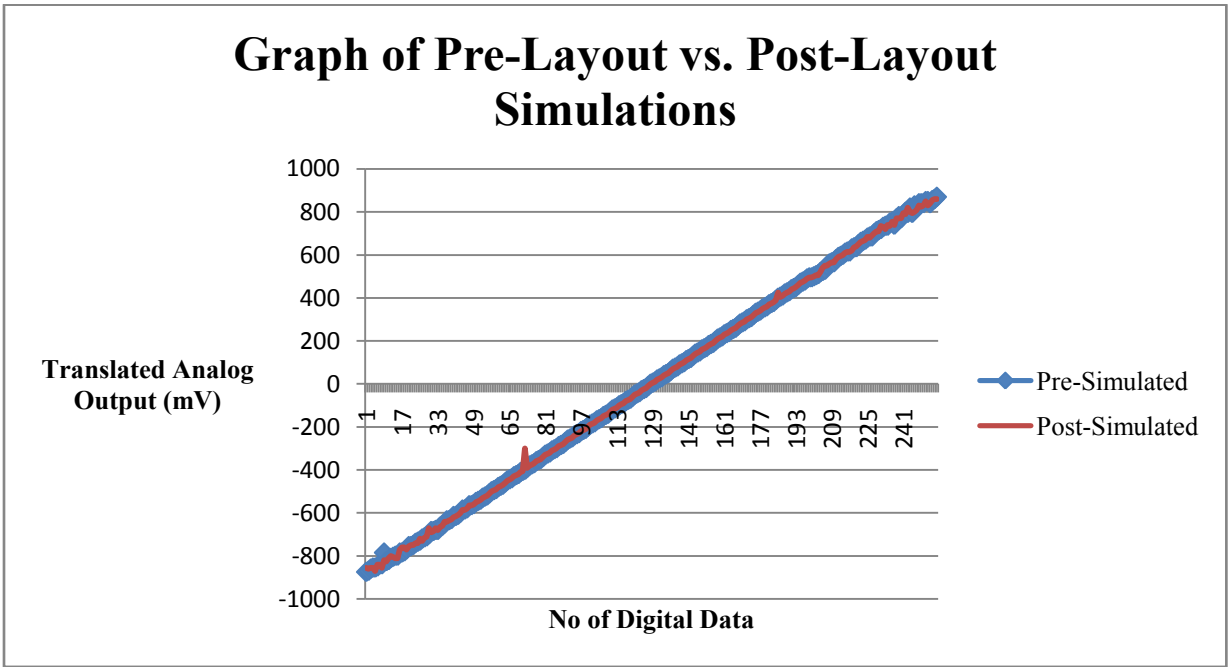

Fig 10: Pre and Post Layout Simulation Results.