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by Anu .Gupta

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8-BIT PIPELINE ANALOG TO DIGITAL CONVERTER

Submitted in partial fulfilment of the requirements of

BITS G540 Research Practice

by

Nazil Muhammed(2023H1230173P)

Abhijeet Singh(2023H1230163P)

Mayank Latke(2023H1230171P)

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Under the supervision

of Dr. Anu Gupta

Professor

Electrical and Electronics Department

10

BITS Pilani (Pilani Campus)



**BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE PILANI,
PILANI CAMPUS**

CERTIFICATE

This certifies that the work completed by Nazil Muhammed (2023H1230173P), Abhijeet Singh (2023H1230163P), and Mayank Latke (2023H1230171P) under my supervision is included in the report titled "8-BIT PIPELINE ANALOG TO DIGITAL CONVERTER," which was submitted to fulfil the requirements of BITS G540 Research Practice.

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Designation

Abstract

As a matter of fact, we are aware that digital signals provide the benefits of simpler processing, analysis, and storage. For processing, we therefore transform the analog signal to a digital signal.

Using the analog to digital converter as the interface will allow us to realize this. Consider an optical mouse as a basic example. Light is reflected from the radiation component when it reaches the desktop. The Image Sensor finally picks it up. The output voltage will now be produced based on the amount of reflected light. An analog signal is what this type of output voltage is. The signal is then converted to a digital format that DSP can process using the ADC. LNA amplifies the received signal in the Ultra-Wideband Wireless Transceiver System.

After that, mixers down convert this wideband signal. ADC processes the baseband signal after autocorrelation and integration. The outcome is the conversion of the analog signal to a digital signal. In this thesis, an ADC is created to meet specific specifications for converting baseband signals to digital signals.

Acknowledgements

I have been eager to express my gratitude to all those who helped me complete the research for my doctorate, and this is the perfect opportunity. In this context, the Department of Electrical and Electronics at BITS Pilani and my esteemed supervisor, Prof. Dr. Anu Gupta, instantly come to mind. They really have been my compass. My heartfelt thanks and appreciation go out to them for their perceptive advice, invaluable suggestions, keen interest, constructive criticism, and steadfast support during the current study. Beyond just academics, they taught me a lot about other facets of life. Since the beginning of this project until it was completed and put into this thesis, I have truly valued their continuous cooperation, for which I am quite grateful.

BITS Pilani
2024

Nazil Muhammed
Abhijeet Singh
Mayank latke

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Chapter 1: Introduction

The Importance of ADCs in a Digital World

24 Analog-to-Digital Converters (ADCs) are essential components that bridge the gap between the physical world (analog signals) and the digital world (computer-based signals). With the ever-growing use of digital processing in communication, instruments, factories, and image technology, the need for ADCs is rapidly increasing. Modern electronics are heavily reliant on digital components and processing, making ADCs even more critical.

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Pipeline ADCs: A Powerful Solution

This project focuses on a specific type of ADC called a pipeline ADC. This design offers three key advantages: low power consumption, high accuracy in representing analog signals, and fast conversion speed. These features make pipeline ADCs ideal for applications where power efficiency is a major concern, such as wireless communication systems.

Project Details: Building an 8-bit ADC

This project uses Cadence Virtuoso, a popular software tool for designing electronic circuits, to create an 8-bit pipeline ADC. The design leverages 180nm CMOS technology, a common method for building integrated circuits. Operational amplifiers (Op Amps) are a fundamental building block within the pipeline architecture, and the entire design will likely operate with a 1.8V power supply.

Objective

The goal of designing a 8-Bit pipeline ADC is to carefully plan its design, connections, and performance to ensure they meet performance standards. The expected results are good and fast while reducing power consumption. The main goal is to design efficient 100Msps 8-bit Pipeline ADC. This process has enabled the design of reliable and efficient 8-Bit pipeline ADC that can be used for implementation in IOT applications, Wireless Communication, Optical Communication, High Frequency Data collection.

Below is the image of N-bit Pipeline ADC.

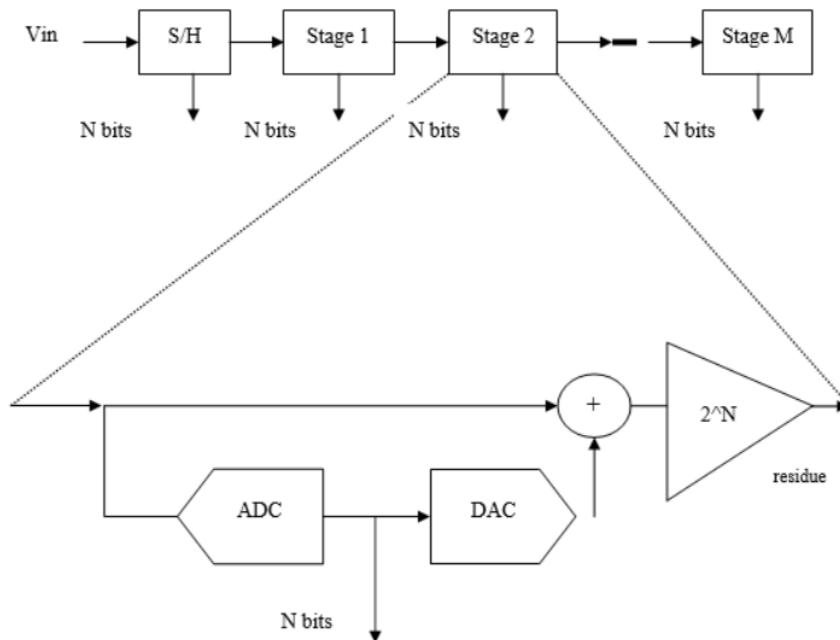


Figure 1: Schematic of N -bit per stage Pipeline ADC

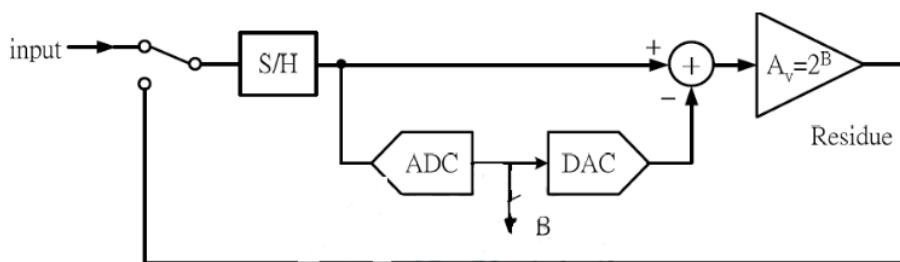


Figure 2: One Stage of Pipeline ADC

2

2.3 Operation of Pipeline Analog-to-Digital Converter

A pipeline ADC is a high-performance converter that breaks down the analog-to-digital conversion into smaller steps, like an assembly line. Each step tackles a portion of the conversion, making it faster than traditional methods.

Here's how it works:

1. **Stage by Stage:** The analog signal goes through multiple processing stations, each taking a bite out of the conversion job.
2. **Gradual Decoding:** These stations use a flash ADC (or similar) to determine a range of possibilities for the signal's value, like making a rough guess.
3. **Refining the Guess:** Each station creates a temporary copy of the signal based on its guess, then subtracts it from the original. The difference, called the residue, holds the remaining conversion details and gets amplified for the next stage.
4. **Passing the Baton:** The residue from the first guesser becomes the input for the next station, and so on. Each station adds its refined information to get the final digital answer.
5. **Double Checking (Optional):** Since errors can creep in during the process, some ADCs have a checker that examines each stage's output and adjusts the final answer for better accuracy.

This pipeline approach allows for high-speed, high-resolution conversions, making it valuable for tasks like digital communication systems and high-definition video processing. However, the design is more complex and introduces a slight delay in the output compared to simpler ADCs.

Chapter 3: Implementation and Results

3.1 Pipeline ADC Components

3.1.1 stage OP AMP

In many analog and mixed signal systems, operational amplifiers are a crucial component. In [2] Analog circuit design, such as that of operational amplifiers in CMOS technology, is becoming increasingly important as the need for mixed-mode integrated circuits grows. Operational amplifiers with two-stage architectures are often designed with modest ⁵ DC gain, high output swing, and reasonable open loop Gain Band Width product (GBW). Our goal is to build multiple fully differential CMOS Opamp topologies using a 180 nm SCL technology node in order to get high bandwidth and high gain. The goal of this effort is to create an operational amplifier capable of operating in a variety of process states, large supply voltage variations, and substantial temperature variations. Gain and bandwidth must be stable throughout several process states in order to complete this assignment. In essence, we

A differential amplifier makes up the first stage of a two-phase operational intensifier, and a ¹⁴ common source amplifier makes up the second stage. The two two-stage op-amp circuits that are being presented were created utilizing 0.18 μ m technology and designed at 1.8 V.

SCHEMATIC OF PROPOSED 2-STAGE OP-AMP:

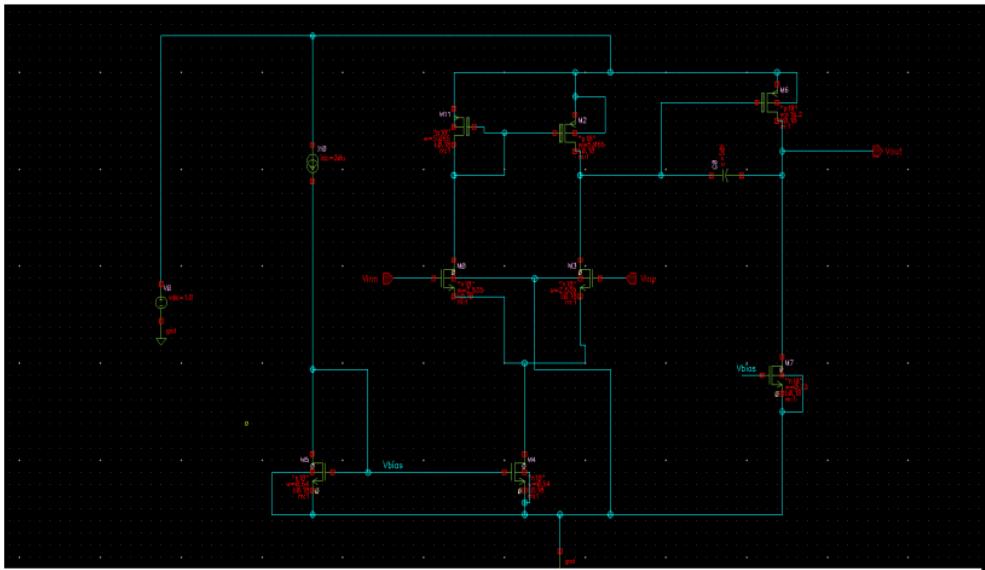


Figure 3: Two stage operational amplifier

This proposed Op Amp implements a 3-bit DAC, a voltage buffer and a subtractor in each stage of our 12-bit pipelined ADC.

SIMULATION:

AC analysis

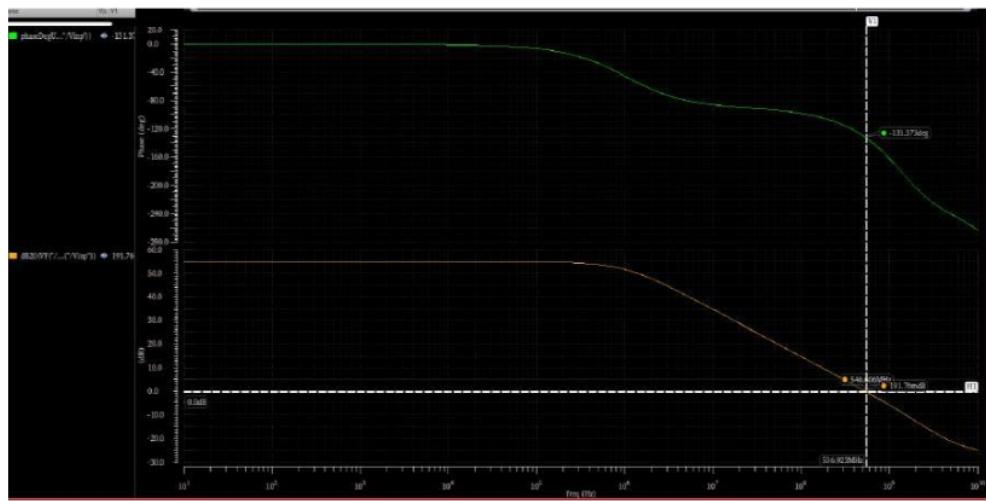


Figure 4: Gain and phase of 2 stage opamp

Here, all transistors are working in the active region, and the circuit is stable.

RESULTS:

OPEN LOOP GAIN = 54.96 dB

Phase Margin = 48.63 degree

Unity gain freq = 546.60 MHz

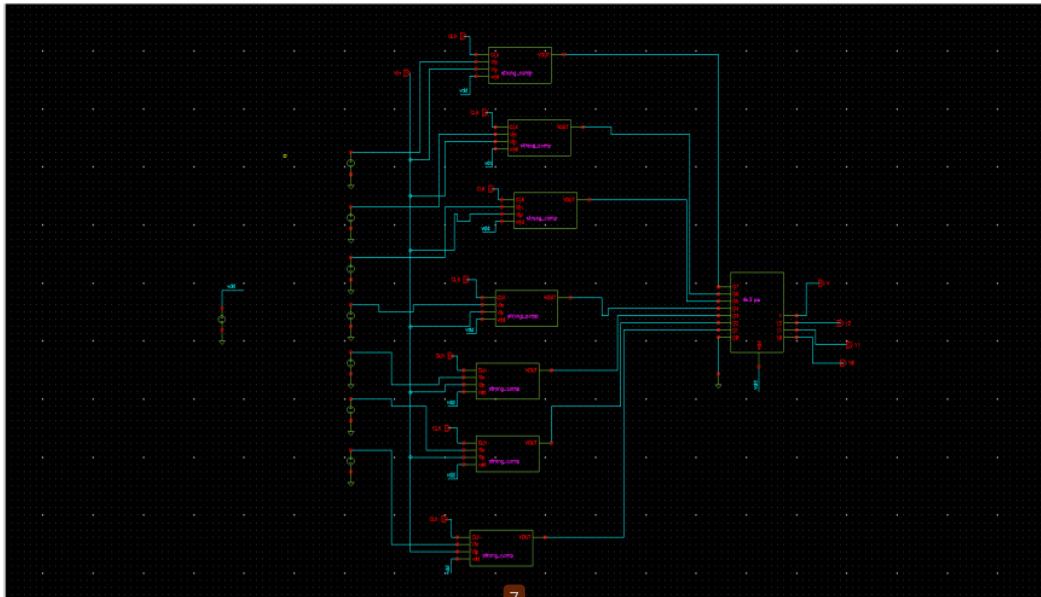
Our pipelined ADC is working with a 5MHz with a 100MHz clock frequency. This proposed Op Amp is working satisfactorily in our ADC structure.

3.2 3- Bit Flash ADC

The comparator circuit is the central component of any analog-to-digital conversion procedure. By comparing two continuum inputs coupled to an inverting and non-inverting terminal, it generates a binary output. Usually, this circuit is fed with differential input. The comparator schematic also has a common-mode input. The voltage range of this common-mode input (ICMR) is when the circuit functions normally. For this ICMR, every MOSFET in the comparator is still in the saturation range. In the current situation, good performance in terms of low power consumption, full O/P swing, high I/P impedance, and less delay can be achieved with dynamic latched comparators. By restricting it to a low power supply, a high-speed dynamic comparator confronts fierce competition as more MOSFETs are needed.

ICMR is impacted by applications such as flash ADC, which restrict it to low power supplies. In this situation, designing a comparator circuit with high performance efficiency is challenging. The Strong-ARM dynamic latch in and is among the best topologies among the several comparator designs displayed in this scenario. because of features like differential pair input-referred offset, full output swing (-VSS to VDD), high-speed comparison, and zero static power. However, because of the stacked MOSFETs' enormous power supply and limitations on energy efficiency, this arrangement cannot operate at high regeneration speeds. An N bit converter's typical flash ADC block diagram uses $2^{(N-1)}$ comparators in the circuit.[3] We therefore employ this strong-arm latch as a comparator in order to create our 3-bit Flash ADC. A 3-bit flash ADC has an 8:3 priority encoder and seven strong arm latch comparators. Because this dynamic latch has a clock, we can regulate and examine the delays and timings of each pipelined ADC stage. This 3-bit flash ADC will provide a single-stage pipelined ADC output as its output; however, after digital error correction, we will essentially extract 2 bits from the 3 bits. To decide how much residue to send to the following step, this output is likewise supplied to the DAC.

7
SCHEMATIC OF 3-BIT FLASH ADC



7
Figure 5: 3-bit flash ADC

SIMULATION RESULT:

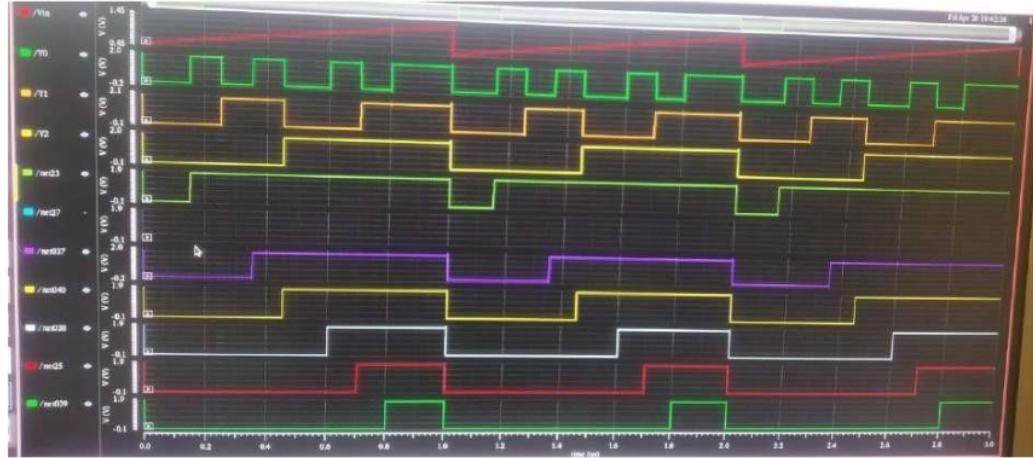


Figure 6: Output of 3-bit flash ADC

Here, you can see that we gave a ramp input, so the result Y2Y1Y0 is showing from full 000 to 111.

3.2.1 Priority Encoder For 3-bit Flash ADC

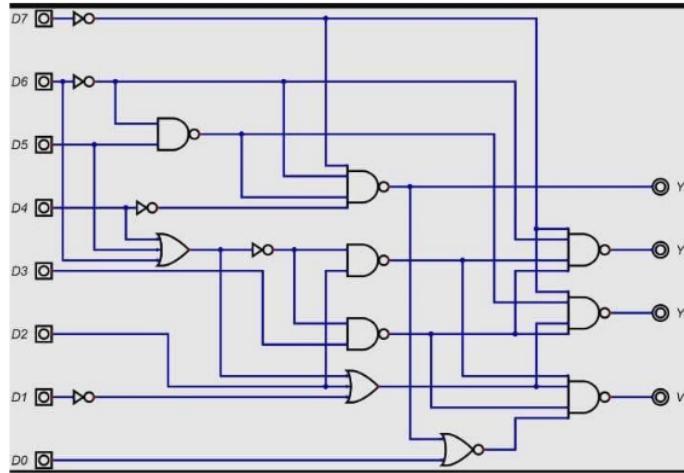


Figure 7: Priority encoder for Flash ADC

3.3 3-Bit R-2R DAC:

Each stage 3-bit digital output is again converted into analog to find the residue and this residue analog input is fed to next stage of pipeline ADC. Here, we implemented an R-2R resistive ladder as non-inverting input to an Op Amp. The above-mentioned Op Amp is used in this DAC. A switch resistor ladder is implemented.

SCHEMATIC OF DAC

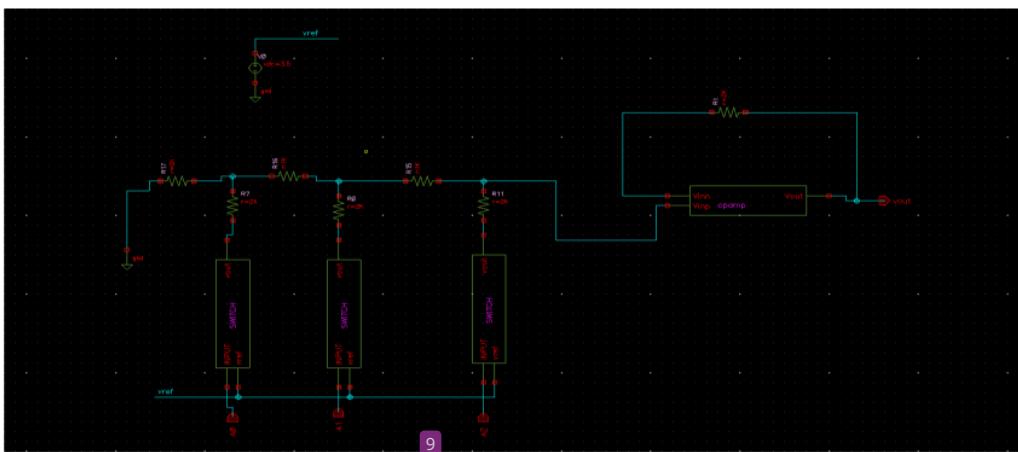


Figure 8: R-2R digital to analog converter

SIMULATION RESULT

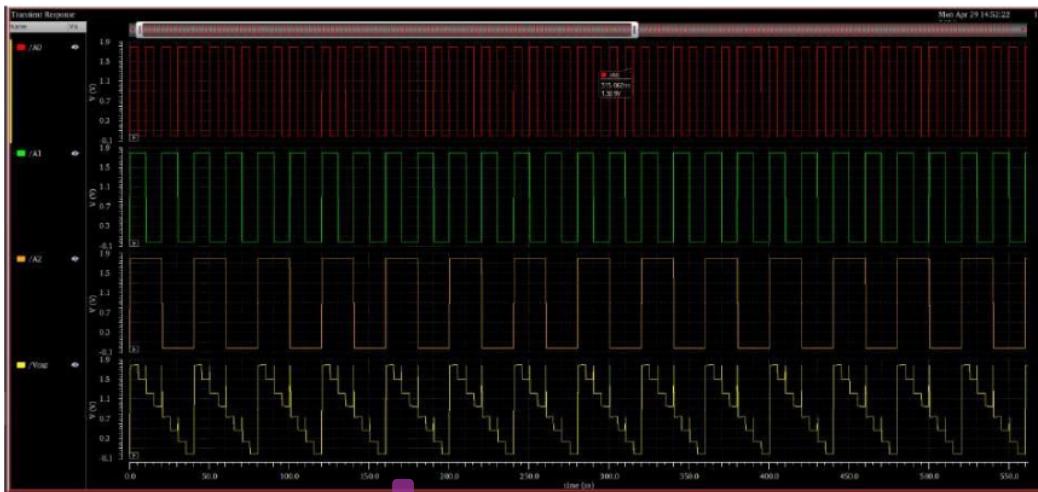


Figure 9: R-2R digital to analog converter output

Here, it is shown that the input is A2A1A0 with A2 as the MSB, and the red signal is output. Here we can see the 8 stages of voltage that a 3-bit digital input makes when it is fed to

¹¹ **3.4 Sample And Hold Circuit:**

A sample and hold circuit is an electronic circuit used to capture and store the voltage of an input signal at a particular instant and hold that voltage constant for a certain period. It consists of two main components: a sample circuit and a hold circuit.

1. **Sample Circuit:** This part of the circuit samples the input signal at regular intervals or when triggered. It captures the instantaneous voltage level of the input signal and holds it momentarily.
2. **Hold Circuit:** Once the sample is taken, the hold circuit maintains the sampled voltage level constant for a certain period, allowing it to be accurately measured or processed by other circuitry.

The main applications of sample and hold circuits include analog-to-digital conversion (ADC), signal reconstruction, and data acquisition systems. They are particularly useful when the input signal needs to be digitized or processed at discrete intervals while preserving its original characteristics.

Sample and hold circuits are often used with analog-to-digital converters in systems where a continuous analog signal needs to be converted into a series of digital values. By holding the sampled voltage level constant until the ADC completes its conversion, the circuit ensures accurate digitization of the analog signal.

There are different implementations of sample and hold circuits, ranging from simple to more complex designs depending on the application's specific requirements. These circuits can be built using operational amplifiers (op-amps), switches, capacitors, and other passive components. The components and circuit topology choice depends on speed, accuracy, and power consumption requirements.

²² **SCHEMATIC OF SAMPLE AND HOLD CIRCUIT**



Figure 10: Track and hold Schematic

SIMULATION RESULT

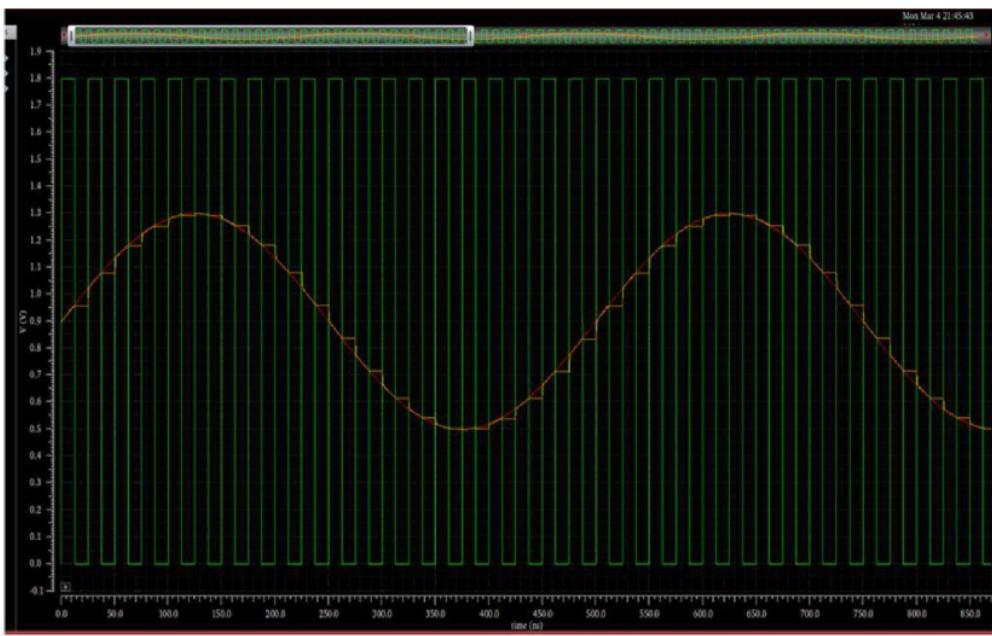


Figure 11: Track and Hold output for sine wave

3.5 Full Adder Circuit:

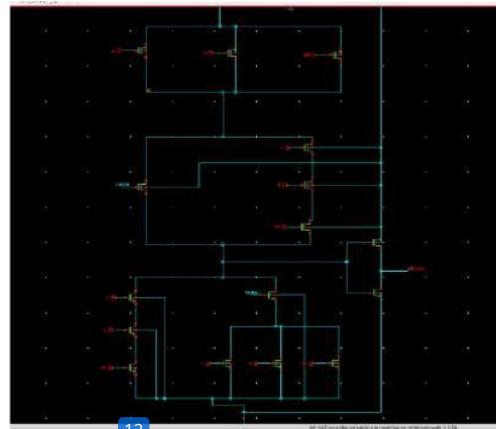


Figure 12:Sum circuit of Full adder

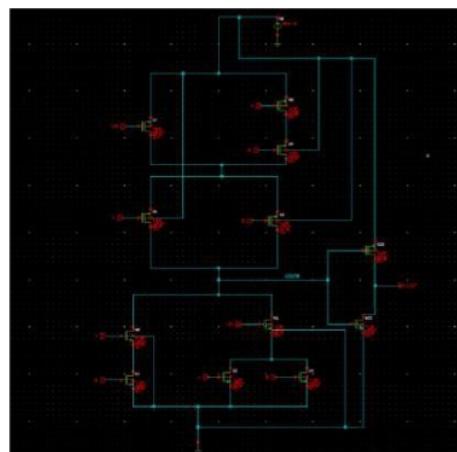


Figure 13:Carry circuit for full adder

3.6 Subtractor:

An operational amplifier (op-amp) subtractor is a circuit configuration that performs the subtraction of two input voltages. It typically consists of an op-amp with multiple.

Input terminals. The basic idea is to subtract the voltages into different input terminals and use feedback to achieve the desired subtraction.

The configuration usually involves an inverting amplifier setup, where one input voltage is connected to the inverting input terminal (-) and the other input voltage is connected through a resistor network to the non-inverting input terminal (+). The output voltage is proportional to the difference between the two input voltages.

The subtractor configuration is commonly used in various electronic circuits, such as instrumentation amplifiers, signal processing circuits, and audio applications, where the need to compute the difference between two signals arises frequently.

SCHEMATIC OF SUBTRACTOR

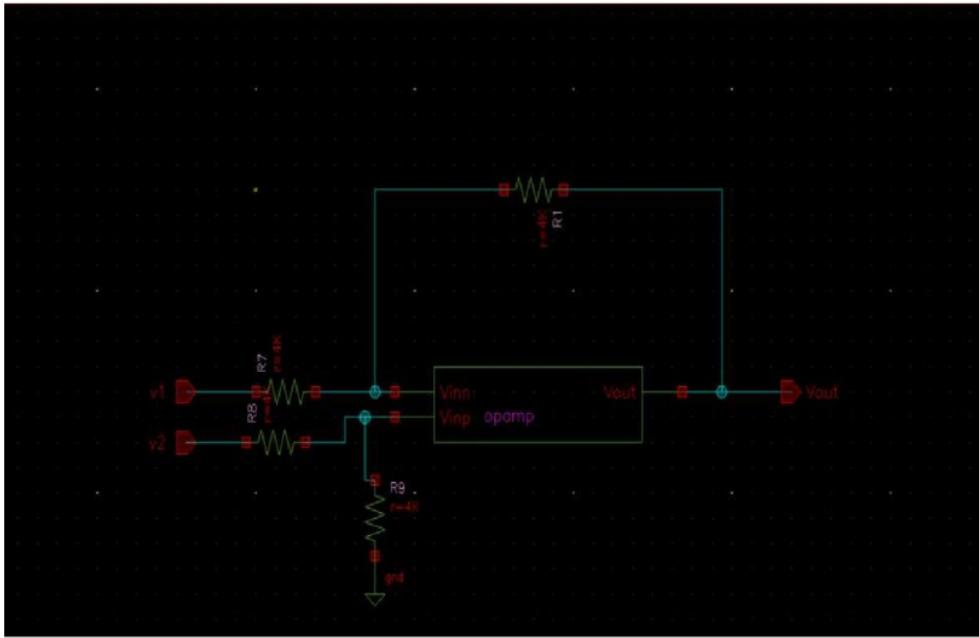


Figure 14: Analog signal subtractor using opamp

SIMULATION

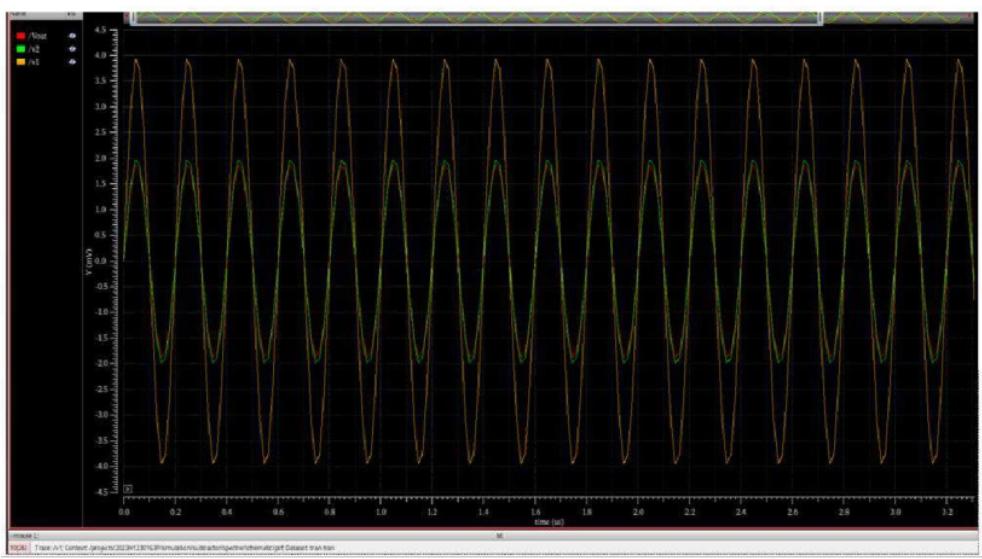


Figure 15: Subtracting 2 analog signals of different amplitude

3.7 D-Flip Flop:

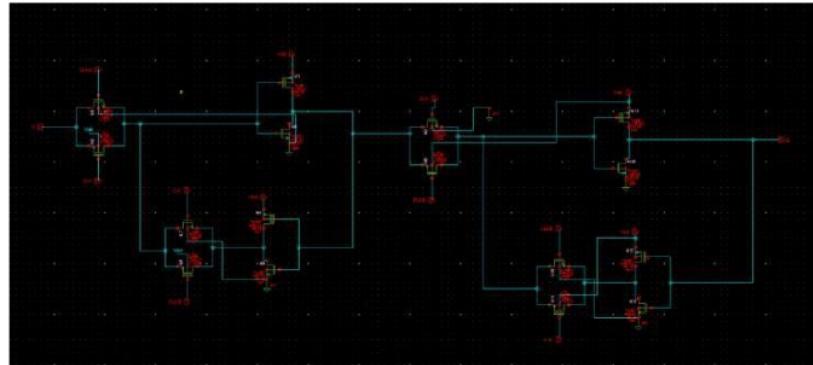


Figure 16: D-flip flop using transmission gates

3.8 Buffer Circuit

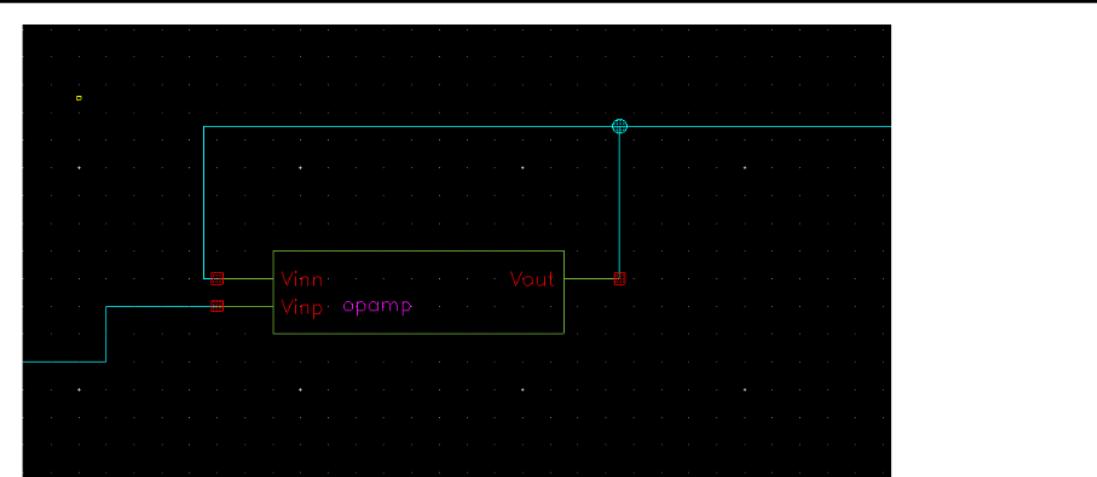


Figure 17: Buffer circuit using negative feedback Opamp

3.9 Amplifier of Gain 2



Figure 18: Non inverting amplifier of Gain "2" using Opamp

3.10 Comparator:

Depending on the differences in their input, metastability analysis can be used to examine the speed of the suggested comparator. When a comparator detects a small difference, it takes some time to produce a valid output. If this procedure is not completed within half the clock pulse, metastability happens. Thus, this type of issue arises at high comparison speeds greater than 1 GHz. In less than a nanosecond, switches are dragged from the source voltage to the drain terminal [4].



Figure 19:Schematic of Comparator 1

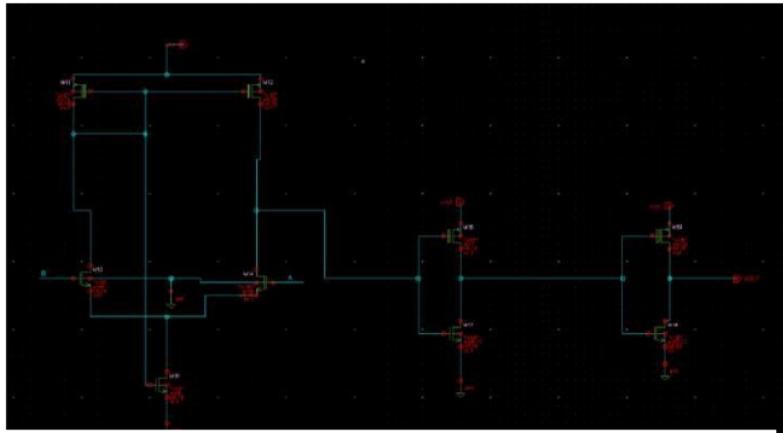


Figure 20: Schematic of Comparator 2

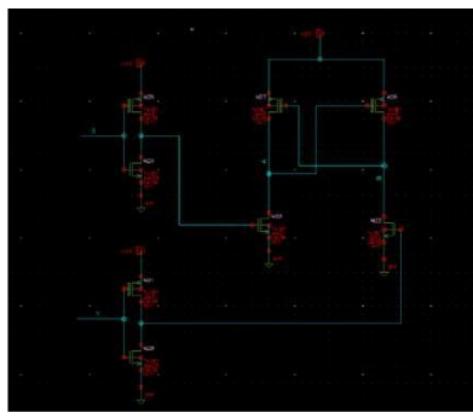


Figure 21:Schematic of Comparator 3

3.11 First Stage Design Of Pipeline ADC.

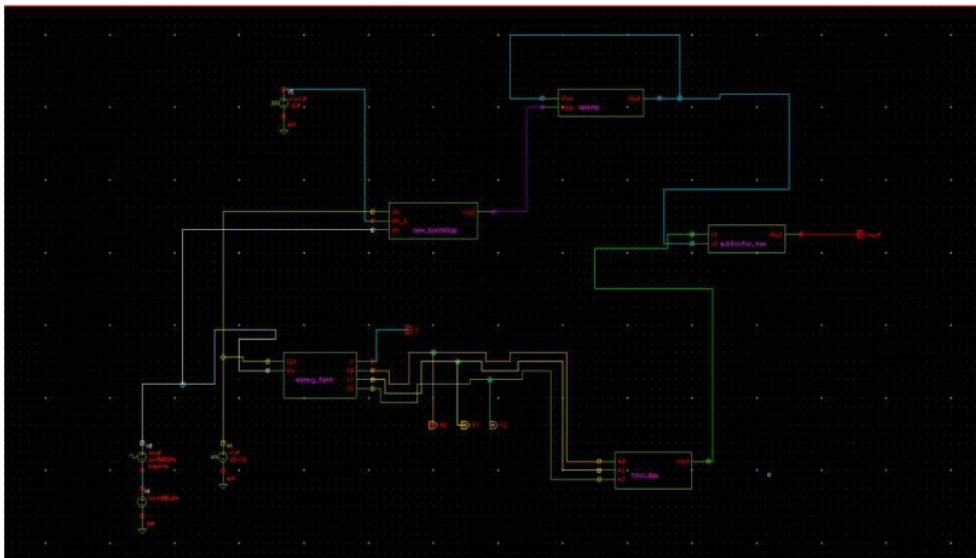
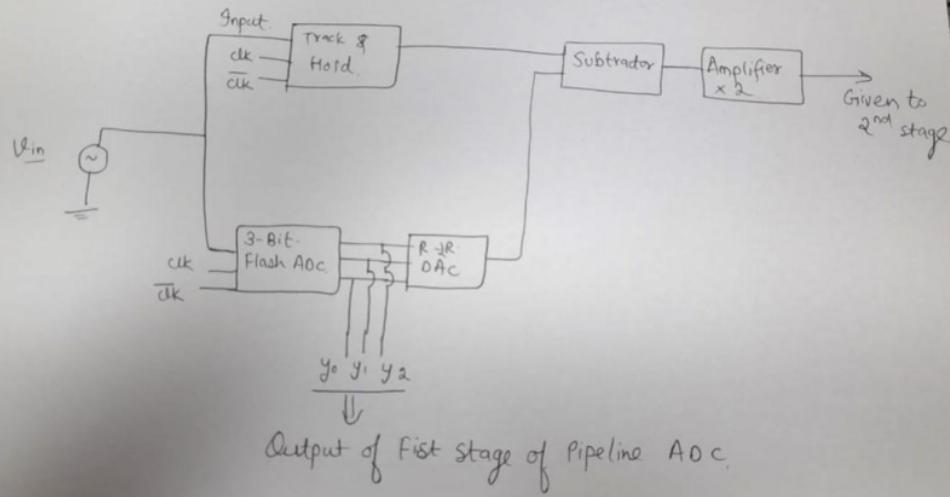


Figure22: First stage of pipeline Analog to digital converter

3.11.1 Hand Drawn Schematic of First stage of pipeline ADC

Buffer will be used if there is an loading effect.



SIMULATION RESULT OF THE FIRST STAGE

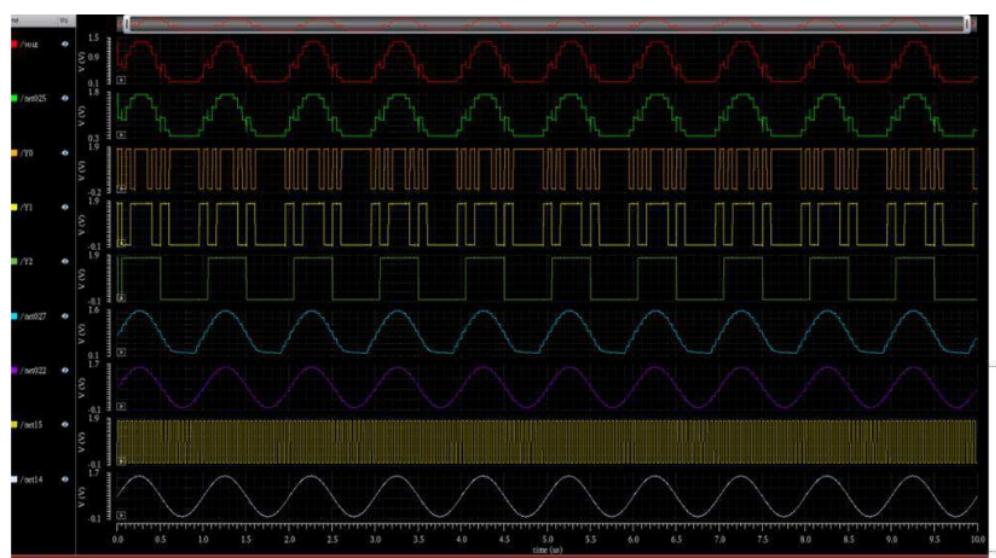


Figure 23:Output of first Stage of pipeline ADC

3.12 Digital Error Correction:

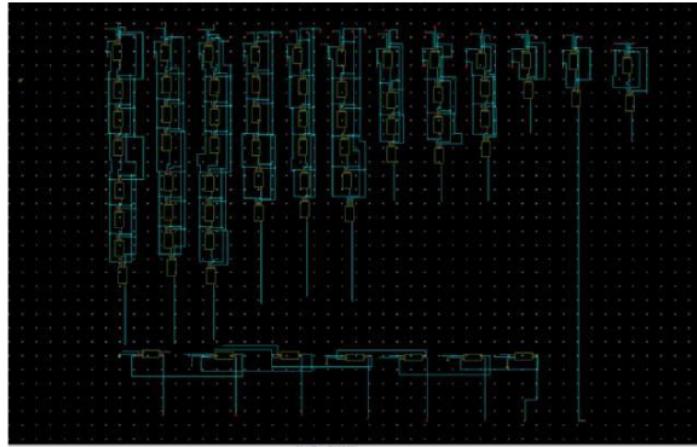
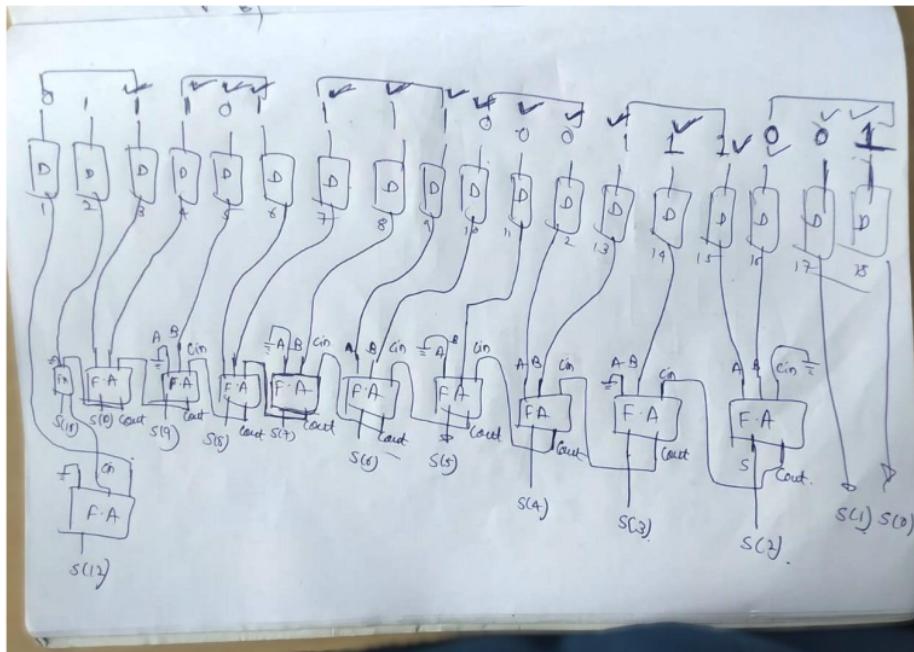


Figure24: Digital error Correction using D flip flop ladder

3.12.1 Hand Drawn Schematic of Digital error Correction Circuit with 1 D-flip flop

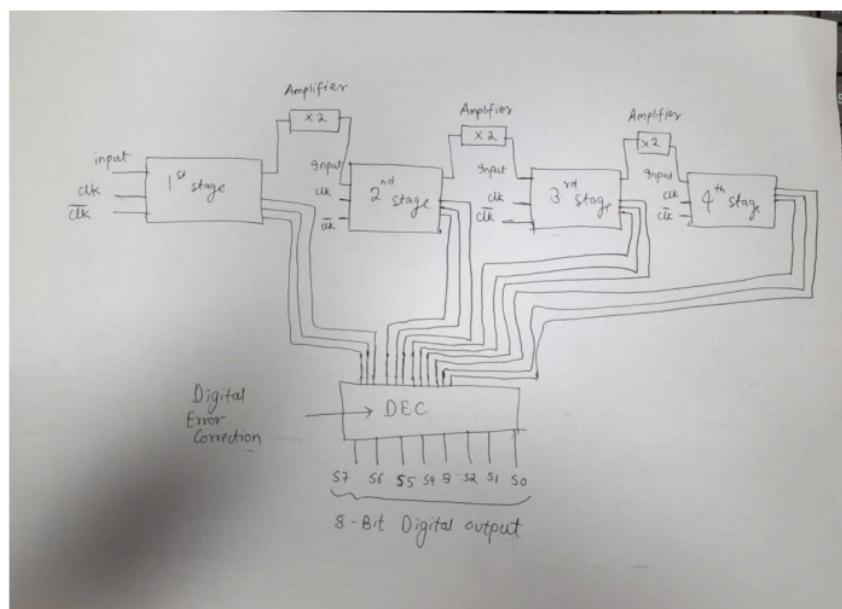


3.13 Final Schematic of 8-Bit Pipeline ADC:⁸



Figure 25.4 stages of 8-bit pipeline ADC using digital error correction

3.13.1 Hand Drawn Schematic of 4 stages of 8-bit Pipeline ADC:



3.13.2 Ramp input to 8-Bit Pipeline ADC:

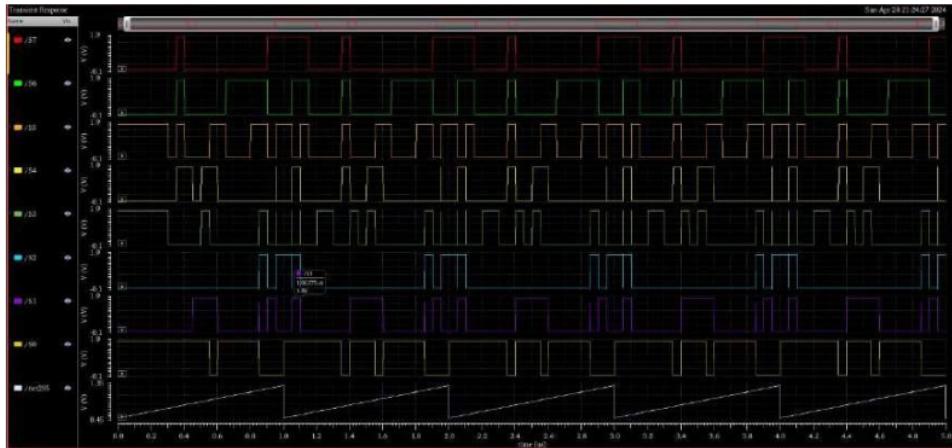


Figure 26: Output of 8-bit pipeline ADC using Ramp input

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3.13.3 Sin Input to 8-Bit pipeline ADC:

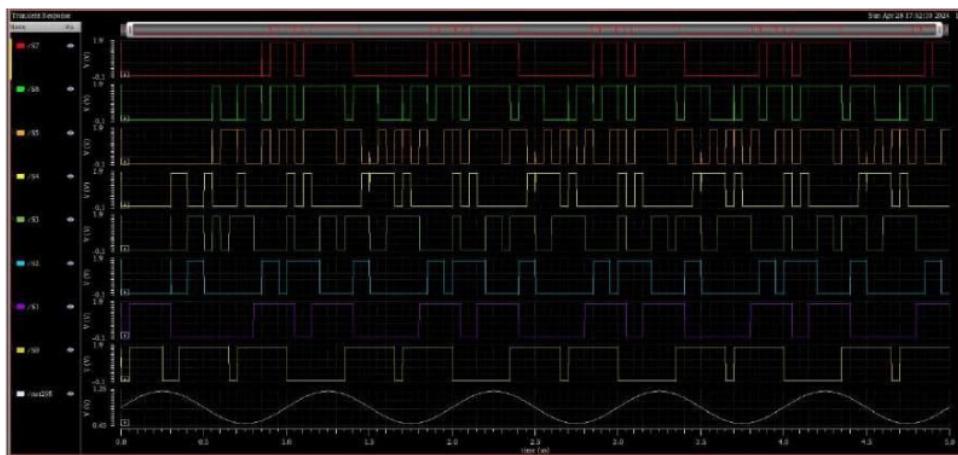


Figure 27: Output of 8-bit pipeline ADC using Sine input

Chapter 4: Conclusion

We have used several components to build stages of 8-Bit pipeline analog to digital converter such as 3-Bit flash ADC, R-2R DAC, Track and Hold circuit using Bootstrap Biasing ,

Strong Arm Latch comparator, Subtractor, amplifier of Gain 2, Digital error correction circuit using D-flip Flop and Full adder

Using all the above components we have put together the 8-bit pipeline ADC and we have checked the output for the sine wave and ramp input.

References

- [1] ³ D. Meganathan, A. Sukumaran, M. M. Dinesh Babu, S. Moorthi, and R. Deepalakshmi, “A systematic design approach for low-power 10-bit 100 MS/s pipelined ADC,” *Microelectronics J*, vol. 40, no. 10, pp. 1417–1435, Oct. 2009, doi: 10.1016/J.MEJO.2009.06.004.
- [2] ⁴ “Design & Implementation of Low Power 3-bit Flash ADC in 0.18 μ m CMOS.” Accessed: May 05, 2024. [Online]. Available: ¹⁶ https://www.researchgate.net/publication/348188967_Design_Implementation_of_Low_Power_3-bit_Flash_ADC_in_018mm_CMOS
- [3] ¹ B. P. Sharma, A. Gupta, and C. Shekhar, “Design & Analysis of Performance-efficient Comparator for IoT Application,” *9th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering, UPCON* 2022, 2022, doi: 10.1109/UPCON56432.2022.9986363.

PRIMARY SOURCES

- | | | |
|---|--|------|
| 1 | Buddhi Prakash Sharma, Anu Gupta, Chandra Shekhar. "Design & Analysis of Performance-efficient Comparator for IoT Application", 2022 IEEE 9th Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), 2022 | 3% |
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