Area, Power and Performance Analysis of High Speed Sample and Hold Circuit

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***Abstract*—An analysis of high speed sample and hold circuit in different structure is presented. Performance and area comparison between two type of sample and hold circuit in low voltage is done. These different type of circuits are simulated and layout designed in 55nm CMOS technology. Both the structures based on a bootstrap switch that can acquire analog wave forms at sampling rate of 100MHz with 10 bit linearity at 1.8V of supply voltage.**

***Keywords*—Bootstrap switch, Non-overlapping clock, sampling switch, Clock feed through, Charge injection**

I. Introduction

The multimedia industry is relay more on the digital signal processing nowadays, Which increases the demand for a high speed analog to digital converters[1][2].Sample and hold circuit is fundamental block of ADC circuit[3][4]. It takes the input samples and hold it for a time period. Basically a sample and hold circuit consist of a sampling switch and a holding capacitor.

Linearity and speed of the sample and hold circuit depends on the ON resistance and capacitance. If an Nmos switch is using as a sampling switch the R_{on} will be given in equation 1.

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}V_{GS} - V_{TH}} \tag{1}$$

$$V_{GS} = V_{DD} - V_{IN} \tag{2}$$

Here the R_{on} depends on the V_{in} voltage. And Changes in Vin reflects in the Ron resistance and which will make the sample and hold circuit nonlinear. The non-linearity can be avoided by making the Ron independent of V_{in} .So the bootstrap switch concept is used in the sample and hold circuit, Shown in Fig 3.

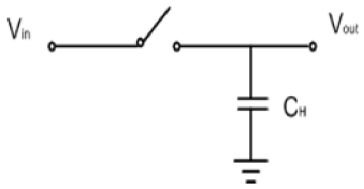

Fig. 1. Simple Sample and Hold Circuit

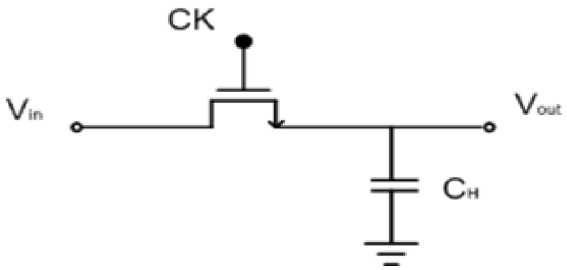

Fig. 2. Sample and Hold Circuit in Transistor level

In the bootstrap switch circuit the capacitor acts as a floating battery. There are two clock signals Phi1 and Phi2 which are non-overlapping. In Phi2 phase Sw3, Sw4 and Sw5 closes remaining opens. Thus the capacitor charges to VDD. In Phi1 phase Sw1 and Sw2 closes and remaining three opens. So at the gate terminal of sampling switch gets V_{DD}+V_{in} voltage. V_{gs} of sampling switch becomes V_{DD}.So Ron becomes independent of V_{in} voltage and the circuits linearity is improved.

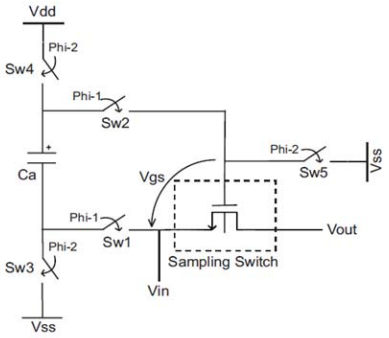

Fig. 3. Simple Bootstrap Switch Concept

Speed of the circuit depends on the ON resistance and capacitance. Parasitic capacitance changes the boosted clock signal voltage level is given in equation 3.

$$V_g = V_{in} + \frac{C_3}{C_3 + C_p}V_{dd} \tag{3}$$

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So the parasitic capacitance should be minimum for the circuit to get a high performance[5].Clock feed through and Charge injectio are the two main non-idealities present in switch capacitor circuit[6].Which degrades the performance of the circuit up to a great extend.

II. Bootstrap switch with boosted clock

Sample and hold circuit containing a bootstrap switch works with a non-overlapping boosted clock signal mainly having three parts. A non-overlapping clock generator, clock boost circuit and a bootstrap switch[7][8]. It is a conventional sample and hold circuit. Fig 4 shows the bootstrap switch used in the circuit. Phi1 and Phi2 are two non-overlapping clock signals which is generated from the clock generator.

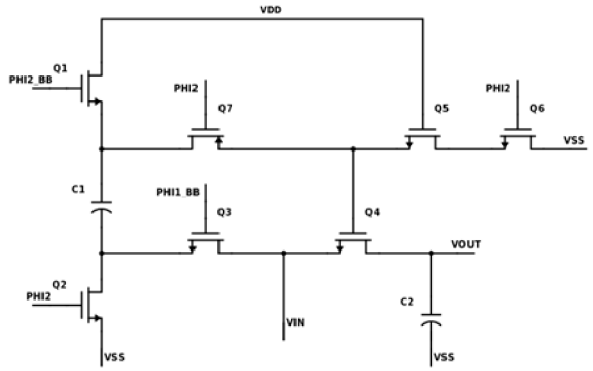

Fig. 4. Bootstrap Switch

$Phi1_{bb}$ and $Phi2_{bb}$ represents the boosted clocks.Q4 is the sampling switch. In the Phi2 phase Q1,Q2,Q5,Q6 turns ON. When Q1 and Q2 turned ON the capacitors top plate connected to VDD and bottom plate is connected to V_{SS}(ground).So capacitor charges to V_{DD} in the Phi2 phase. At the same time Q5 and Q6 are ON so the gate of sampling switch gets a low voltage which turns OFF the sampling switch. It is the Hold mod of sample and hold circuit. At this mode whatever voltage stored in the Output capacitor C2 will be obtained at the Output terminal. In Phi1 phase Q1,Q2 and Q6 are in OFF state. But Q3 and Q7 are in the ON state. So at the gate of sampling switch Q4 gets a voltage V_{DD}+ V_{in} and the source terminal of the sampling switch having Vin voltage .Thus the Q4 will be in ON state and V_{gs} will be V_{DD} .So Ron is independent of V_{in}. And in this mode the output follows the input voltage.

Here non-overlapping clock is used for the complete charging of capacitor C1.Otherwise the capacitor cannot charge up to V_{DD} ,which will leads to variations at the V_{gs} voltage of sampling switch. Non-Overlapping clocks are generated from the circuit shown in the Fig 5.

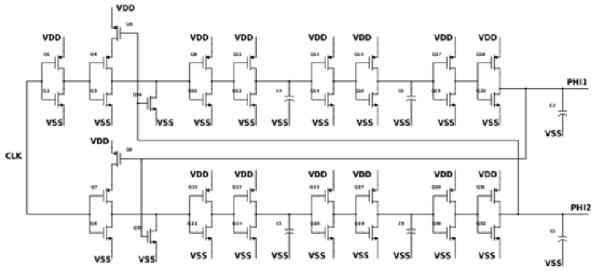

Fig. 5. Non-overlapping Clock Generator Circuit

Inverter, NOR gate and buffers are used in the circuit. Here CLK signal is given to one NOR gate and inverted CLK signal is given to second NOR gate with a delay .And the buffers are used to strengthen the signals. The obtained Phi1 and Phi2 are the non-overlapping clock signals.

In the bootstrap switch circuit we are using nmos Q1 to charge the capacitor. Since nmos is a week One loading device it cannot charge up to V_{DD}. In order to get a complete conduction boosted clocks are applied to the gates of Q1. Fig 6 shows the clock boost circuit.

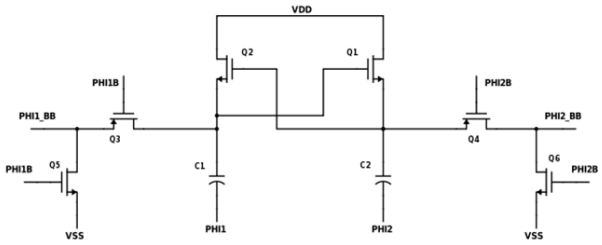

Fig. 6. Clock Boost Circuit

In clock boost circuit two back to back connected nmoses boosts the charge stored in the capacitors. The capacitors are initially charged to V_{DD} and in each clock the back to back connected nmoses boosts it in to $2V_{DD}$. Q3,Q5 and Q4,Q6 are symmetric.Phi1b and Phi2b are the inverted signals of Phi1 and Phi2 respectively.$Phi1_{bb}$ and $Phi2_{bb}$ are the two non-overlapping boosted clocks.In Phi1 phase $Phi1_{bb}$ becomes $2V_{DD}$ and $Phi2_{bb}$ becomes zero and in Phi2 phase $Phi2_{bb}$ becomes $2V_{DD}$ and $Phi1_{bb}$ becomes zero.Thus the clock boost circuit gives 0-$2V_{DD}$ non-overlapping clock signals.

III. Bootstrap switch without boosted clock

A sample and hold circuit without boosted clock[9] is shown in Fig 7. In the circuit Q12 is the sampling switch. When the CLK is low CLKB becomes high and which turns ON Q6,Q15, Q9 and Q14, thus the node n2 gets ground voltage so Q5 turns ON.So the capacitors top plate connects to V_{DD} and bottom plate connects to ground .Capacitor C1 charges to V_{DD}. Since Q3 is in On state the node n1 will be V_{DD}, so Q7 will be in OFF condition.Q10 and sampling switch will be in OFF condition since the nod n2 voltage is ground voltage. Q7 and Q10 will isolate the sampling switch from the capacitor

C1 in the charging phase. In this state the sampling switch is in OFF condition and the voltage in the output capacitor will be obtain at the output.

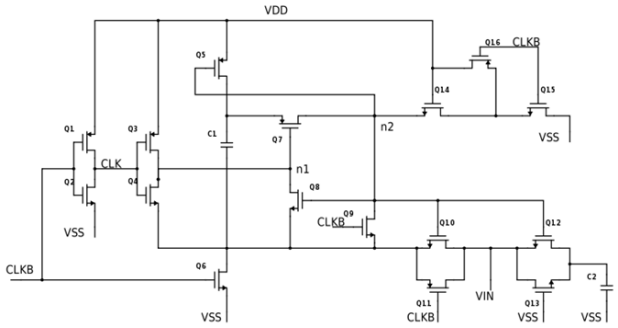

Fig. 7. Bootstrap Switch Circuit without Boosted Clock Signal

When the CLK is high and CLKB becomes low the node n1 will be connected to the bottom plate of Capacitor C1 and it will be in low voltage which Turns ON the Q7 ,and Q6 will be in OFF state. Thus the node n2 connected to top plate of Capacitor C1 .It turns ON the Q10 and the Sampling switch .At the gate terminal of the sampling switch will obtain a voltage V_{DD}+V_{in} and at the source it is V_{in}. Thus Vgs of the sampling switch will be V_{DD}. Pmos Q16 is added to the circuit to reduce the parasitic capacitance. It can increase the linearity of the circuit. Transistors Q9 and Q11 are used for the Fast turn on and turn off which increase the speed of the sampling switch. The dummy switch Q13 will reduce the switching non linearities by introducing a clock feed through error with same amplitude and opposite phase of the sampling switch.

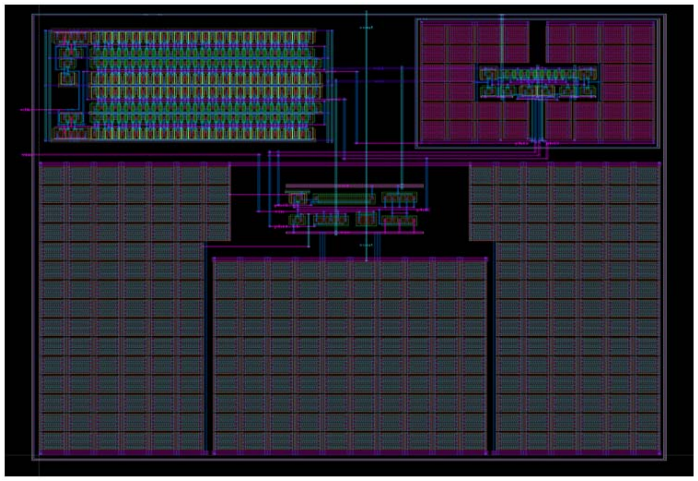

Fig. 8. Layout of Bootstrap switch with Boosted Clock Circuit

IV. Comparison

In bootstrap switch with boosted clock signal circuit requires two extra circuits compared to the bootstrap switch without boosted clock signal circuit, Non-overlapping clock generator and clock boost circuit. When nmos Q1 in Fig 4 changed to pmos the boosted clock can be avoided. In the second circuit clock boost is not there so two capacitance can be avoided which will reduce the area and cost of the IC. Fig 8 and Fig 9 shows the layouts of bootstrap switch with clock boost and without clock boost circuits. For the bootstrap switch with boosted clock signal circuit requires 50u x 50u area but in the case of bootstrap switch without boosted clock signal circuit requires only 40u x 30u area. Area is around 50% less in the sample and hold circuit in which clock boost circuit is not there.

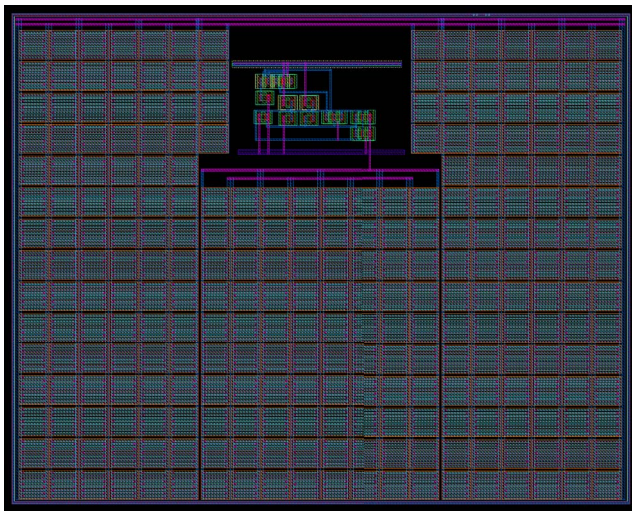

Fig. 9. Layout of Bootstrap switch without Boosted Clock Circuit

To improve the linearity of the circuit one transistor Q15 is added in the circuit Fig 7. Which will helps to reduce the parasitic capacitance effect of the sampling switch. When the CLKB is low the transistor Q15 turns on and the transistor Q14 becomes off thus the leakage through Q14 can be reduced. And by introducing a dummy switch the switching non linearities can also be reduced. For speed improvement two transistors Q9 and Q11 are introduced which will helps for fast turn on and turn off of the sampling switch.

V. Simulation Results

Both the sample and hold circuits are simulated and layout design done in 55nm cmos technology. The circuits are designed for a sampling rate of 100MHz and 10 bit linearity at 1.8 supply voltage. Bootstrap switch with boosted clock circuit is having SFDR 66.86dB and an ENOB of 10.81 bits. But it is not satisfying all corners. Corner simulations are done across process, supply voltage and temperature. Supply voltage from 1.62 V to 1.98 V and Temperature from -50 to 150 Degree Celsius. Fig 10 shows the SFDR[10] plot for bootstrap switch with boosted clock circuit and Table 1 shows the corner simulation results of bootstrap switch with boosted clock circuit. But in the case of bootstrap switch without boosted clock is having an SFDR 73.48dB and an ENOB 11.78 bits. And in the corner simulation it is satisfying in all corners. Both the circuits are designed for a 400 fF output capacitance as per the specifications. Power consumption of the first circuit is 1.134 mW and the second circuit is around 0.986mW. Fig 11 shows the SFDR plot for bootstrap switch without boosted clock and Table 2 shows the corner simulation results of bootstrap switch without boosted clock circuit.

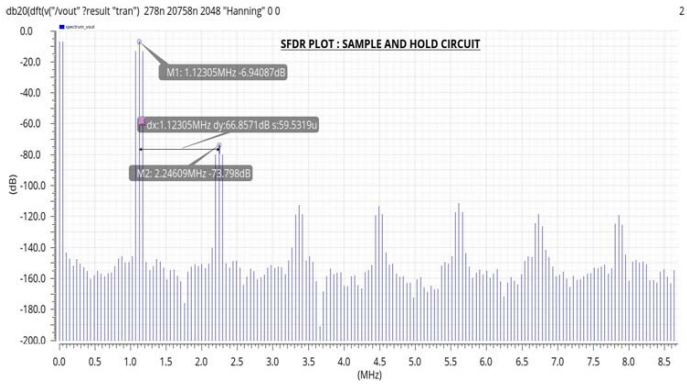

Fig. 10. SFDR plot of Bootstrap Switch with Boosted Clock Circuit

Table I. shows the corner simulation values for Bootstrap switch with boosted clock signal circuit.

TABLE I.
CORNER SIMULATION RESULT

Corner	Process	Temparature	V_{DD}	SFDR	ENOB
Nom	FET-tt-pre	30	1.8	66.86	10.81
$C1_0$	FET-ffp-pre	-50	1.62	71.28	11.54
$C1_1$	FET-ffp-pre	150	1.62	55.17	8.868
$C1_2$	FET-ffp-pre	-50	1.98	78.7	12.78
$C1_3$	FET-ffp-pre	150	1.98	64.75	10.46
$C1_4$	FET-ssp-pre	-50	1.62	54.43	8.738
$C1_5$	FET-ssp-pre	150	1.62	44.98	7.154
$C1_6$	FET-ssp-pre	-50	1.98	66.74	10.79
$C1_7$	FET-ssp-pre	150	1.98	51.8	8.27

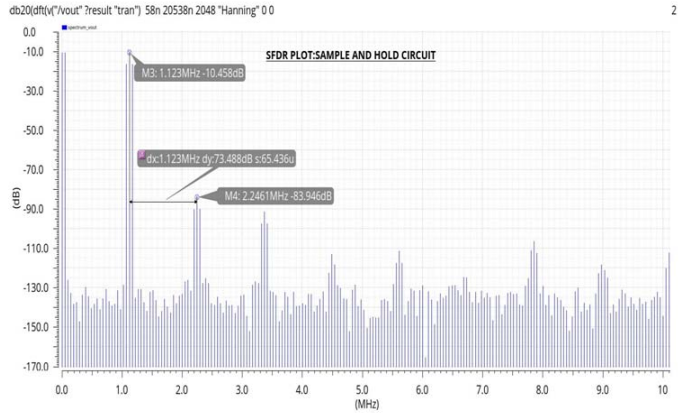

Fig. 11. SFDR plot of Bootstrap Switch without Boosted Clock Circuit

Table II. shows the corner simulation values for Bootstrap switch without boosted clock signal circuit.

TABLE II.
CORNER SIMULATION RESULT

Corner	Process	Temparature	V_{DD}	SFDR	ENOB
Nom	FET-tt-pre	30	1.8	73.49	11.78
$C0_0$	FET-ssp-pre	-50	1.98	78.64	12.53
$C0_1$	FET-ssp-pre	150	1.98	68.53	10.98
$C0_2$	FET-ssp-pre	-50	1.62	70.99	11.33
$C0_3$	FET-ssp-pre	150	1.62	59.05	9.492
$C0_4$	FET-ffp-pre	-50	1.98	80.17	12.93
$C0_5$	FET-ffp-pre	150	1.98	74.73	11.92
$C0_6$	FET-ffp-pre	-50	1.62	76.1	12.23
$C0_7$	FET-ffp-pre	150	1.62	67.51	10.86

VI. CONCLUSION

High speed sample and hold circuit analysis done in two structures, one is bootstrap switch with boosted clock and second one is bootstrap switch without boosted clock. The comparison of these two circuits includes area analysis ,linearity analysis, speed analysis and performance analysis. In all cases the bootstrap switch without boosted clock sample and hold circuit giving the better results. It can be used for the high speed applications of sample and hold circuit.

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