3.6 DIGITAL ELECTRONICS

L T P

4 - 4

RATIONALE

This course has been designed to make the students know about the fundamental principles of digital electronics and gain familiarity with the available IC chips. This subject aims to give a background in the broad field of digital systems design and microprocessors.

LEARNING OUTCOMES

After undergoing the subject, student will be able to:

- explain the importance of digitization.
- verify and interpret truth tables for all logic gates.
- realize all logic functions with NAND and NOR gates
- design and demonstrate adder and subtractor circuits
- verify and interpret truth tables of multiplexer, demultiplexer, encoder and decoder ICs
- design and realize different sequential circuit(Flip flops, counters and shift registers)
- verify performance of different A/D and D/A converters.
- explain the features and applications of different memories

DETAILED CONTENTS

1. Introduction (03 Periods)

    1.1 Distinction between analog and digital signal.
    1.2 Applications and advantages of digital signals.

2. Number System (03 Periods)

    2.1 Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa.
    2.2 Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction.

3. Codes and Parity (04 Periods)

3.1 Concept of code, weighted and non-weighted codes, examples of 8421, BCD, excess-3 and Gray code.
3.2 Concept of parity, single and double parity and error detection

4. Logic Gates and Families (06 Periods)

4.1 Concept of negative and positive logic
4.2 Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates, NAND and NOR as universal gates.
4.3 SSI, MSI, LSI, VLSI (Definition)
4.4 Propagation delay, Noise Margin, Fan in, Fan out, Power dissipation.
4.5 Comparison between TTL, CMOS, ECL, MOS on basis of diff parameter.
4.6 Introduction to Bipolar logic, MOS, ECL, TTL and CMOS logic families
4.7 Basic logic gate using NMOS, PMOS, CMOS

5. Logic Simplification (06 Periods)

5.1 Postulates of Boolean algebra, De Morgan's Theorems. Implementation of Boolean (logic) equation with gates
5.2 Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits

6. Arithmetic circuits (03 Periods)

6.1 Half adder and Full adder circuit, design and implementation.
6.2 Half subtractor and Full subtractor or Circuit, design and implementation.

7. Combinational Circuit (06 Periods)

7.1 Introduction to combinational circuit
7.2 Multiplexer, De-multiplexer, Encoder, Decoder block diagram and Circuit.
7.3 7 segment decoder
7.4 BCD Encoder Circuit

8. Introduction to Sequential circuit (06 Periods)

8.1 Introduction to Sequential
8.2 Copmparison between combinational and sequential circuit

8.3 Concept and types of latch with their working and applications
8.4 Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops.
8.5 Difference between a latch and a flip flop

9. Counters (06 Periods)

9.1 Introduction to Asynchronous and Synchronous counters
9.2 Binary counters
9.3 Divide by N ripple counters, Decade counter, Ring counter and twisted Ring counter.

10. Shift Register (05 Periods)

10.1 Introduction and basic concepts including shift left and shift right.
a) Serial in parallel out, serial in serial out, parallel in serial out, parallel in parallel out.
b) Universal shift register

11. A/D and D/A Converters (04 Periods)

11.1 Working principle of A/D and D/A converters
11.2 Brief idea about different techniques of A/D conversion and study of :
- Stair step Ramp A/D converter
- Dual Slope A/D converter
- Successive Approximation A/D Converter

11.3 Brief idea of :
- Binary Weighted D/A converter
- R/2R ladder D/A converter

11.4 Applications of A/D and D/A converter.

12. Semiconductor Memories (04 periods)

Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM), static and dynamic RAM.

LIST OF PRACTICALS

1. Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates

2. Realisation of logic functions with the help of NAND or NOR gates

3. - Design of a half adder using XOR and NAND gates and verification of its operation

   - Construction of a full adder circuit using XOR and NAND gates and verify its operation

4. Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops).

5 Verification of truth table for encoder and decoder ICs, Mux and DeMux

6. To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.

7. To design a 4 bit ring counter and verify its operation.
8. Use of Asynchronous Counter ICs (7490 or 7493)

Note: Above experiments may preferably be done on Bread Boards.

INSTRUCTIONAL STRATEGY

The digital systems in microprocessors have significant importance in the area of electronics. Adequate competency needs to be developed by giving sufficient practical knowledge in microprocessors (programming as well as interfacing), A/D, D/A Converters and other topics. Help may be taken in the form of charts, simulation packages to develop clear concepts of the subject. Programming exercises other than the tested in circulation may be given to the students.

MEANS OF ASSESSMENT

- Class test/quizzes
- Home assignments
- Attendance
- Sessional Test
- Practical Tasks

RECOMMENDED BOOKS

1. Digital Logic Designs by Morris Mano, Prentice Hall of India, New Delhi
2. Digital Electronics by RP Jain, Tata McGraw Hill Education Pvt Ltd, New Delhi
3. Digital Electronics by BR Gupta, Dhanpat Rai & Co., New Delhi

4. Digital Systems: Principles and Applications by RJ Tocci, Prentice Hall of India, New Delhi

5. E-books/e-tools/relevant software to be used as recommended by AICTE/NITTTR, Chandigarh.

Websites for Reference:

http://swayam.gov.in

SUGGESTED DISTRIBUTION OF MARKS

Topic No.	Time Allotted (Periods)	Marks Allocation (%)
1.	03	07
2.	03	07
3.	04	07
4.	06	09
5.	06	11
6.	03	11
7.	06	11
8.	06	05
9	06	11
10.	05	11
11.	04	07
12	04	07
Total	**56**	**100**