Abhinav Gummadi

972-854-1095 | abhinavgummadi.work@gmail.com | linkedin.com/in/abhinavgummadi

Education

University of Wisconsin - Madison — Madison, WI
B.S. Double Major in Computer Science and Computer Engineering — *Est. May 2027*

University of Texas at Dallas — Richardson, TX
B.S. Computer Engineering (GPA: 3.87) — *Aug 2023 - May 2025*

Projects

SRAM Design: | *Virtuoso, HSpice, WaveView, PrimeTime, Calibre* — May - June 2025

- Designed 6T, 8T, and 10T SRAM cells, balancing storage density and read/write stability between design
- Created layouts in Virtuoso, Simulated designs in HSPICE, analyzed read-write delays with WaveView; used PrimeTime for static timing analysis (STA)
- Achieved functional cell designs with small delays and power efficiency, suitable to develop larger SRAM arrays

8-Bit Adder ASIC: | *HSpice, Verilog, Innovus, Abstract View, PrimeTime, Calibre* — April - May 2025

- Designed a 8-bit ripple-carry adder in Verilog, emphasizing area minimization by leveraging previously built standard cells library (D-FF, INV, NAND2, NAND3, XNOR2, OAI22, NOR2)
- Built ASIC using Abstract View and Innovus for design, placement, and routing; verified functionality via SPICE testbenches and HSPICE simulations
- Conducted Static Timing Analysis with PrimeTime, ensuring robust timing closure and minimal time delays

Flip-flop Design: | *Virtuoso, HSpice, WaveView, Abstract View, Calibre* — Jan - March 2025

- Designed a rising edge D flip-flop with synchronous reset functionality, optimized for area efficiency
- Simulated design in HSPICE, verified functionality and measured delays (setup, hold, clock-¿Q) with WaveView
- Created schematic and layout designs in Virtuoso, placement for Poly-Silicon placement, and M1 routing

Logic Gate Layout and Schematics: | *Virtuoso, HSpice, WaveView, SiliconSmart, Calibre* — Jan - Feb 2025

- Designed logic cells, including INV, NAND2, NAND3, XNOR2, OAI22, and NOR2, for use in VLSI/ASIC libraries
- Created schematic and layouts in Virtuoso; verified functionality with HSPICE simulations and Waveform analysis
- Optimized designs for area efficiency while minimizing power requirements and parasitic capacitance

Experience

Autonomous Vehicle Engineer — Sept. 2023 – May 2025
NOVA - University of Texas at Dallas — *Richardson, TX*

- Worked with different engineering teams to research, design and develop an open-source self-driving car, achieving Level 4 autonomy
- Refined computer vision platform, including LiDAR, GNSS, and ZED; Optimized and Refined autonomous systems with CARLA and ROS to train vehicle model for object detection, point-cloud processing, and route planning
- Deployed upgraded Onboard Computer, integrated NVIDIA AGX computer, stitching ZED camera footage, and developing motor firmware for a 1/3 scale car to enhance automation capabilities and kickstart

Technical Skills

Languages: C/C++, Assembly, VHDL, Verilog/SystemVerilog, SPICE, TCL, Python, Perl, Shell
Skills: Static Timing Analysis (STA), Routing and Placement, DRC/LVS, Synthesis, Testbench Development, Cell/System Simulation, CMOS Design
Software Tools: Linux, Virtuoso, Vivado, Innovus, Primetime, WaveView, HSPICE, Abstract View, Design Vision, PrimeLib, Calibre, Library Compiler, SiliconSmart ACE
Coursework: VLSI Design, Digital Design, Signals and Systems, Electronic Circuits, Computer Architecture
Soft Skills: Communication/Teamwork, Curiosity, Adaptable, Resilient/Driven, Openness