No. L. S.- 3961038

B/C.–(T).E–2/S/'15

Signature of Invigilator

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West Bengal State Council of Technical Education

MCQ Question. EXAMINATION

Subject.....

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(i) The three main components of a digital Computer system are —
(a) Memory, IO, DMA (b) ALU, CPU, Memory (c) CU, ALU, Register
(d) CPU, Memory, IO

(ii) Second generation of Computer used → (a) transistor (b) IC (c) Vacuum tube
(d) LSI

(iii) Processor of all computers, whether micro, mini or mainframe must have — (a) ALU (b) Primary Storage (c) Control Unit (d) all of these.

(iv) In which addressing mode is operand specified in the instruction itself? (a) Register mode (b) Immediate mode (c) Direct addressing mode
(d) Index addressing mode.

(v) The instruction LOAD is a — (a) zero address (b) one address instruction
(c) two addressing instruction (d) three-addressing instruction.

(vi) The number of fatch operation to execute instruction in immediate mode is — (a) 0 (b) 1 (c) 2 (d) none of these.

(vii) The instruction 1111 1111000011 00 is a — (a) direct memory reference instruction (b) indirect memory reference instruction (c) register reference instruction (d) input-output instruction.

NB: Register Ref. → 0 | 111 , memory Ref. (Indirect) 1 | 001 ('0' for direct ↑ opcode other than 111)

Input-output Ref — 1 | 111

(viii) 01110000 represents (a) 0 (b) NaN (c) $+\infty$ (d) $-\infty$

(ix) The largest floating point number that can be represented by 8 bit is — (a) 01111111 (b) 11111111 (c) 01101111 (d) 01111110

(x) If 'n' is number of bits in exponent, the bias number can be calculated as (a) $2^n - 1$ (b) 2^n (c) 2^{n+1} (d) $2^{n-1} - 1$

(xi) In Booth's algorithm, if the multiplier has 'n' bits then the multiplicand should have — (a) 1 bit (b) n-bits (c) n+1 bits (d) 2n bits

(xii) k-way set associative means — (a) K-blocks are present in a set (b) k-set are present in a block (c) K-set are present in the cache (d) none of these

(xiii) A typical modern computer uses — (a) LSI chip (b) VLSI chip (c) valves (d) vacuum tube.

(xiv) A subtractor is not usually present in a computer because — (a) it is expensive (b) It is not possible to design (c) the adder will take care of subtraction (d) none of the above.

(xv) The instruction 0101 111100001100 is a — (a) direct memory reference instruction (b) Indirect memory reference instruction (c) register reference instruction (d) input-output instruction.

0/1 | 000 to 110 memory ref. instruction

Direct Indirect

(xvi) If we want an addition/subtraction circuit to do subtraction, the initial value of carry in should be — (a) -1 (b) 0 (c) 1 (d) 2

(xvii) In auto increment addressing mode the value of the register is incremented by 1 ____ the execution of the instruction ____
(a) before (b) after (c) during (d) not in the list.

(xviii) Virtual memory is — (a) Primary memory (b) Secondary memory.
(c) both of these (d) none of these.

(xix) Direct memory mapping is — (a) one to one mapping (b) many to many mapping (c) many to one mapping (d) all of these.

(xx) In associative mapping technique, number of comparators required is — (a) 1 (b) 2 (c) equal to the number of blocks in main memory (d) equal to the number of lines in cache memory

(xxi) If the negative number are stored in 2's complemented form, the range of numbers that can be stored in 8 bits is ____
(a) −128 to +128 (b) −128 to +127 (c) −127 to +128 (d) −127 to +127

(xxii) The cost of storing a bit is minimum in —
a) Cache memory b) Register c) RAM d) Hard disk

(xxiii) Tera is '2' to the Power of — (a) 10 (b) 20 (c) 30 (d) 40

(xxiv) In 'immediate addressing the operand is placed —
(a) in the CPU register (b) after opcode in the instruction
(c) in memory (d) in stack.

(xxv) The instruction ADD is ____ addressing instruction —
a) 0 b) 1 c) 2 d) 3

(xxvi) Negative number can be represented in — (a) Sign-magnitude form
(b) 1's complent form (c) 2's complent form (d) all of the above.