B.Tech Third Year 6th Semester Examination
Department: Computer Science and Engineering
Course Name: Operating System Code: CS 341
Full Marks-100 Time: 3 hours

1. A computer uses 46–bit virtual address, 32–bit physical address, and a three–level paged page table organization. The page table base register stores the base address of the first–level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second–level table (T2). Each entry of T2 stores the base address of a page of the third–level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes. What is the size of a page in KB in this computer? 10

2. A memory management system has 64 pages with 512 bytes page size. Physical memory consists of 32-page frames. What is the number of bits required in logical and physical address?

4

3. Consider the following page reference string : 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.
Calculate the correct number of page faults related to LRU, FIFO and optimal page replacement algorithms, respectively, assuming 05-page frames and all frames are initially empty.

12

4. Consider the two-dimensional array A:
int A[][] = new int[100][100];
where A[0][0] is stored at location 200, in a paged memory system with pages of size 200. A small process resides in page 0 (locations 0 to 199) for manipulating the A matrix; thus, every instruction fetch will be from page 0.
For three-page frames, how many page faults are generated by the following array initialization loops, using LRU replacement, and assuming page frame 1 has the process in it, and the other two are initially empty:

a.
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for( int j = 0 ; j < 100 ; j++ )
        for( int i = 0 ; i < 100 ; i++ )
                A[i][j] = 0;
```

b.
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for( int i = 0 ; i < 100 ; i++ )
        for( int j = 0 j < 100 ; j++ )
                A[i][j] = 0;
```
5

5. Consider a demand-paging system with the following time-measured utilizations:
CPU utilization 20%
Paging disk 97.7%
Other I/O dev. 5%
For each of the following, say whether it will (or is likely to) improve CPU utilization.

Explain your answers.

a. Install a faster CPU.
b. Install a bigger paging disk.
c. Increase the degree of multiprogramming.
d. Decrease the degree of multiprogramming.
e. Install more memory.
f. Install a faster hard disk, or multiple controllers with multiple hard disks.
g. Increase the page size. 14

6. Write a short note on the following: 5x4=20

a. Internal and External fragmentation
b. Paging and Segmentation
c. File allocation policies
d. Directory structures
e. File system structure

7. What are the various kinds of performance overhead associated with servicing an interrupt? Explain steps of direct memory access. 5+3=8

8. What do you mean by RAID structure? Also discuss different types of RAID levels. 2+6=8

9. Discuss the strengths and weaknesses of implementing an access matrix using capabilities that are associated with domains. 5

10. Consider a 128 KB program to be loaded from the disk have 1 rotation time of 20 ms. The total size of the track is 64 KB and average seek time of disk is 30 ms. The paging is applied on program and program is divided into pages of size 4KB. Assume that pages are spread randomly over the disk. Then how much time is required to load the program from the disk? 8

11. Suppose a disk has 250 cylinders, numbered from 0 to 249. At some time, the disk arm is at cylinder 100, and there is a queue of disk access requests for cylinders 10, 25, 30, 85, 90, 100, 105, 110, 135, 145 and 245. If Shortest-Seek Time First (SSTF) is being used for scheduling the disk access, the request for cylinder 90 is serviced after servicing how many requests? 6