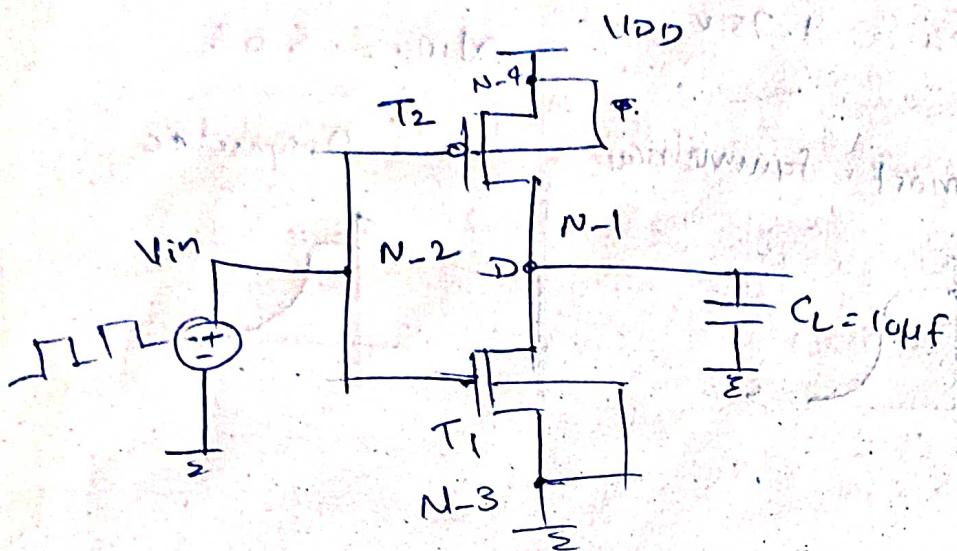


3 / ULSI Design Tools

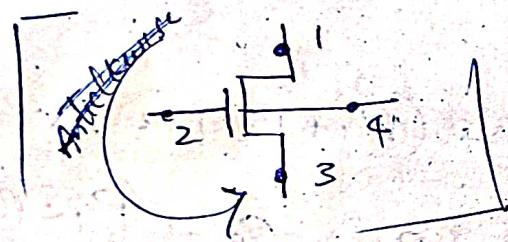
• netlist



Schematic

netlist

Simulation



$$W = 1.5L \quad (\text{min.})$$

Condition

$$\frac{W_P}{W_N} = \frac{\mu_N}{\mu_P} = (2-3)$$

lib '45nm lib' MOS

must \leftarrow MT1 N-1 N-2 N-3 N-3 L=45nm W=90nm
 pmos
 MT2 N-1 N-2 N-4 N-4 L=45nm W=180nm

C_L N-1 gnd 10fF

V_{DD} N-4 gnd 1V

V_{in} N-2 gnd pulse (0 1 0 1n 1n 10n 20n)

[Pulse (V_i , V_f , T_r , T_f , P_w , P_f)]

Analysis

• trau → Time

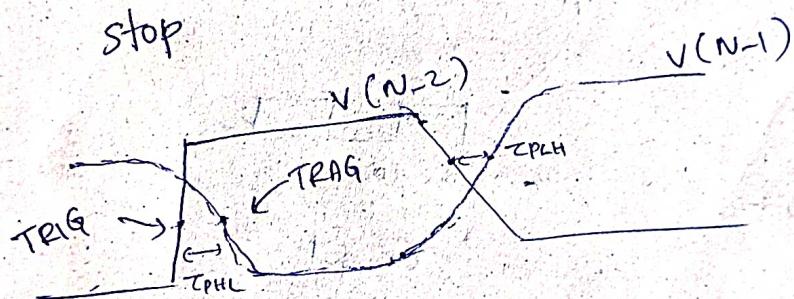
• DC → Voltage

• AC → Frequency

① trau

• trau start stop step
loop 0.1n → understand

• Print $V(N-1) \dots V(N-2)$



Area:

Delay:

$$T_d = T_{PHL} + T_{PLH}$$

measure

TRAN

T_{PHL}

TRIG $V(N-2)$ $V_{DL} = 0.5$

$T_0 = 0$ RISE = 1

TRIG $V(N-1)$ $V_{DL} = 0.5$

FALL = 1

T_{PLH} $V(N-2)$ " " FALL

$V(N-1)$ " " RISE =

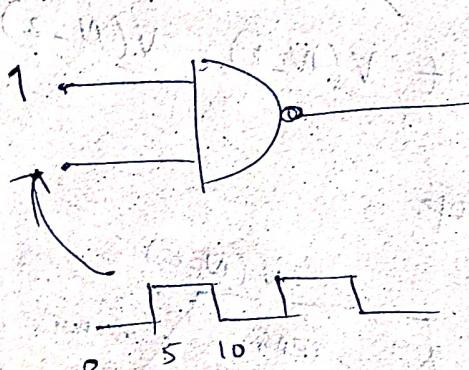
measure TRAN TP PARAM = $(TPHL + TPLH)$

Power Analysis: measure Avg-Power Avg Power from $= 0.1 \text{ nJ}$ Toc 2nd

for DC: VDD = N-4 and 1V
V_{thm} = N-2 and 1V

.dc Vin 0.1 0.01

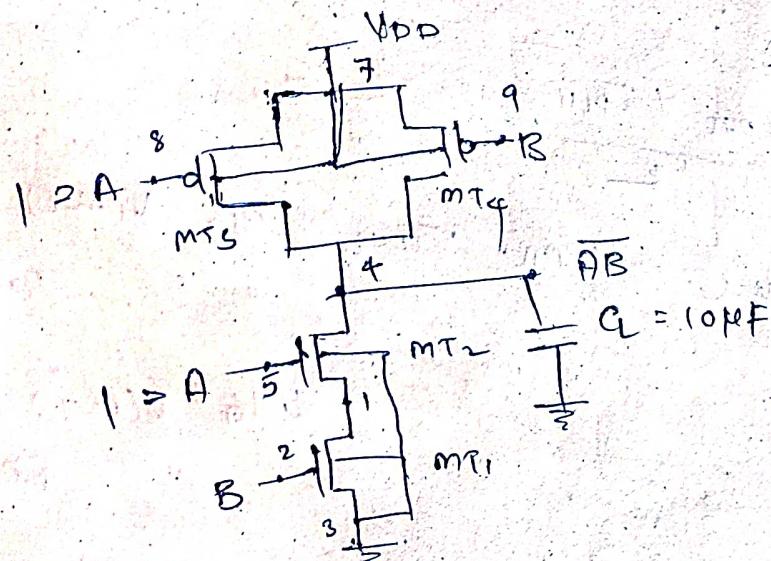
Eg: Write the net list



$$t_r = 1$$

$$t_f = 1$$

Time Scale "ns"



lib

MT₁ N-1 N-2 N-3 N-3 L=45nm W=90nm
~~MT₂~~ N-4 N-5 N-4 N-8 L=45nm W=180nm

MT₃ N-5 N-1 N-3 L=45nm W=90nm

MT₂ N-4 N-4 L=45nm W=180nm

MT₃ N-4 N-8 N-7 N-7 L=45nm W=180nm

MT₄ N-4 N-8 N-7 N-7 L=45nm W=180nm

CL N-4 gnd 10μ

V_{DQ} N-7 gnd 1V

V_{DS} N-8 gnd ()

V_G N-9 gnd pulse ()

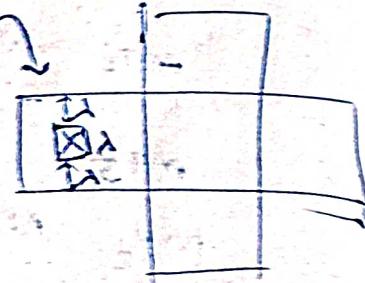
V_C N-2 gnd 1V

V_G N-5 gnd ()

"TRANSISTOR SIZING"

$$W = B\lambda \quad \text{Depending on Specs}$$

$$\lambda = \frac{L}{2}$$



$$\text{So, } W_{\min} = 1.5L$$

$$T_{PCH} = T_{PHL}$$

$$\frac{w_p}{w_n} = (2-3)$$

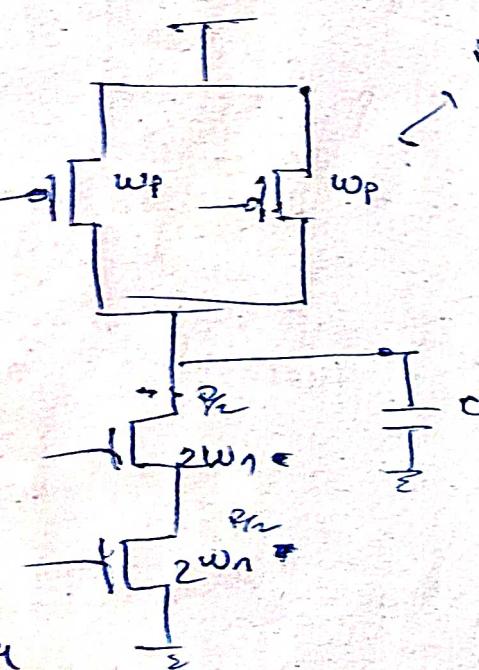
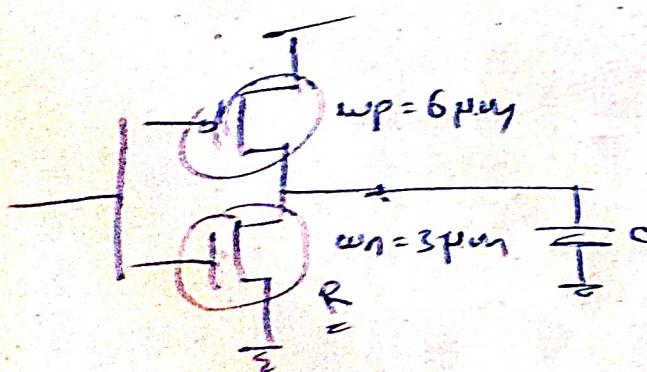
Let say $w_p = 2w_n$

$$L = 2 \mu m$$

$$w_p = 6 \mu m$$

$$w_n = 3 \mu m$$

NAND Gate Size:

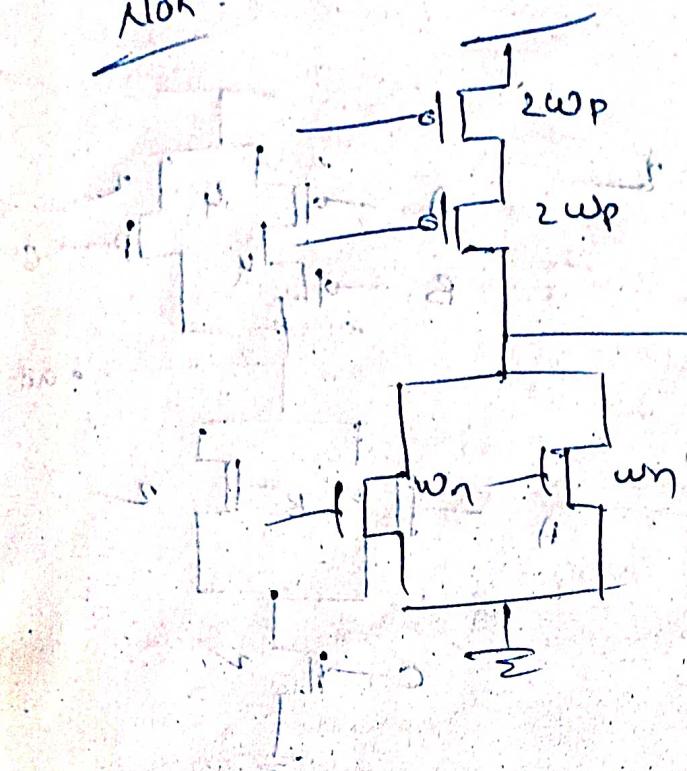


Most other
only
Transistor is

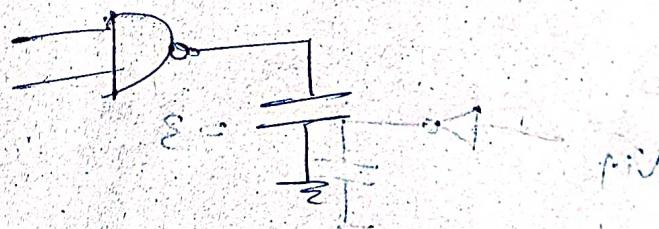
Delays should be
same w.r.t. inputs

• Both should drive the Capacitance at equal rate

NOR:

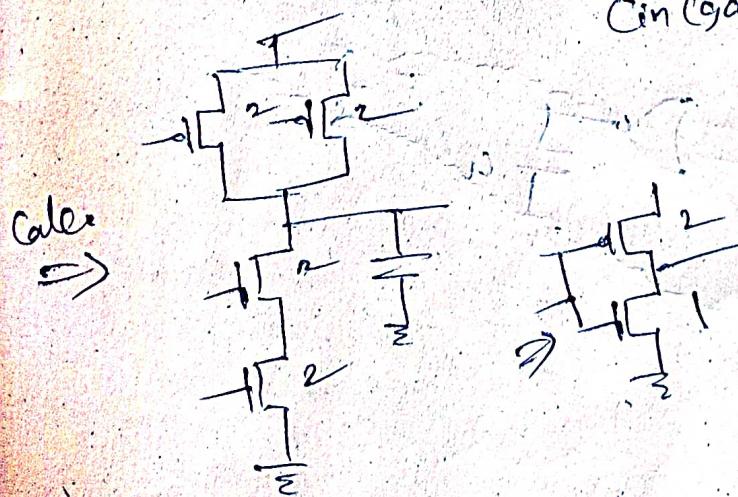


~~logical effort~~ $(g_f) \geq 1$ (except inverter)
 $(g=1)$



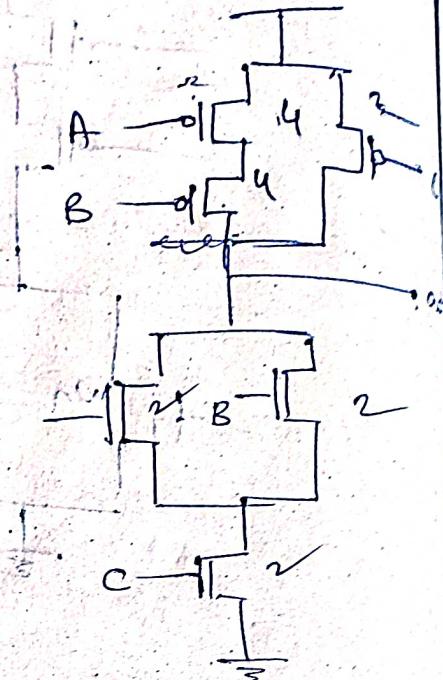
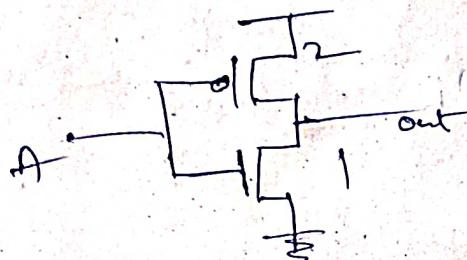
$$\Sigma g = \frac{C_{in}(\text{gate})}{C_{in}(\text{inv})} = \frac{4}{3} \text{ (nand)} = 1.33$$

$$C_{in}(\text{gate}) | \text{nand} = \frac{4C_p}{3C_p}$$



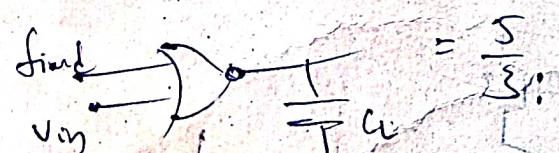
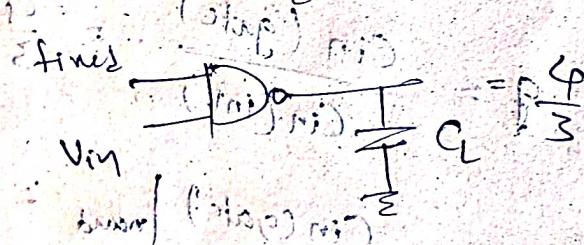
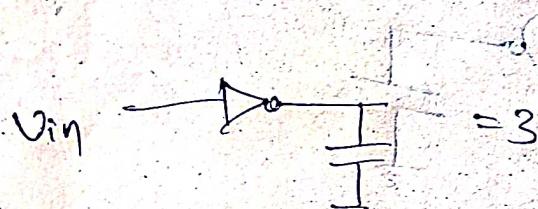
$$NOR = \frac{5}{3}$$

$$\underline{\text{Eg:}} \quad \overline{(A+B)C} = ?$$

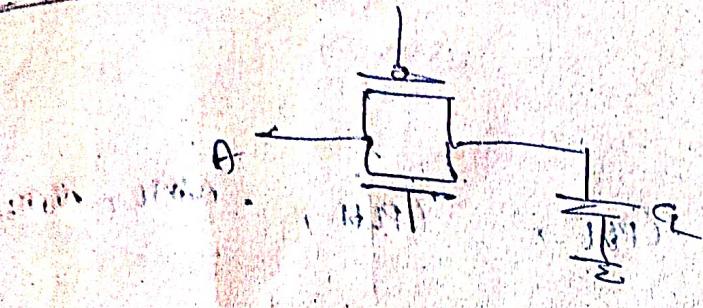


(After drawing) we get

\therefore drawing input = $(A+B)C$



why not?



inverted output of in.

$$g = \frac{2}{3}$$

Cmos inverter is more sustainable to noise.

(Assign)

1) • de / NM \rightarrow 350 nm

2) • trn / P.D delay

3) • ac T_{ATL}, T_{PLH}, T_p

a) Write the netlist for the NAND gate to perform transient / AC / DC analysis. Using also for CMOS inverter

b)

• lib 'Nmos.lib' nmos

• lib 'pmos.lib' pmos

m₁ 1 2 0 0 nmos

m₂ 1 2 9 9 pmos

