Novel QCA-Based Single-bit Comparator Circuit AND Fault tolerance analysis

ABHIVARDHAN TIPPANI

ELECTRIC COMMUNICATIONS ENGINEERING

INDIAN INSTITUTION OF INFORMATION TECHNOLOGY,SRICITY

abhivarhdan.t2 l @iiits.in

ABSTRACT:
In order to maximize performance and efficiency, a novel 1-bit comparator circuit architecture based on (QCA) is presented in this study. Our design outperforms traditional CMOS-based systems in terms of functionality, speed, and energy economy by utilizing the special qualities of QCA. We validate the feasibility and superiority of our new QCA-based comparator design through comprehensive simulation tests. By advancing QCA-based digital circuit design, this research opens the door for the development of next-generation computer systems.

Section 1

INTRODUCTION: This research document develops and analyzes a QCA-based 1-bit comparator circuit in order to investigate a novel way of digital circuit design. Comparators are essential components of digital systems that support mathematical operations and critical decision-making processes. This study aims to achieve two main goals: firstly, it presents a novel approach to design for QCA-based 1-bit comparators that optimizes performance and efficiency; secondly, it does a thorough examination of the functionality, fault tolerant analysis.

Following is the structure of this research paper: In Section 2, (QCA) are thoroughly introduced, with its benefits, drawbacks, and fundamental ideas explained. With a focus on important architectural breakthroughs and optimization techniques, Section 3 discusses the literature rivews of the papers, Section 4 presents our unique design approach for the QCA-based 1-bit comparator circuit. An analysis of the circuit's performance metrics and a comparison with traditional designs are provided in Section 5, which also shows the findings of comprehensive simulation studies. In summary, the paper's major conclusions, ramifications, and directions for further research are covered in Section 6.

Section 2

Overview of the QCA Designer's 1-Bit Comparator Circuit:
A new nanotechnology called (QCA) uses the ideas of quantum mechanics to create and implement nanoscale digital circuits. Quantum dots are used by QCA devices as cellular automata to carry out logic operations. In this case, comparing two binary inputs inside the QCA paradigm requires the use of a 1-bit comparator circuit.
Context: QCA technology marks a move away from conventional silicon-based electronics and toward more compact and energy-efficient computing. Utilizing quantum dots that interact via Coulombic interactions, QCA makes it possible to design high-speed, compact digital circuits.
Functionality: Using QCA cells, a 1-bit comparator in QCA carries out the same basic task as its classical counterpart. It accepts a pair of binary inputs and outputs whether they are equal or one is greater than the other. The QCA designer manipulates the polarization states of quantum dots through logic operations.
Uses:
Ultra-Compact Computing: Because quantum dots are so tiny, QCA circuits have the potential to enable incredibly small-scale computing.
Low Power Consumption: When compared to traditional electronic equipment, QCA products have the ability to drastically cut power consumption.
High-Speed Operations: QCA circuits have the capacity to work quickly, which speeds up computation for some uses.

The purpose of the QCA Design is:
Utilizing the size, speed, and energy efficiency advantages of is the main goal of building a 1-bit comparator circuit in QCA. The goal of the design is to show that quantum-dot interactions can be used to create digital logic operations.

The objective of this project is to demonstrate and investigate the use of QCA Designer for the implementation of a 1-bit comparator. This research aims to explore the theoretical underpinnings of QCA, elucidate the design concepts of the 1-bit comparator, and showcase simulation outcomes that showcase its operational capabilities. Discussions of the difficulties, possible improvements, and wider ramifications of QCA technology in computing in the future are also covered.

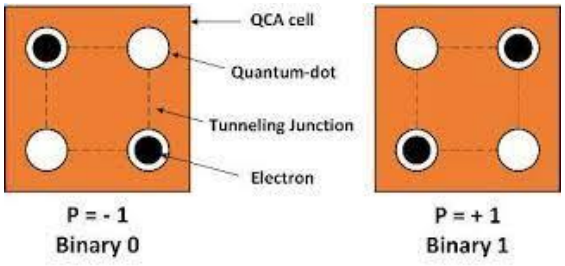

FIG 2.0 Representation of QCA Cell

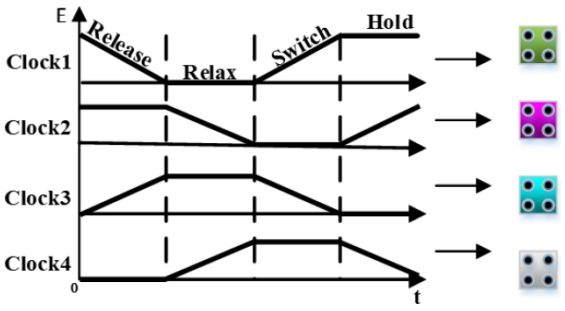

FIG 2.1 Clock Representation in QCA

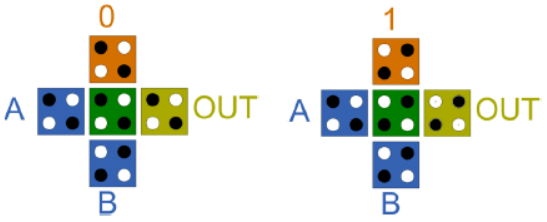

FIG 2.3Representation of QCA Majority gate

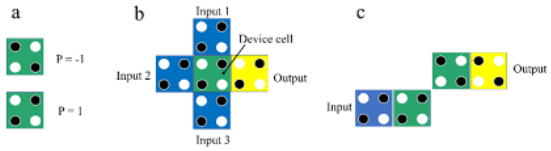

FIG2.4 Representation of 3 input majority gate(b)&inverter(c).

Section 3

Literature reviews:

Paper 1:

The study highlights the reduced size and lower power consumption of (QCA), a nanotechnology substitute for CMOS in logic circuits and VLSI devices.
Comparator with a single bit: A brand-new, 0.07 square micrometer single-bit comparator design based on QCA is put forth, using a mere 39 quantum cells.
Benefits of Design: In comparison to earlier studies, the suggested comparator design uses fewer cells, takes up less space, and runs on a single layer without crossings.
Future Applications: According to the study, the suggested comparator may one day be utilized to create intricate logical and arithmetic circuits.

Paper 2: The paper presents a (QCA) layout strategy for designing memory blocks and Configurable Logic Blocks (CLBs) for Field Programmable Gate Arrays (FPGAs). In order to get around CMOS technology's drawbacks, effective QCA-based circuit designs are suggested. The approach is centered on maximizing area, delay, complexity, and number of cells for better FPGA performance and lower costs. New building blocks, like D-Flip Flops, memory cells, multiplexers, and decoders, are suggested and compared to current architectures. The results show increased cost-effectiveness and reliability, and they may be applied to embedded systems based on FPGAs. The study comes to the conclusion that, in comparison to existing alternatives, the suggested strategy and blocks offer faster, more dependable designs.

Paper 3:

QCA Technology: Because of its fast speed and low power consumption, QCA is a promising nanotechnology that may eventually replace CMOS in VLSI circuits.
Comparator Design: This design is the most area-efficient to date because it only requires 14 cells in the comparator circuit.2.
Realization of Logic Gates: In addition to majority and universal gates in QCA, the comparator circuit may also create fundamental digital logic gates.

Paper 4 :

QCA Technology: Using fundamental components such as QCA cells and gates like inverters, majority, and XOR gates23, the research addresses QCA as a viable technology for nano-scale digital circuits.
Comparator Design: Compared to earlier designs, a novel 1-bit comparator circuit is suggested that is more efficient in terms of size, cell count, and delay.4. Simulation Results: QCADesigner is used to model the suggested design, which reveals that it only needs 38 QCA cells, 0.03 µm2 of area, and a 0.5 clock cycle delay.

Paper 6: The research presents new topologies for XNOR gates.
Novel Structures: Three novel XNOR gate structures are put forth that depart from traditional logic gate designs by utilizing the built-in capabilities of QCA technology.
Simulation and Comparison: Simulation is used to verify the suggested structures and comparator design. The results are encouraging when compared to previous designs found in the literature.

Paper 7:

Design Innovations: It highlights the reduced size and cell complexity of optimized designs for a 1-bit comparator and a complete adder in QCA.
Performance Analysis: The suggested designs outperform conventional systems in terms of energy usage and quantum cost.
Simulation Results: The QCADesigner program is used to verify the designs' operational usefulness by testing their stability under temperature variations.

Paper 11:

Innovative Designs: Compared to current single-layer and some multilayer designs, it suggests more efficient designs for ripple carry adders, ripple borrow subtractors, full adders, and full subtractors.
Design Advantages: The suggested designs are comparable with multilayer designs due to their benefits in circuit area, latency, and cell count.
Implementation and Verification: To ensure the viability and efficiency of each suggested design, QCADesigner was utilized for implementation and verification.

Paper 21:

Provides a ground-breaking method of computing at the nanoscale with the promise for exceptionally fast, incredibly low power, and extremely dense circuits. Full Comparator Design: Using just one clock cycle, the suggested design is more effective than the previous one, with notable gains in cell count, area, and delay.
Simulation Results: The developed circuit's accurate logical function was confirmed through simulation using the QCA Designer tool.

Paper 24: It draws attention to the problems and solutions involved in developing system architectures based on QCA.
Design Challenges: It describes certain difficulties, like timing and layout concerns, that were discovered during the preliminary designs of QCA microprocessor components and offers floor planning strategies as solutions.
Clocking Methodology: The multi-phased clocking technique, which is crucial for QCA functioning and is quite different from CMOS designs, is explained in this document.

Further Directions: The article makes several recommendations for further study, such as finishing up the architecture of the Simple 12 microprocessor, dealing with problems with long wire and signal routing, and looking into architectural possibilities for multithreading in QCA.

Paper 25:

Quantum-Dot Cells: The study looks into cells made of two-electron quantum dots.These cells use Coulombic forces to connect with nearby cells.

Binary Encoding: The ground-state polarization is controlled by the polarizations of nearby cells. The polarization of the cells, which results from electron alignment, encodes binary information. According to the paper, a linear array of these cells has the ability to convey binary information through polarization states and function as a binary wire.

Computational Model: The arrays are analyzed using a Hartree self-consistency scheme, which demonstrates that the cells may reliably transfer the encoded information and act as wires in quantum cellular automata.

Section 4

PROPOSED WORK:

In this research paper, the proposed single-bit single layered comparator circuit layout is designed using default simulation setup of QCA Designer tool.

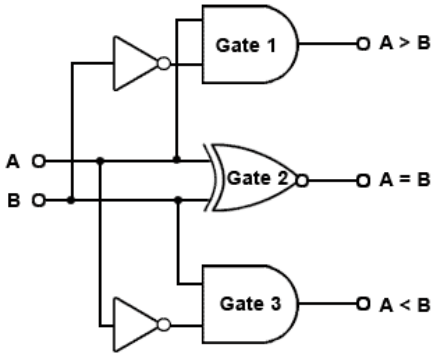

FIG 4.1 LOGIC DESIGN OF 1-BIT COMPARATOR CIRCUIT

The schematic of the comparator circuit consists of the different logic gates. Two NOT gates, two AND gates, and one XOR gate are utilized for the proposed comparator circuit.

Inputs		Outputs		
B	A	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

TABLE 4.1 LOGIC FLOW IN COMPARATOR CIRCUIT

Three input majority gates with a fixed polarity of -1—which function as the AND gate—QCA inverters, which are created by arranging the cells diagonally, and a strong XNOR gate design are used to realize the QCA circuit. The layout that has been suggested is

as shown in Figure 9. Here, A_E_B indicates that A = B, A_G_B indicates that A > B, and A_L_B implies

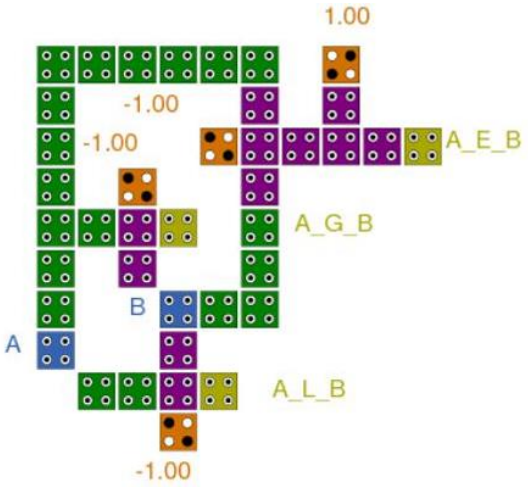

FIG 4.2 Previously designed 1 bit comparator

circuit When constructing comparator circuits, the majority gate theory is applied, and QCA cells are used to construct basic logic circuits. With 39 cells, the mentioned single-bit comparator circuit occupies 0.04 square micrometers of space. The proposed design has a delay of 0.5 since it utilizes two clock pulses throughout.

Novel 1 bit comparator circuit

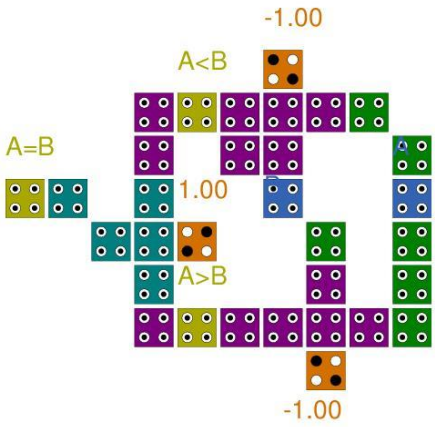

FIG 4.3 Novel 1 bit comparator circuit

SIMUALATION AND RESULTS:

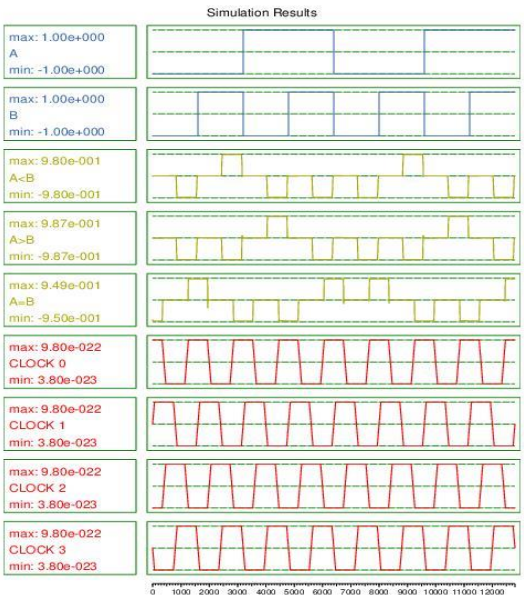

Fig 4.4 simulation result of the circuit

The both the logics are same but difference in implementation the both follows logic A<B – A'B

A>B – AB'

A=B – A'B'+AB

And the table 2.1 and the out puts are same the difference between Fig 2.1 and Fig2.2 is difference of no.of cells and the area of the novel circuit is 0.042 μm^2

Power analysis:

Power analysis of the novel 1-bit comparator circuit in QCA gives important new information on the design's energy consumption and efficiency. The objectives of this study were to evaluate the power metrics, identify possible areas for optimization, and to understand how the circuit functions under different scenarios.

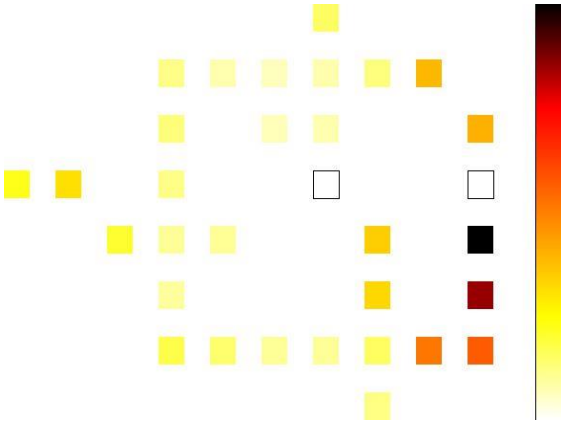

Fig 4.5 QCA pro circuits layouts

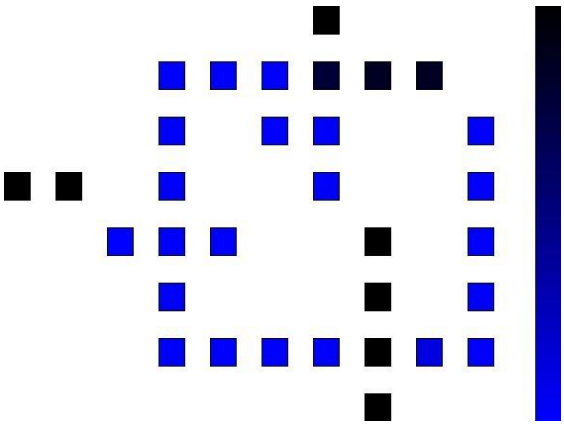

Fig 4.5 QCA pro circuits layouts

Section 5

FAULT TOLERANCE:

When discussing QCA, fault tolerance refers to a system's capacity to maintain dependability in the face of flaws or imperfections. Based on the

concepts of quantum physics, are a nanotechnology-based computing paradigm that employs quantum dots to represent binary information.

- QCA devices are subject to faults and defects like any other physical system, which might arise from manufacturing flaws, environmental factors, or radiation-related problems.
- QCA defects might appear as misplaced or absent quantum dots, lattice structure disruptions, or other physical flaws.
- Fault-tolerant QCA circuit design and implementation are being investigated by researchers. This entails creating circuits based on QCA that can identify flaws and lessen their effects in order to maintain operation.
- QCA is inherently robust because of its quantum-level construction. A considerable amount of fault tolerance is provided by the inherent interaction between the quantum-dot cells and Coulombic forces.

Missing cell defect:

- A missing cell defect in (QCA) is the lack or failure of a quantum-dot cell in the QCA lattice structure. The quantum characteristics of electron charge are used by QCA, a computing paradigm based on nanotechnology, to represent binary information. In a QCA device, every quantum-dot cell contributes to the system's overall performance.
- It occurs when the cell in the at any position is fault or failed or missing from the actual position is called the missing cell defect.
- It will arise when the manufactur imperfections or due to environment changes or impact of the other factors.

Similar to this new circuit, there are 24 possible configurations for the circuit, and each one has a distinct binary number output.
Order of the cells:

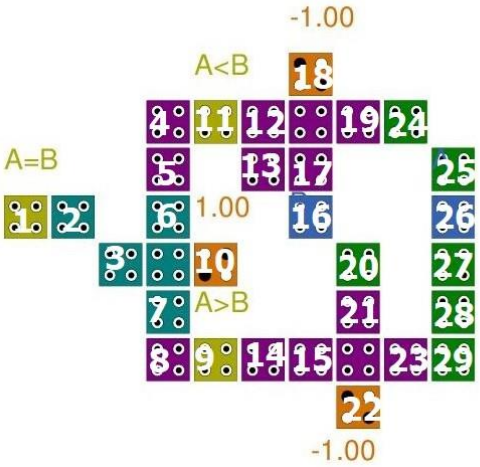

Fig 4.6 Numbering of the missing cell defect

Table 5.1

Cells	A=B 1001	A>B 0100	A<B 0010	Fault bits of 12bits
1.	0000	0100	0010	2/12
2.	0010	0100	0010	3/12
3.	0010	0100	0010	3/12
4.	0000	0100	0010	2/12
5.	0000	0100	0010	2/12
6.	0000	0100	0010	2/12
7.	0000	0100	0010	2/12
8.	0000	0100	0010	2/12
9.	0010	0100	1100	2/12
10.	1001	0100	0010	0/12
11.	1001	0100	0010	0/12
12.	0000	0100	1111	5/12
13.	0011	0100	1111	5/12
14.	0000	1111	0010	5/12
15.	1011	0100	0000	2/12
16.	1101	0000	0010	2/12
17.	1101	0000	0010	2/12
18.	0000	0000	0010	3/12
19.	1011	0100	0000	2/12
20.	1110	0000	0000	5/12
21.	1011	0100	0000	2/12
22.	1001	0100	0010	0/12
23.	1101	0000	0010	2/12
24.	1101	0000	0010	2/12
Total				58/288

From the table 2.2 the cell numbers are given by each column top to bottom respectively.
A=B is the outputs of the each case and A>B and A <B are also accordingly .

The total no of fault bits are 58 and total no.of outputs are 288=0.201
Therefore the percentage is 20.138%

Cell addition defect:

A cell addition defect in (QCA) is a problem in which there is an additional quantum-dot cell in the QCA lattice structure, or when the extra cell is incorporated incorrectly. The quantum characteristics of electron charge are used by QCA, a model of computing based on nanotechnology, to represent binary information. In a QCA device, every quantum-dot cell plays a part in the overall system performance.

- When an additional quantum-dot cells is added or improperly integrated into the QCA lattice structure defect results erros in the manufacturing process depature from the design brief or external circumstances affecting the QCA device's sturcural integrity could all lead to this flaw.
- A second quantum dot cell circuits ability to function normally.It might obstruct the flow of information computational processes,and genral impacted region operation,which could result in accurate results and system failures.

As in this novel circuit there are 33 possibilities around the circuit and each one have unique output in forms of binary numbers.

Order of the cells:

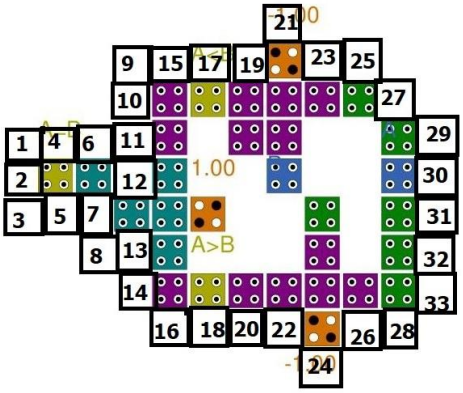

Fig 4.6 Numbering of Cell addition defect

Table 5.2

Cells	A=B 1001	A>B 0100	A<B 0010	Fault bits of 12bits
1.	1001	0100	0010	0/12
2.	0000	0100	0010	2/12
3.	1001	0100	0010	0/12
4.	0000	0100	0010	2/12
5.	0110	0100	0010	2/12
6.	0110	0100	0010	2/12
7.	1111	0100	0010	2/12
8.	1001	0100	0010	0/12
9.	1111	0100	0010	2/12
10.	0000	0100	0010	2/12
11.	1001	0100	0010	0/12
12.	0110	0100	0010	4/12
13.	1001	0100	0010	0/12
14.	1000	0100	0010	1/12
15.	1001	0100	0010	0/12
16.	1001	0100	0010	0/12
17.	1001	0100	0010	0/12
18.	1001	0100	0010	0/12
19.	1011	0100	0000	2/12
20.	1101	0000	0010	2/12
21.	1100	0100	0010	2/12
22.	1101	0000	0010	2/12
23.	1001	0100	0010	0/12
24.	1001	0100	0010	0/12
25.	1001	0100	0010	0/12
26.	1101	0000	0010	2/12
27.	1010	0100	0000	3/12
28.	1101	0000	0010	2/12
29.	1001	0100	0010	0/12
30.	1001	0100	0010	0/12
31.	1001	0100	0010	0/12
32.	1001	0100	0010	0/12
33.	1001	0100	0010	0/12
total				34/396

The table 2.3 defines the total fault percentage of the circuit when the cell addition defect is applied

I.e 34/396=0.085x100
=8.58%.

Research is still being done to reduce manufacturing flaws and increase the general resilience of QCA devices.

The goals of continuous improvement are to increase QCA-based computing security and address problems associated with cell addition faults.

CELL DIPLACEMENT DEFECT:

- A quantum-dot cell that is displaced or positioned improperly within the QCA lattice results in a cell displacement fault. The QCA device's structural integrity may be impacted by environmental variables, design parameters being violated, or manufacturing faults.
- Initially the quantum-dot cells are arranged as per the regular lattice

structure then each cell is displaced from the regular position then the output vary and that is moved in horizontal and vertical direction as per requirement Appropriate configuration guarantees effective Coulomb interactions for trustworthy data processing.

- Any of the four directions—East, West, North, and South— may be the source of this displacement. Each cell was moved in every direction that was feasible, and we measured the farthest distance at which the necessary outputs could be obtained

Order of the cells:

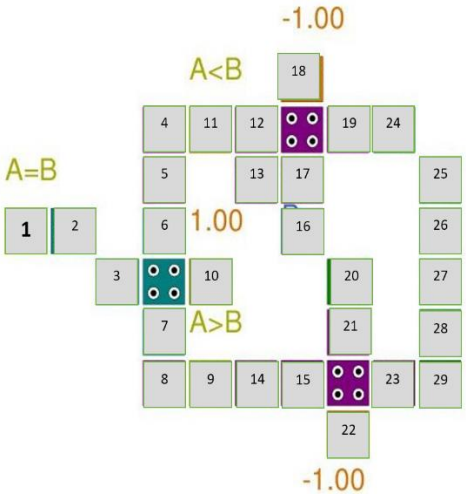

Fig 4.6 Numbering of CELL DIPLACEMENT DEFECT

Table 5.3

Cells	Horizontal		Vertical	
s.no	+ve	-ve	+ve	-ve
1.	NA	-17	17	-7
2.	11	NA	7	-7.4
3.	NA	-1.8	2.5	-2.6
4.	NA	-5	NA	-6
5.	3	-2	NA	NA
6.	2	-1	NA	NA
7.	2	-2.6	NA	NA
8.	NA	-3	1	NA
9.	NA	NA	7	-5
10.	3	NA	7	-6
11.	NA	NA	5	-1
12.	NA	NA	NA	-4
13.	NA	✓	✓	NA
14.	NA	NA	✓	-17
15.	3	-0.3	NA	NA
16.	4	-1	2	NA
17.	2	NA	NA	NA
18.	5	-4	-12	NA
19.	NA	NA	3	-5
20.	1	-0.7	NA	-0.1
21.	0.2	-1	NA	NA
22.	6	-5	6	NA
23.	NA	NA	2	-0.3
24.	2	NA	5	-3
25.	7	-8	NA	-11
26.	7	-7	NA	NA
27.	✓	-9	NA	NA
28.	✓	-10	NA	NA
29.	0.07	NA	0.6	NA

The table 2.4 describe the where the fault occurs when we displaced the each individual bit
At the particular point the output will break and give the error output the points are given in the table

The values are the extreme point of getting the required output
NA implies that the cell didn't have the displacement availability in the that direction.
The(✓) implies the cells when they are displaced value 20,even though the out put are required output.

Comparison:

Table 5.4

Design or comparator	Cell count	Area(μm^2)	Latency (clock cycle)	Circuit cost
1[refered paper]	39	0.07	0.5	1.36
4	38	0.03	0.50	0.57
5	40	0.05	0.75	1.50
8	42	0.05	0.75	1.58
9	43	0.08	1.25	4.30
12	40	0.04	0.75	1.20
14	54	0.05	0.75	1.58
16	58	0.05	0.75	1.58
18	49	0.07	0.75	2.57
22	42	0.05	0.75	1.58
23	73	0.06	1.00	4.38
Proposed Novel circuit	32	0.05	0.50	1.2

Section 6:

Conclusion:

1-Bit Comparator Circuit: Compared to earlier designs, this new 1-bit comparator circuit in QCA is more area-efficient and requires fewer cells.
Fault Tolerance Analysis: This study examines how QCA devices handle faults, focusing on how reliable the system is when flaws or imperfections exist.Important insights into the circuit's robustness and reliability have been gained from the fault-tolerant analysis of the unique 1-bit comparator design in (QCA). The QCA lattice structure's inherent durability to some errors is demonstrated by the 1-bit comparator. The fault-tolerant study demonstrated that the circuit continues to function even when certain flaws are present, adding to the design's dependability.The purpose of this study was to investigate the fault-tolerant properties of the comparator and evaluate its performance in a variety of failure scenarios.

References:

[1] K. Anjalideep, H. Kumar, S. Srivastava and V. K. Sharma, "QCA-based Single-bit Comparator Circuit," *2022 3rd International Conference on Smart Electronics and Communication (ICOSEC)*, Trichy, India, 2022, pp. 328-332

[2] M. Raj, L. Gopalakrishnan, S. -B. Ko, N. Naganathan and N. Ramasubramanian, "Configurable Logic Blocks and Memory Blocks for Beyond-CMOS FPGA-Based Embedded Systems," in IEEE Embedded Systems Letters

[3] Chakrabarty, R., Roy, S., Pathak, T., & Mandal, N. K. (2021, December 1). *Design of Area Efficient Single Bit Comparator Circuit using Quantum dot Cellular Automata and its Digital Logic Gates Realization*. International Journal of Engineering. Transactions

[4] Shiri, A., Rezai, A., & Mahmoodian, H. (n.d.). *Design of efficient coplanar 1-bit comparator circuit in QCA technology*. \

[5] DESIGN OF EFFICIENT COPLANAR 1-BIT COMPARATOR CIRCUIT IN QCA TECHNOLOGY Ahmadreza Shiri, Abdalhossein Rezai, Hamid Mahmoodian ACECR Institute of Higher Education, Isfahan Branch, Isfahan 84175-443, Iran

[6] Single-bit comparator in (QCA) technology using novel QCA-XNOR gates Ali Hussien Majeed a,* , Mohd Shamian Zainal b , Esam Alkaldy a , Danial Md. Nor b a Department of Electrical Engineering, University of Kufa, Najaf, 54003, Iraq b Department of Electrical Engineering Technology, Universiti Tun Hussein Onn Malaysia, Parit Raja

[7] Abdullah-Al-Shafi, M., & Bahar, A. N. (2016, October 3). *Optimized design and performance analysis of novel comparator and full adder in nanoscale*. Cogent Engineering.

[8] D. Ajitha, K. V. Ramanaiah and V. Sumalatha, "A novel design of cascading serial bit-stream magnitude comparator using QCA," 2014 International Conference on Advances in Electronics Computers and Communications, Bangalore, India, 2014.

[9] *A Novel Full Comparator Design Based on - Volume 5 Number 6 (Nov. 2015) - ijiee*. (n.d.). https://www.ijiee.org/index.php?m=content&c=index&a=show&catid=59&id=630

[10] TY - JOUR AU - Tougaw, Douglas AU - Lent, Craig PY - 1996/11/01 SP - 4722 EP - 4736 T1 - Dynamic behavior of quantum cellular automata VL - 80 DO - 10.1063/1.363455 JO - Journal of Applied Physics ER -

[11] Labrado, C., & Thapliyal, H. (2016, March 1). *Design of adder and subtractor circuits in majority logic-based field-coupled QCA nanocomputing*. Electronics Letters.

[12] M. Goswami, B. Kumar, H. Tibrewal and S. Mazumdar, "Efficient realization of digital logic circuit using QCA multiplexer," 2014 2nd International Conference on Business and Information Management (ICBIM), Durgapur, India, 2014, pp. 165-170.

[13] Majeed, A. H., Alkaldy, E., Zainal, M. S., & Nor, D. M. (2019, June 1). *A new 5-input majority gate without adjacent inputs crosstalk effect in QCA technology*. Indonesian Journal of Electrical Engineering and Computer Science.

[14] Roohi, A., Thapliyal, H., & DeMara, R. F. (2015, October 1). *Wire crossing constrained QCA circuit design using bilayer logic decomposition*. Electronics Letters.

[15] Singh, G., Sarin, R. K., & Raj, B. (2016, March 14). *A novel robust exclusive-OR function implementation in QCA nanotechnology with energy dissipation analysis*. Journal of Computational Electronics (Print).

[16] S. Umira, R. Qadri, Z. A. Bangi and M. T. Banday, "A Novel Comparator-A Cryptographic Design in Quantum Dot Cellular Automata," 2018

International Conference on Sustainable Energy, Electronics, and Computing Systems (SEEMS), Greater Noida, India, 2018, pp. 1-10.

[17] T. Toffoli and N. Margolus, Cellular Automata Machines: A New Environment for Modeling (MIT Press, Cambridge, MA, 1987).

[18] TY - JOUR AU - Ahmad, Firdous PY - 2014/01/01 SP - A new F-shaped XOR gate and its implementations as novel adder circuits based (QCA) VL - Volume 16, JO - IOSR Journal of Computer Engineering (IOSR-JCE) ER

[19] Wang, W., Walus, K., & Jullien, G. (2004, January 24). *adders*.

[20] A. (n.d.). *VHDL program coding for 1 bit comparator waveform Xilinx*.

[21] Hayati, M., & Rezaei, A. (2012, April 4). *Design and Optimization of Full Comparator Based on Quantum-Dot Cellular Automata*. Etri Journal.

[22] Beigh, M. R., Mustafa, M., & Ahmad, F. (2013, January 1). *Performance Evaluation of Efficient XOR Structures in (QCA)*. Circuits and Systems.

[23] B. Ghosh, S. Gupta and S. Kumari, "Quantum dot cellular automata magnitude comparators," 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC), Bangkok, Thailand, 2012, pp. 1-2.

[24] Problems in designing with QCAs: Layout = TimingMichael T. Niemier, Peter M. Kogge,04 January200.

[25] Lines of interacting quantum-dot cells: A binary wire Craig S. Lent and P. Douglas Tougaw Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556 (Received 23 February 1993; accepted for publication 2 August 1993)