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QCA-based Single-bit Comparator Circuit

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***Abstract*—Quantum-dot cellular automata (QCA), which consists of a group of cells is a new growing technology and is confirmed to be an advanced alternative of complementary metal oxide semiconductor (CMOS) technology. When the cells of QCA are combined and ordered in a certain way, it can perform various computational tasks. Since, comparators are one of the most vital and widely used circuits and used to compare input voltages, currents, and some other measurable quantities. This paper proposes a novel design for comparator in QCA nanotechnology. The proposed comparator is designed using 39 quantum cells and covers an area of almost 0.07 square micrometers. Further, the proposed design is compared with the previous works. The comparison concludes that the proposed comparator is designed utilizing much lesser number of cells and requires much smaller area than the previous works as also specified in the paper. The proposed comparator has been designed in a single layer.**

Keywords—Quantum-dot cellular automata, comparator, digital design, QCA cell, layout area

I. INTRODUCTION

The world has been using CMOS technology for last few decades for the implementation of different logic circuits and very large scale integration (VLSI) devices. It was in need of a better alternative as CMOS has already been improved and upgraded to its fullest and still is associated with many problems from its large size to huge power consumption and many more [1-3]. Hence, various researchers and scientists came up with an improved alternative which works on nanotechnology. QCA, which is also called Quantum-dot Cellular Automata is a much smaller and advanced alternative method used in the implementation and designing of various logic circuits and VLSI systems & devices [4, 5]. Furthermore, QCA nanotechnology also consumes very less power than CMOS as it does not need the flow of current in circuits for its implementation.

QCA nanotechnology are utilised to design various VLSI devices and different sequential circuits where it is also widely used for the implementation of comparators [6]. Comparator is a widely used circuit for the arithmetic logical unit. It helps to compare the two values. Therefore, in this paper, a novel comparator is proposed which takes much lesser number of cells and area into consideration for its implementation using QCA.

The remaining paper is divided in different sections such as: the fundamental operation and principles of QCA method are provided in section 2 of this paper. Then, the proposed digital comparator using QCA cells is provided in section 3. The simulation and comparison is given in section 4. The comparison of the proposed comparator with the previous comparators is shown in section 4. The conclusion of this research work is discussed in section 5.

II. PRINCIPLES OF QCA

QCA technology works on the principle of polarization. QCA as the name suggests, comprises of quantum cell which is also regarded as the fundamental unit of the nanotechnology. The excitement of the cells is possible with the neighbouring cells [7]. Furthermore, the polarization of a cell is decided by the two electrons present in the four dots of a square-shaped cell [8]. Either the polarization of a cell can be +1, which symbolizes the logic "1" or -1, which symbolizes the logic "0" depending upon how the electrons are placed diagonally in four quantum-dots due to the columbic repulsion force [9]. Fig. 1 shows the fundamentals of the QCA cell.

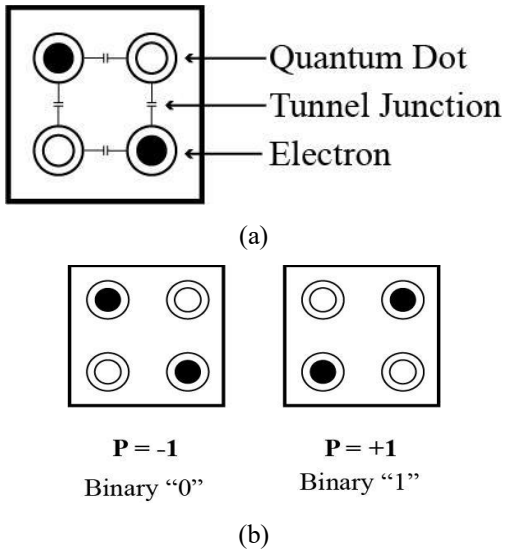
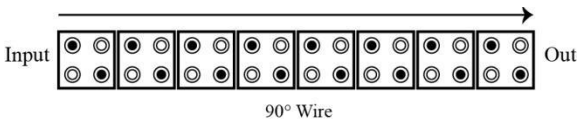


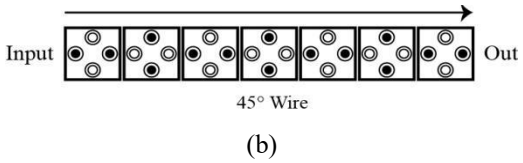
Fig. 1. (a) Basic Quantum Cell (b) -1 and +1 polarized cell

The most basic elements required for the implementation of QCA logic circuits and VLSI devices are wires, inverters and majority gates [10-12].

A wire for the transmission of data in QCA logic is constructed by orderly placing cells together in a row or column [13]. There are two types of wire models namely, 90-degree wire and 45-degree wire. The data in a wire is transmitted due to the property of columbic interaction. Fig. 2 illustrates the wire models in QCA technology using 90-degree and 45-degree cells.



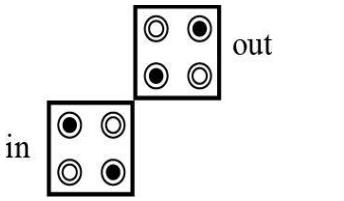
(a)



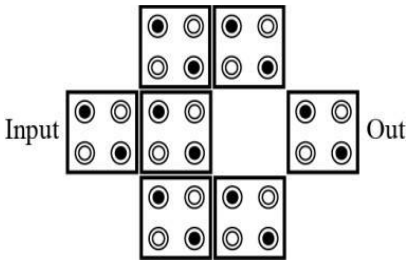
(b)

Fig. 2. Quantum Cell Array (a) 90- and (b) 45-degree wires

An NOT logic gate works on creating the inversion of electrostatic interactions after the electrons in four quantum dots are placed diagonally because of the force of columbic repulsion. An inverter can be constructed by placing quantum cells diagonally upon each other [14]. Scientists utilized the different configurations of QCA cells for the formation of inverter circuits. Fig. 3 demonstrates the two kinds of widely used NOT gates or inverters using QCA cells.



(a)



(b)

Fig. 3. QCA inverter (a) simple design (b) robust design

A majority voter or gate is the universal gate of QCA technology used for the implementation of QCA logic. It is the logic operational gate for the designing of the different circuits in QCA technology. A majority gate as the name itself suggests, reflects true as its output only when the maximum of its inputs is true and vice-versa as each and every input of the gate is given equal priority [15]. Further, the two types of majority gate are - 3-input and the 5-input gates.

The Boolean expression is implemented with the help of some gates in QCA. These gates are the backbone of the field. Majority gate is such type of QCA design for the implementation of the QCA circuits. Majority gate along with inverter built all the blocks in domain. The connections of the cells with accurate clocking make them suitable for logic formation. Various kinds of majority gates are available in QCA theory. These can be classified on the basis of input terminals and their orientations in QCA technology. 3-Input majority voter is given in Fig. 4, which contains three inputs and further reflects true as output of two or more than two of its input are true. Similarly, 5-Input majority voter or gate is presented in Fig. 5, which contains five inputs and further reflects true as its output if and only if three or more than three of the inputs are true.

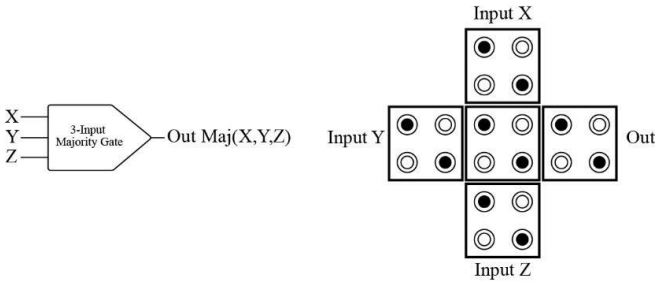


Fig. 4. The QCA-based 3-input majority voter or gate

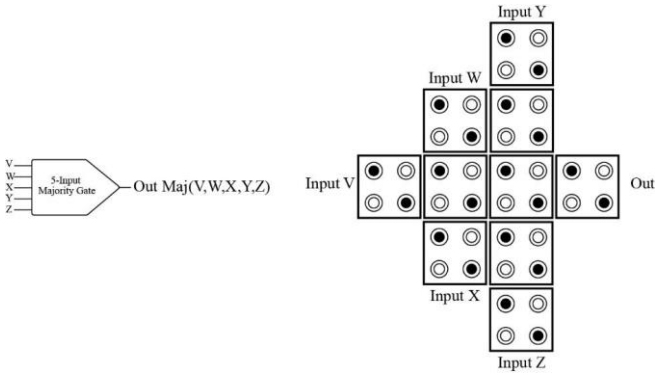


Fig. 5. The QCA-based 5-input majority voter or gate

The flow and direction in QCA nanotechnology is controlled by the four clocks namely Switch, Release, Hold, and Relax [16]. As the electrons easily tunnel between quantum-dots, the switch phase helps in the propagation of data and further helps in the analysis of computation. When the inter-dot barrier is high, the hold phase helps in preventing the tunnelling of electrons through the latching of information in QCA cells. Whenever in Release phase, all the data and value present in the QCA cell gets erased due to the unpolarization of the cells. And lastly in Relax phase, QCA cell goes into an ideal stage and gets charged again to go back to the switch phase [17]. A four phase QCA clock is shown in Fig. 6.

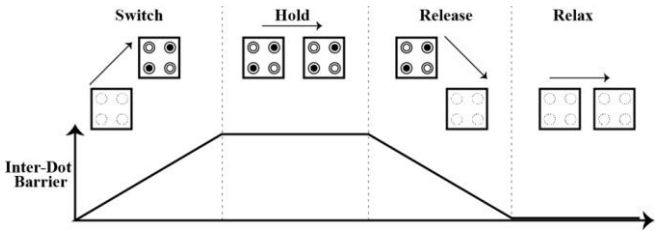


Fig. 6. QCA clocking for logic circuits

Moreover, most of the large-scale circuits implemented and designed using QCA cells is distributed into four clocking zones as shown in Fig. 7. All the cells present in a particular zone, which exhibit same behaviour and compute a specific calculation is controlled by an individual QCA clock signal [18]. Fig. 7 is the complete zone based QCA clocking system, which is used for the implementation of the most of the QCA circuits. A barrier height differentiates the used phases in the QCA circuits. Depending on the nature of barrier height, phases push the operation.

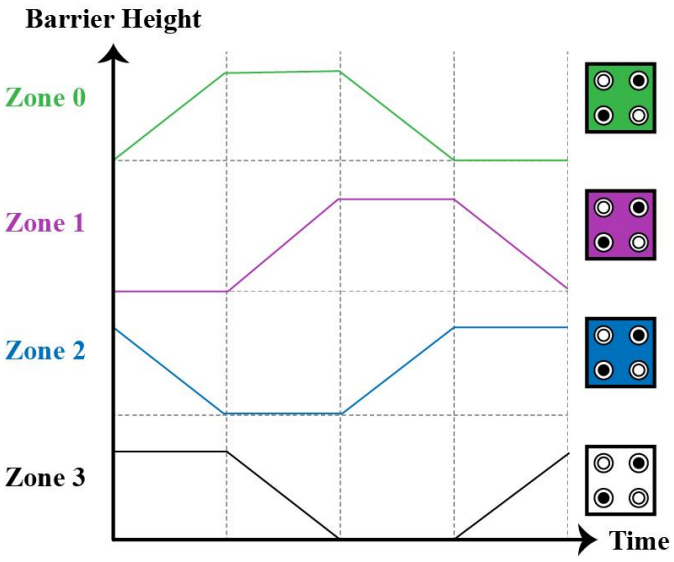


Fig. 7. QCA four phases and four zones of clocking scheme

III. Proposed Work

In this research paper, the proposed single-bit single-layered comparator circuit layout is designed using default simulation setup of QCA Designer tool. The default simulation setup for the digital comparator circuit with the software is given in Table 1.

TABLE 1. DEFAULT SIMULATION PARAMETERS

1.	Cell size	18nm
2.	Number of Samples	12800
3.	Radius of effect	90nm
4.	Relative Permittivity	12.9
5.	Convergence Tolerance	0.001
6.	Clock High	9.8e-22J
7.	Clock Low	3.8e-23J
8.	Clock Amplitude Factor	2
9.	Layer Separation	11.5nm
10.	Maximum Iterations per sample	100

In case of comparator circuit, one output will be at logic '1', while others will be at logic '0'. It depends on the comparison status of the two numbers. One output will be selected at a time, while others will be deactivated. There are three possibilities for the comparison of the numbers. The application of the logic gates for the different outputs is observed. The outputs are converted in the form of the Boolean functions. The comparator expressions are given in equations 1, 2 and 3, which are applicable to design the proposed layout. Suppose, A and B are the two inputs.

$$if\ A\ less\ than\ B\ then\ output\ is\ \bar{A}B \quad (1)$$

$$if\ A\ greater\ than\ B\ then\ output\ is\ A\bar{B} \quad (2)$$

$$if\ A\ equal\ to\ B\ then\ output\ is\ (AB + \bar{A}\bar{B}) \quad (3)$$

The equations 1, 2, and 3 of the comparator are considered and the gate level architecture of the proposed design is given in Fig. 8. The schematic of the comparator circuit consists of the different logic gates. Two NOT gates, two AND gates, and one XOR gate are utilized for the proposed comparator circuit.

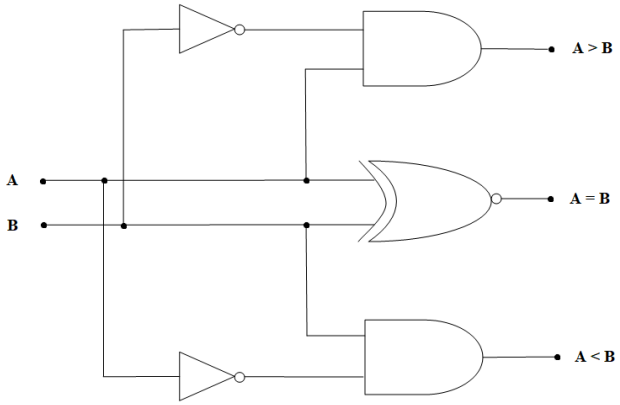


Fig. 8. Single-bit comparator schematic

The operation of the single-bit comparator circuit can also be explained in the form of truth table. So, table 2 provides the logical operation in Fig. 8.

TABLE 2. LOGIC FLOW IN COMPARATOR CIRCUIT

Inputs		*Outputs*		
A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

The QCA circuit is realized by using 3-input majority gates with fixed polarity of -1, which works as the AND gate, QCA inverters by arranging the cells diagonally and a robust XNOR gate design in QCA. The proposed design is given in Fig. 9. Here, A_G_B depicts A > B, A_E_B shows A = B, and A_L_B presents A < B for the developed digital comparator circuit.

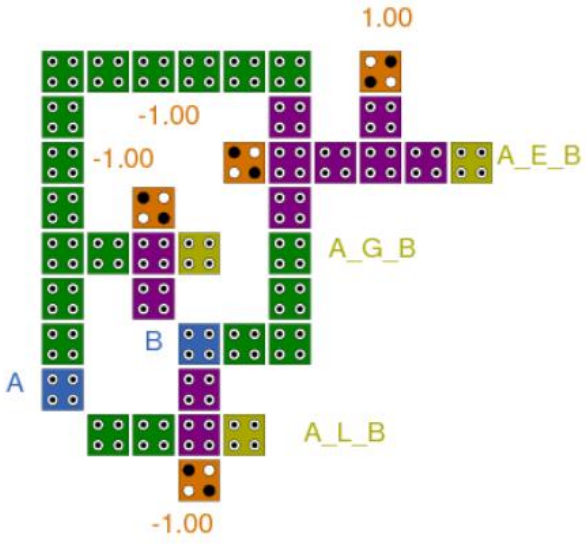


Fig. 9. Proposed design for single-bit comparator

The majority gate theory is applied for the formation of comparator circuit, where fundamental logic circuits are designed using QCA cells. The above-mentioned single-bit comparator circuit has an area of 0.04 square micrometers with only 39 cells. Since, the proposed design uses two clock pulses throughout; therefore it has a latency of 0.5.

IV. Simulation Discussion and Comparison

This section discusses the simulation result and the analysis of the proposed comparator circuit. The results after simulation of the single-bit comparator are shown in Fig. 10. The Fig. clearly shows the correct functioning of the comparator. Two signals A and B are introduced in the circuits via inputs. When A is greater than B, the A_G_B signal goes HIGH and when A is smaller than B, A_L_B goes HIGH and when both of them are equal, A_E_B goes HIGH while the other two goes LOW.

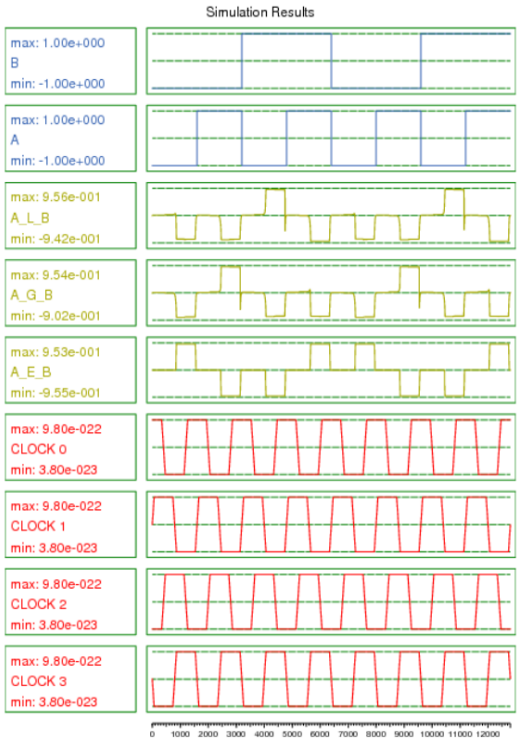


Fig. 10. Simulation results of single-bit comparator

The presented work is also compared with the available similar comparator designs in QCA technology. The comparison is performed for the number of cells, area, clock, and crossover type's parameters. Here, multilayer, co-planar, logical, and single layer are used for the crossover type. Table 3 presents the comparative study of the various comparator circuits in QCA technology.

TABLE 3. COMPARISON OF THE PROPOSED DESIGN WITH THE PREVIOUS WORK

Reference	No. of cells	Area (μm^2)	Clocks	Crossover type
[6]	101	–	4	Co-planar
[19]	81	0.06	3	Multi-layer
[20]	79	0.04	4	Two-layer
[21]	58	0.055	3	None
[22]	42	0.05	3	None
Proposed	39	0.04	2	None

The results presented in table 3 clearly show that the proposed comparator outperforms among the comparators. The proposed comparator uses less number of QCA cells and clocks as compared to other designs. The proposed design is also a single layer design without any crossover and uses as minimum area as required.

The energy dissipation is also calculated for the proposed single-bit comparator circuit. The energy is counted as the bath of the energy, which is the summation of all the coordinating cells. The energy dissipation for the design is 22.3 meV with error of -2.25 meV. The average value of the energy dissipation per event switching is 2.03 meV with the error of -0.20 meV.

V. Conclusion

Quantum-dot Cellular Automata or simply QCA technology is a new growing technology and confirmed to be an advanced alternative of CMOS technology. Therefore, in this paper, a single-bit comparator is designed and simulated using an efficient design methodology under QCA nanotechnology. The paper also shows the benefits of implementing and designing designs in the QCA nanotechnology rather than CMOS technology. Furthermore, the paper bestows vital enhancements in the proposed design in QCA over the previous works including smaller area, lesser number of cells, and design complexity. QCA Designer is used for performing the designs and simulations of the proposed work in QCA technology. In future, many complex arithmetic and logical circuits can be designed using the proposed comparator circuit

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