Birla Institute of Technology & Science – Pilani
Hyderabad Campus
1st Semester 2019-2020
Computer Architecture (CS F342) – Mid Sem Test (Regular)
Date: 01.10.2019 Weightage: 30% Duration: 1hr 30 min. Type: Closed Book

Instructions: Answer all questions. All parts of a question ***should*** be answered consecutively. No of pages: **2**

Q1. (a) Consider the CPU of a computing system where 20% of its total execution time is spent on floating point multiplication operations and 40% of its total execution time is spent on floating point addition operations. Given are two scenarios to improve the performance of this system. Scenario 1: Enhance the floating point multiplication operations by a factor of 10; Scenario 2: Enhance the floating point addition operations by a factor of 1.5. Which of the two scenarios would you prefer?

(b) Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions (A, B, C, D and E) in the instruction set. P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is as follows:

Class	CPI on P1	CPI on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	3	4

Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence. Compute the peak performances of P1 and P2 expressed in instructions per second.

(c) We have a program which can be executed on either of the two machines A and B. If we compile the program for machine A, the program has exactly 100000 instructions. How many instructions would the same program need to have when compiled for machine B, in order for the two machines to have exactly the same execution time for this program? The following table shows the characteristics of the two machines.

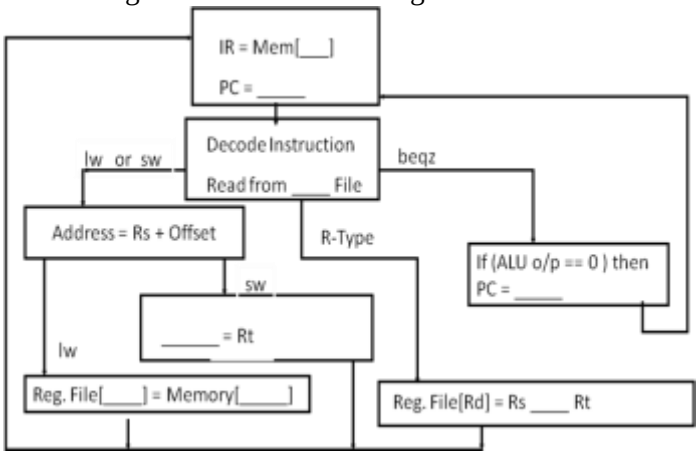
Machine	Overall CPI	Clock rate
A	1.9	1.8 GHz
B	2.6	2.4 GHz

(d) Assume that a program has 4% serial portion. Apply Amdahl's law to find (i) the limit of speedup on 16 processors (ii) the maximum speedup.

(2+2+2+2 = 8 marks)

Q2. (a) (i) Show how you can implement the operation ***swap $rs, $rt*** using only R-type MIPS instructions, without using any additional registers. (ii) If the implementation of this instruction in hardware will increase the clock period of a single-instruction implementation by 8%, what percentage of swap operations in the instruction mix would recommend implementing it in hardware? (s/w-based implementation takes 3cc and h/w-based implementation 1cc. Assume that the base CPI = 1).

(b) The following diagram shows the register-transfer control logic in MIPS ISA. Fill in the blanks.



(c) Consider the shift operations supported in MIPS. Given that: $t2 = 0xabcd1234, fill in the blanks in the following table.

PTO

Instruction	Output
sll $t1, $t2, 8	$t1= _____
srl $t1, $t2, 4	$t1= _____

(2+4+2 = 8 marks)

Q3.(a) Represent the number 286.75_{10} in IEEE 754 single precision format. Show all the steps clearly.
(b) Apply the IEEE 754 multiplication algorithm for 32 bit numbers to find the product of the numbers x1= 125.125_{10} and x2 = 12.065_{10}. You need to show all the steps clearly.
(c) Find the sum of A = 9.75_{10} and B = 0.5625_{10} using the IEEE 32-bit floating point arithmetic. The steps should be clear.
(d) The IEEE 754 standard does **"*Nearest Even*"** rounding by default. Consider the following decimal example on Nearest Even rounding and round to nearest hundredth. Fill in the blanks.

$Value_{10}$	Rounded value	Action performed and reason
7.8949999		
7.8950001		
7.8950000		
7.8850000		

(2+2+2+4 = 10 marks)

Q4.(a) Consider the Booth's algorithm for multiplication of signed numbers. Let the Multiplicand M = 0101 1010 1110 1110 and the Multiplier Q = 0111 0111 1011 1101. Apply the Booth's encoding technique and find the total number of additions/subtractions in this multiplication.
(b) Given Dividend Q = 11, Divisor M = 3, A = 0, number of bits in dividend n = 4, perform restoring division as per the following table. Show all the steps clearly. **(4 + 4 = 8 marks)**

n	M	A	Q	Operation
4	00011	00000	1011	initialize

Q5. (a) The five stages of a processor have latencies as shown in the following table. The state register latency is 20ps.

	Fetch	Decode	Execute	Mem	Write back
(i)	300ps	400ps	350ps	550ps	100ps
(ii)	200ps	150ps	100ps	190ps	140ps

If you are asked to split one of the pipeline stages into two equal halves, which one would you choose? Find out the cycle time, the latency and the throughput after performing the split. Compute these values for both pipelined as well as non-pipelined cases.
(b) (i) A non-pipelined processor with six execution stages has latencies 50ns, 50ns, 60ns, 60ns, 50ns and 50ns. Compute the instruction latency in this machine and the time taken to execute 100 instructions. (ii) If we introduce pipelining with an overhead of 5ns to each execution stage, find the instruction latency in the pipelined machine and the time taken to execute 100 instructions. (iii) Compute the speedup obtained for 100 instructions. **(6 + 6 = 12 marks)**

Q6. (a) Consider the following scenarios regarding data hazards in pipelined processors. There are two instructions I and J, such that J follows I. Identify the correct type of the data hazard (RAW, WAR or WAW) for the following cases.

Slno.	Scenario	Type	Slno.	Scenario	Type	Slno.	Scenario	Type
1	I: R2 <- R1 + R3 J: R4 <- R2 + R3	____	2	I: R2 <- R1 + R3 J: R3 <- R4 + R5	____	3	I: R2 <- R1 + R3 J: R2 <- R4 + R5	____

(b) Consider the following MIPS code segment. (i) Identify the data hazards. (ii) Apply instruction reordering as a solution (iii) Use forwarding as a solution and show the forwarding paths. **(3 + 3 = 6 marks)**

```
add $s0, $t0, $t1
sub $t2, $s0, $t3
add $t3, $s0, $t4
and $t7, $t5, $t4
```

Q7. (a) Which of the following addresses are word-aligned for a MIPS 32-bit ISA and why? **(4 + 4 = 8 marks)**

(i)0x000AE430	(ii)0x00014432	(iii)0x000B0737	(iv)0x0E0D8844

(b) Consider the instruction that loads the word at address 0x00400060 into register $8. Assume that register $10 contains 0x00400000. The instruction is executed as follows: Fill in the blanks.

1. The 32-bit address in $10 is: _____
2. The offset is sign-extended to 32 bits as: _____
3. The memory address computed as the 32-bit sum of the above is: _____
4. Main memory is asked for data from the address: _____
5. After a one machine cycle delay the data reaches $8.