Birla Institute of Technology & Science – Pilani
Hyderabad Campus
1st Semester 2018-2019
Computer Architecture (CS F342) – Mid Sem Test (Regular)

Date: 10.10.2018 Weightage: 30% Duration: 1hr 30 min. Type: Closed Book

Instructions: Answer all questions. All parts of a question ***should*** be answered consecutively. No of pages: **2**

Q1. **(a)** Floating point arithmetic is known to be commutative. Let A = 1.0, B = $1.5*10^{38}$ and C = - $1.5*10^{38}$. Prove that FP arithmetic is not associative using the given values.
(b) Perform addition of the floating point numbers 0x3FC00000 and 0x40500000 in the IEEE 754 single precision format. Give the sum in hexa form. Show all the steps clearly.
(c) What 8-bit pattern would represent the number 3/256, in an 8-bit hypothetical floating-point format, including support for denormalized numbers and nonnumeric values where the first bit is for sign, next four bits for excess-7 exponent and 3 bits for the mantissa?
(d) Consider the 64- bit, IEEE 754 floating point format. $b_{51}..b_0$ is the mantissa, b_{63} is the sign bit s and E' be the biased exponent. Derive an expression to compute the base-10 value of a normalized double precision number in terms of the given info.
(e) Perform the 32-bit division of the IEEE 754 Floating point numbers (X_1 / X_2), where X_1=127.03125 and X_2=16.9375. Show the steps clearly.

(2 x 5 = 10 marks)

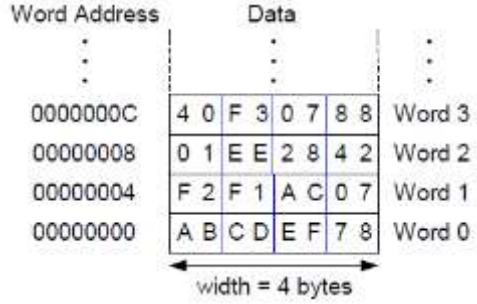
Q2. (a) Translate the for loop control structure given below to its MIPS equivalent in the template given below.

for loop control structure	Equivalent MIPS code
$a0 = 0; **for** ($t0 =10; $t0 > 0; $t0 = $t0 -1) **do** {$a0 = $a0 + $t0}	li $a0, ____ li $t0, ____ loop: add _____ addi _____ bgtz _____

(b) You are quite familiar with MIPS 32-bit ISA. If the instruction set of the MIPS processor is modified, the instruction format must also be changed. For each of the suggested changes, show the size of the bit fields of an R-type format instruction. Also, what is the total number of bits needed for each instruction?

Suggested modification	Size of bit fields and instruction format	Total no. of bits needed for each instruction
8 registers		
10-bit immediate constant		
128 registers		
All arithmetic instructions can use base addressing mode with the last argument (Example: add $a0, $a2, 0[$t1])		

(c) This problem pertains to reading a byte-addressable memory in MIPS. Refer to the following byte-addressable scheme in MIPS and complete the table.



After the instruction lw $s3, 4($0) is executed, value at the destination operand is _____

The instruction to store the value held in $t7 into the 11th 32-bit memory location is _____

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(d) Consider the big-endian and little-endian schemes in MIPS. Assume that $t0 initially contains 0x23456789. After the following code is run, what are the respective outcomes? Answer as per the table given below.

sw $t0, 0($0)
lb $s0, 1($0)

Scheme	Outcome
Big-endian	
Little endian	

(e) Consider the MIPS ***div*** instruction. The instruction format is **000000 | R_s | R_t | 00000 | 00000 | 011010**. Show in psedo code form, the 3 effects of execution of this instruction.

(2 x 5 = 10 marks)

3. (a) The 5 stages of a processor have the following latencies. Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between the pipeline stages.

Fetch	Decode	Execute	Memory	Writeback
300ps	400ps	350ps	500ps	100ps

(i)What is the cycle time for the processor, if the execution is non-pipelined? (ii) If the execution is pipelined, then what is the execution time?

(b) Assume the distribution of instructions that run on a processor is: 50% ALU; 25% BEQ; 15% LW and 10% SW. Assuming there are no stalls or hazards, what is the utilization of the data memory?

(c) We have a 'k' segment pipeline with clock cycle time as 'T_p'. Let there be 'n' tasks to be completed in the pipelined processor. Compute the time taken $ET_{pipeline}$ to execute 'n' instructions in this pipelined processor.

(d) Using the data given in Part (c), compute the speedup (S) of a pipelined processor over a non-pipelined processor, when 'n' tasks are executed on the same processor. Given, the number of tasks 'n' is significantly larger than k, that is, n >> k.

(e) This problem pertains to memory alignment in ISAs. For the given address, please fill in the details in the table.

Memory Address	Alignment (8 bits)	Alignment (16 bits)	Alignment (32 bits)	Alignment (64 bits)
0x00000005				

(2 x 5 = 10 marks)

4. The following table shows the template for implementation of Booth's algorithm for signed multiplication. Complete the implementation. Show all the steps clearly.

Input: 0110, 0010 // Multiplicand M, Multilpier Q, Product in A					
A	Q	Q_{-1}	M		step count sc
0000	0010	0	0110	Initial values	

(10 marks)

5. The following algorithm is meant to perform the non-restoring division of unsigned integers. Complete the algorithm.

Step 1: The registers are initialized with corresponding values (Q = Dividend, M = Divisor, A = 0, n = number of bits in dividend)
Step 2: Check the sign bit of the register _____
Step 3: If it is 1, then shift left the contents of _____ and perform A = A+M, otherwise shift left ____ and perform A = _____
Step 4: Again check the sign bit of register _____
Step 5: If sign bit is 1, Q_0 becomes ____ otherwise Q_0 becomes ____.
Step 6: Decrement the value of ____ by 1
Step 7: If n is not equal to zero, go to step ____ otherwise go to next step
Step 8: If sign bit of A is 1, then perform A = ____
Step 9: Register ____ contains quotient and _____ contains remainder

(12 marks)

6. (a) Let ***lw*** be the slowest instruction in a single-cycle implementation scenario with a latency of 5 (IF) + 3 (ID) + 5 (EX) + 5 (MEM) + 3 (WB) = 21 ns. There are N instructions and the CPI of a single-cycle implementation is 1. What is the running time?

(b) Now, if the ALU is made 25% faster, it takes 5/1.25 = 4 ns to do the ALU computation; the clock-cycle time is reduced to 20 ns. What is the new running time? What is the percentage of improvement?

(4 + 4 = 8 marks)