Computer Architecture (CS F342) Test-3 Date: 13 November 2020 (Friday) Weightage: 15% Mode: Open Book

The question paper contains a total of 9 questions. The duration of the test is 30 minutes. The exam will start at 4:10 PM and end at 4:40 PM.
Each question carries different points and is mentioned beside each question. Each wrong answer will be awarded a negative of 25%. Negative marking is for the MCQ type questions ONLY. Please fill in the student information in the first section and then start answering the questions.

* Required

1. Email address *

Student Information

2. Write your name: *

3. Institute Id: *

4. Declaration: I declare that I have not consulted or shared my answers with anyone. I have maintained academic honesty. I am liable to penalization if found otherwise. Write your name below to agree: *

Questions

5. Consider a branch instruction which is executed 8 times in a program. The actual outcomes of the branch are NT, T, NT, T, NT, NT, NT, T, where T= taken, and NT= not taken. If n-bit dynamic local branch prediction is used, calculate the prediction accuracy when i) n=1 ii) n=2. Assume that predictions always initialized to NT state. 4 points

Mark only one oval.

- 3/8, 5/8
- 1/8, 7/8
- 1/4, 3/4
- 5/8, 3/8

6. A non-pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is 2 points

Mark only one oval.

- 4.5
- 4.0
- 3.33
- 3.0

7. Consider a pipelined processor with 4-stages viz., IF, ID, Ex, WB. The IF, ID, and WB take 1 cycle to complete, whereas the number of cycles for Ex stage depends on the instruction. ADD and SUB take 1 cycle in Ex stage, whereas MUL takes 3 cycles in Ex stage. What is the number of clock cycles that will be required to complete the set of instructions mentioned below when i) Operand forwarding is used, ii) when operand forwarding is not used? 4 points

```
ADD R2, R1, R0      //R2<-R0+R1
MUL R4, R3, R2      //R4<-R3+R2
SUB R2, R5, R4      //R2<-R5-R4
```

Mark only one oval.

- ◯ 8, 10
- ◯ 8, 12
- ◯ 8, 8
- ◯ 6, 8

8. For the following set of instructions, mention all the RAW, WAR and WAW hazards. 2 points

```
ADD R2, R1, R0      //R2<-R0+R1
MUL R4, R3, R2      //R4<-R3+R2
SUB R2, R5, R4      //R2<-R5-R4
```

9. Consider a (2, 2) correlating branch predictor. If the physical memory size is 4GB, what is the number of bits in global predictor? Assume that BTB is as large as the physical memory. 2 points

Mark only one oval.

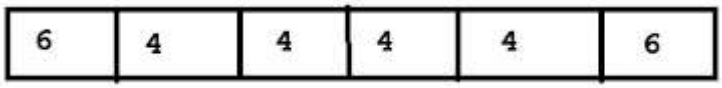
- ◯ 4GB
- ◯ 8GB
- ◯ 8MB
- ◯ 5MB

10. Consider a (2, 2) correlating branch predictor. The physical memory size is 4GB, and that the BTB uses direct mapping with a block size of 16 words and word size of 4 bytes. If there are 128 blocks in the BTB, what is the number of bits in the global predictor. 4 points

Mark only one oval.

- ◯ 16K
- ◯ 64K
- ◯ 128K
- ◯ 1K

11. Assume a hypothetical pipelined architecture which has 28 bits of instruction format as shown below (The fields are same as any MIPS instruction). Assume that the physical memory address is of 20 bits and the size of the registers are 32 bits. Then the size of the IF/ID register in a pipelined datapath will be 2 points



Mark only one oval.

- ◯ 128
- ◯ 104
- ◯ 72
- ◯ 76

12. Assume the following set of instructions and that the architecture supports 1 delay slot. Assume that the program requires 100 cycles to execute with no miss-predictions. The program has 20% branch instructions and branch is successful 60% of the time. Now we used a static branch prediction where we always consider branch not taken, and the branch delay slot is filled with the fall through instruction viz., I3. However, if branch is successful, I3 has to be rolled back which incurs an additional penalty of 4 cycles. What is overall increase in number of cycles required? 4 points

```
L0:I1
   beq r1, r2, L1
   I3
   I4
   I5
   j L0
L1: //code
//code
```

Mark only one oval.

- 48%
- 22%
- 60%
- 32%

For the following question, provide a step-wise solution in the space given below the question. There is no negative marking for this question.

13. A 5-stage pipelined RISC processor running at 2.4 GHz is used to execute a program. The instructions statistics for this program are as follows: Branch =20%, Load =20%, Store =10%, Arithmetic instruction = 50%. Assume that there are no data-dependencies in the program. Also assume that the instructions fetch operations hit in the cache whereas 2% of all data accesses incur a cache miss. The penalty to access the main memory for a cache miss is 10 cycles. The processor uses a dynamic branch predictor and a branch target buffer to predict all the branches. The Customer demands the processor manufacturer that at least 2 billion instructions per second. What must be the minimum branch prediction accuracy for the branch predictor to satisfy this demand? 6 points