Birla Institute of Technology and Science – Pilani, Hyderabad/Goa Campus
Second Semester 2018-19
CS F342: Computer Architecture Comprehensive Exam (PART A, Closed Book-Solutions)
Time: 2:00PM – 4:00PM **Date:** 13th May 2019 **Max. Marks:** 80M

ID No:	**Name:**

Note: Answer all the questions in the space provided.

1. Fill in the blanks (Answer in the boxes provided) **[2+2+2+2=8M]**

(i) When CPU performs a write and it results in a cache hit, both the content in the cache and the corresponding copy in the memory are updated if the _____cache write policy is applied.

(i) Write Through

(ii) If, the cache miss rate can be reduced by increasing the width of a cache block. This reduction is due to the _____ property of cache.

(ii) Spatial Locality

(iii) _____ should be considered for designing the cooling requirement of a processor.

(iii)Sustained Power Consumption (Thermal Design Power)

(iv) A desktop computer without screen or keyboard usually accessed via a network can be categorized as _____

(iv) Low end Server, Simple Server

2. Change the sequence of instructions given below to find the gcd of two numbers which are stored in memory locations pointed by $t0 and $t0+4. (**Note: No partial marking**) **[8M]**

```
1.          lw $s0, 0($t0)
2.          lw $s1, 4($t0)
3.          slt $t3, $s0, $s1
4.          sub $s1, $s1, $s0
5.  L2:     sub $s0, $s0, $s1
6.          beq $t3, $zero, L2
7.          j L1
8.          j L1
9.  L1:     beq $s0, $s1, EXIT
10. EXIT:   sw $s0, 8($t0)
11.         jr $ra   ;Exits the Main program
```

Answer: Correct Sequence of Instructions

Sl No	Instructions
1	lw $s0, 0($t0)
2	lw $s1, 4($t0)
3	L1: beq $s0, $s1, EXIT
4	slt $t3, $s0, $s1
5	beq $t3, $zero, L2
6	sub $s1, $s1, $s0
7	j L1
8	L2: sub $s0, $s0, $s1
9	j L1
10	EXIT: sw $s0, 8($t0)
11	jr $ra

3. Match the pseudo-instructions with the corresponding MIPS instruction sequence ($at is a temporary register used for converting pseudo instructions): **[2+2+2+2=8M]**

1) bge $s0, $s1, LABEL	A) slt $at, $s1, $s0 bne $at, $zero, LABEL
2) bgt $s0, $s1, LABEL	B) slt $at, $s1, $s0 beq $at, $zero, LABEL
3) ble $s0, $s1, LABEL	C) slt $at, $s0, $s1 bne $at, $zero, LABEL
4) blt $s0, $s1, LABEL	D) slt $at, $s0, $s1 beq $at, $zero, LABEL

Answer:

1) →	D)
2) →	A)
3) →	B)
4) →	C)

4. Assume you have a 32-bit, byte-addressed machine with virtual addressing. However, any memory address whose two high-order bits are 11 is treated as unmapped. These addresses are only accessible in privileged mode—i.e. by the operating system—and bypass virtual address translation. Answer all the questions below. Your answer can be expressed as multiple of a power of 2, or in terms of KB, MB, GB, or TB as appropriate. (**Note: No partial marking**) **[2+2+2+2=8M]**

(i) What is the maximum amount of physical memory this system can address?

(ii) What is the maximum amount of virtual memory any single user process/program on this system can address?

(iii) How many virtual pages are available to each user process/program, assuming page size as 4KB?

(iv) Assuming each page table entry is 4 bytes, how much memory would a page table require?

Answers:

(i) $2^{32} = 4GB$

(ii) (Exclude privileged mode cases) $2^{32}-2^{30}=3x2^{30}=3GB$

(iii) $(2^{30}x3)/(2^{12}) = 3x2^{18}$ Pages

(iv) $3 \times 2^{18} \times 4 = 3MB$

5. A processor has the following specifications:
Word size is 16-bits; No. of blocks in cache is 8; Cache block size is 1 word; Cache uses LRU replacement policy and Write back scheme; Main memory is word addressable (not byte addressable as in MIPS); (Assume 'V' → Valid bit, 'D' → Dirty bit)

For the given sequence of operations, complete the tables of the L1 cache contents, assuming a
i) 2-way set associative cache and ii) 4-way set associative cache, after all operations have been complete.
Write the full memory address in each cache entry rather than just the tag bits so you can easily write it in hexadecimal. The LRU column should contain a natural number (1, 2…..) where lowest number represents the most recently used item, and highest number represents the least recently used. Assume that all cache lines are invalid when the sequence of operations starts.

Sequence:
Read 0x4949 from address 0xF222
Read 0xAAAA from address 0x6767
Read 0x2345 from address 0xCABB
Read 0x1188 from address 0xFACE
Read 0x4444 from address 0x1234
Read 0x5555 from address 0xDAC1
Read 0xACED from address 0xACED
Read 0x9999 from address 0x5876
Write 0x8201 to address 0x8640
Read 0x4444 from address 0x1234
Read 0x1776 from address 0xBEDD
Write 0x2017 to address 0x4582

(Note: No Partial Marking. All the entries have to be correct to get the full marks) [8M+8M]

2- Way set Associative Cache

Set	Address	Data	V	D	LRU
0	1234	4444	1	0	1
0	8640	8201	1	1	2
1	BEDD	1776	1	0	1
1	ACED	ACED	1	0	2
2	5876	9999	1	0	2
2	4582	2017	1	1	1
3	6767	AAAA	1	0	2
3	CABB	2345	1	0	1

4- Way set Associative Cache

Set	Address	Data	V	D	LRU
0	8640	8201	1	1	3
0	4852	2017	1	1	1
0	1234	4444	1	0	2
0	5876	9999	1	0	4
1	BEDD	1776	1	0	1
1	CABB	2345	1	0	4
1	DAC1	5555	1	0	3
1	ACED	ACED	1	0	2

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6. An image of resolution 100 X 100 should be transformed using a 5-stage pipelined MIPS processor operating at 20MHz. Assume that this processor does not support branch and multiplication instructions. The transformation involves increasing brightness (adding each 8-bit pixel by 3) and then increasing contrast (multiplying each 8-bit pixel by 4).
   i) Provide instruction sequence (using not more than 8 instructions) to transform two pixels (as per specifications above). Assume the pixels of the image are stored as array in memory, initial address of this array is stored in $t1. The transformed pixels should be stored back in the same locations as original pixels.
   ii) Calculate no of clock cycles and the execution time required for transforming all the pixels of given 100 x 100 resolution image, assuming forwarding is allowed to input of EX stage only and compiler does not have the capability to reorder instructions to reduce stalls. Also assume that instruction memory and data memory access is completed in 1 clock cycle.

(i) **[4M]**

No	Instruction Sequence
1	lb $t0, 0($t1)
2	addi $t0, $t0, 3
3	sll $t0, $t0, 2
4	sb $t0, 0($t1)
5	lb $t0, 1($t1)
6	addi $t0, $t0, 3
7	sll $t0, $t0, 2
8	sb $t0, 1($t1)

(ii) **[4M]**

(Show your main calculations below)
There are 4 instructions required for transformation of one pixel. But a stall is also required because load is followed by data dependent instruction. Hence total number of clock cycles for transforming one pixel = (4 instructions +1 (stall) – 1 +5) = 9

For two pixels = 2x4 instructions + 2 stall -1 + 5 = 14

No. of clock cycles required for transforming 100 x 100 resolution image = 10000x4 instructions + 10000 stalls -1 + 5 = 50004 clock cycles

Execution time for transforming 100 x 100 resolution image = 50004 x (1/20MHz) = 2.5 ms

7. The IEEE Standard for Floating-Point Arithmetic (IEEE 754) is a technical standard for floating-point arithmetic established in 1985 by the Institute of Electrical and Electronics Engineers (IEEE). Answer all the questions below related to floating point operations. **[2+2+4=8M]**

(i) Determine the decimal number (accurate up to three digits after decimal point) represented by the 32-bit IEEE-754 floating point number 0x44FC63AE?

(ii) Convert decimal number 11.52 into IEEE-754 single precision floating point format and represent it in hexadecimal.

(iii) Two 32-bit numbers A and B are given as inputs to a floating point (IEEE 754) adder (without rounding stage). The 32-bit output of this floating point adder is C. Assuming that the hexadecimal notation of A is 0x41080000 and B is 0x425E0000; Find the hexadecimal notation of C.

(i) 2019.115

(ii) 413851EC

(iii) 0x42800000

8. The Instruction Set Architecture (ISA) serves as the boundary between software and hardware. There are three most common types of ISA namely: Stack based ISA, Accumulator Based ISA and General Purpose Register (GPR) based ISA (GPR based ISA can further be classified as Register-Memory and Register-Register ISA). Answer the following questions on ISA. **(Note: No Partial marking) [3+3+2=8M]**

(i) Given the following code for a stack based ISA, where 'add' represents addition operation and 'mul' represents multiplication operation, determine the expression implemented by the code.

push A
push B
add
push C
mul
pop D

(ii) Write the code to implement the expression found in 8 (i) for Accumulator based ISA.

(iii) List one major disadvantage of stack based ISA.

(i) Expression:
D = C* (A+B)

(ii) Code for Accumulator based ISA:
load A
add B
mul C
store D

(iii) Disadvantage of Stack based ISA:
Stack resides in Memory and becomes a bottleneck since memory is accessed more frequently

9. Answer the following in in short sentences (up to 15 words). **[2+2+2+2=8M]**

(i) The amount of time required to read a block of data from a disk into main memory is composed of seek time, rotational latency, and transfer time. Seek time refers to the time taken to/for_____

for the read-write head to move into position over the appropriate track

(ii) List one advantage of arbitration scheme used in PCI bus, with respect to bus priority and fairness.

PCI-Bus uses Centralized Parallel arbitration, which assures fairness. Least priority device never gets locked out.

(iii) List two ways to improve *Mean Time To Failure (MTTF)* of a storage device.

1. Fault Avoidance
2. Fault Tolerance
3. Fault Forecasting (ANY TWO)

(iv) List two characteristics of a Processor-Memory Bus.

1. Short
2. High Speed
3. Optimized for Cache block transfers (ANY TWO)

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Additional Space:

Additional Space: