Birla Institute of Technology & Science – Pilani

Hyderabad Campus

1st Semester 2019-2020

Computer Architecture (CS F342) – Comprehensive Examination (Regular)

Date: 07.12.2019 Weightage: 40% Duration: 3 hrs. Type: Closed Book

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Instructions: Answer all questions; All parts of a question ***should*** be answered consecutively; No of pages in the question paper: **3;** show the steps clearly wherever applicable.

Q1. (a) Amdahl's law helps us quantify the performance improvement in a computing system. Let $Perf_{\_max}$ be the maximum possible performance improvement. (i) Compute the $Perf_{\_max}$ for a given system, if the part that can be improved is 25% of the overall system and its performance can be doubled. (ii) Compute the $Perf_{\_max}$ for another system where the part that can be improved is 75% of the overall system and its performance can be doubled. (iii) From the above two scenarios, prove quantitatively the statement "the more the part that cannot be improved, the less the benefit of improvement".

(b) Consider a 400MHz CPU used to execute a benchmark program. The instruction type, the instruction count and the clock cycle count are as shown in the table below. Compute the average CPI, the processor performance (MIPS rate) and the execution time for this program when executed in this CPU.

Instruction Type	Instruction Count	Clock cycle count
int arithmetic	45000	1
Data transfer	32000	2
FP	15000	2
Control transfer	8000	2

(c) Assume that we are designing an ISA for 16 registers, using a fixed-length 16-bit encoding. (i) What is the maximum number of ALU operations that we can encode if each instruction encodes a destination and two source registers (as in "`add R0, R1, R2`") to indicate that the sum of R1 and R2 should be placed into R0? (ii) What is the maximum number of ALU operations that we can encode if each instruction encodes a destination register (also used as a source operand) and an additional source register (as in "`add R0, R1`") to indicate that the sum of R0 and R1 should be placed into R0?

(d) Assume that we are using an 8-stage pipelined CPU. If this machine has a 2 GHz clock, how many nanoseconds does it take to complete each instruction once it enters the pipeline?

(3 + 3 + 2 + 3 = 11 marks)

Q2. (a) Consider a machine for which the cache contains 65,536 (64K) bytes of data in 64-byte blocks with two-way set-associative placement (LRU and write back). The address coming into the cache is divided into two fields: 34-bit block address and 6-bit block offset. (i) What is the width of the tag field? (ii) What is the size of the address for the CPU to reach a word in the cache?

(b) The following table shows some of the implementation details of a direct-mapped cache using muxes and comparators. Number of blocks in the cache is n. Fill in the blanks in the table.

Block j of main memory can map to line number (___ mod ____) only of the cache
Number of multiplexers required = Number of bits in the _____ field
Size of each multiplexer = Number of lines in cache x _____
Number of comparators required = _____
Size of comparator = Number of bits in the ____ field
Hit latency = ____ latency + ____ latency

(c) Translation Lookaside Buffer (TLB) is a special cache used to keep track of the recently used transactions. Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. Compute the effective memory access time, given the TLB hit rate is 0.6; the time to search TLB is 10ms and the physical memory access time is 80ms.

PTO

(d) Consider the following code segment for multiplying two matrices. We go with the following three assumptions: (i) the binary for executing this function fits in one page, and the stack also fits in one page (in a separate page) (ii) the two entries are already in TLB when the function begins to execute (iii) an integer requires 4 bytes for storage. Compute the number of TLB misses if the page size is 4096 and the TLB has 8 entries and uses LRU replacement policy.

```
int a[1024][1024], b[1024][1024],
c[1024][1024];
multiply() {
  unsigned i, j, k;
```

```
for(i = 0; i < 1024; i++)
  for(j = 0; j < 1024; j++)
    for(k = 0; k < 1024; k++)
      c[i][j] += a[i,k] * b[k,j];}
```

(2 + 4 + 2 + 4 = 12 marks)

Q3. (a) Consider the Booth's algorithm for 2's complement multiplication. Let the multiplier be -57 (represented in 8 bits). The following table depicts the steps for bit pair recoding of the multiplier. Fill in the blanks.

Step1: Take 2's complement of the given multiplier as: _____
Step 2: Append 0 to LSB: _____
Step 3: The Booth's coding logic is: _____
Step 4: Apply the Booth's coding logic as (add 1 bit at a time, from LSB to MSB): _____
Step 5: The multiplier -57 will be recoded as: _____

(b) Given two normalized decimal numbers A = 1.25×10^{-306} and B = 1.23×10^{-306}. Using these two numbers, prove that "the result of an operation on two normalized numbers will not itself be representable always as a normalized number". Answer as per the template provided below.

From the given values, it is obvious that A ≠ B; but in finite precision normalized floating point arithmetic, A – B = ____ as A – B = 0.02 x ___; i.e, A – B = ____in the normalized form, which is too_____ to be represented as a normalized number. It is therefore rounded to the value of ____.

(c) The following table shows the initialization steps involved in dividing unsigned binary integers in 6 bits using non-restoring division. Given Dividend = 46_{10}, and Divisor = 23_{10}. Fill in the blanks.

Set Register A = _____; Set Register Q = Dividend = _____; AQ = _____ , Q_0 = _____; Set M = Divisor = _____, M' = 2's complement of M = _____; Set Count = _____, since _____ bit operation is being done here.

(d) The scenario given below states the three rules for multiplication using Booth's algorithm. Fill in the blanks using 'added to', 'subtracted from' or 'left unchanged if' appropriately.

The multiplicand is _____ the partial product upon encountering the first least significant 1 in a string of 1's in the multiplier; The multiplicand is _____ the partial product upon encountering the first 0 (provided that there was a previous '1') in a string of 0's in the multiplier; The partial product is _____ the multiplier bit is identical to the previous multiplier bit.

(2.5 + 2.5 + 4 + 3 = 12 marks)

Q4.(a) Correlating branch predictors help the processor address control hazards. Consider the following implementation scenario of correlating branch prediction. Assume that the variable x is in the register R1.

```
if (x= = 0)
x = 1;
if (x= = 1)
```

```
    BNEZ R1, L1          Branch b1
    ADDI R1,R0, #1
L1: SUBI R3, R1, #1
    BNEZ R3, L2          Branch b2
L2:
```

Fill in the following table:

Initial value of x	x = = 0? (Y/N)	b1(Taken/Not Taken)	Value of x before b2	x = = 1? (Y/N)	b2(Taken/Not Taken)
0	Y				
1					
2					

PTO

(b) There are three 5-stage MIPS machines, each with different branch resolution strategies. Machine M1 has a branch predictor which always predicts the correct target and hence ideal. Machine M2 resolves branches in the EX stage (2 penalty cycles) using a predict-not-taken scheme. Machine M3 resolves branches in the ID stage using one branch delay slot. Assume the following:- all the three have the same frequency; 20% of the instructions are branches; 25% of branches are taken and the stalls are due to branches alone; the compiler is able to fill 30% of the delay slots with useful instructions. Find the CPIs of M1, M2 and M3.

(7 + 3 = 10 marks)

Q5. (a) Given that we have six 1TB disks to assemble a RAID system considering RAID levels 0, 5 and 6. Compute the effective data storage capacity for each of the levels. Also, find as to how many disks can fail before the data is lost permanently in each of the above cases. Answer according to the given template.

RAID level	Data storage capacity	No.of disks which we can afford to fail
0		
5		
6		

(b) This problem pertains to the performance of system components. Assume that a server machine crashes on an average once a month and then it takes 12 hours to reboot it. Compute the server availability.
(c) Consider a disk system environment comprising 1000 disks with MTTF = 100,000 hrs and MTTR = 100 hrs.(i) Find the availability in this case. (ii) if Annualized Failure Rate (AFR) is the average rate of failures per year (%), find AFR.
(d) Consider three operations associated with the RAID architecture. Map each of them to the correct RAID levels.

Operation	(i)stripe data across all disks	(ii) logical write amounts to two physical writes	(iii) logical write means minimum 2 to maximum N physical reads and writes.
RAID level			

(3 + 2 + 2 + 3 = 10 marks)

Q6. (a) Consider the cache coherence problem. An example scenario of a write update or broadcast protocol working on a snooping bus for a single cache block (X) with write-back caches for a 2-processor setup is given below. We assume that neither cache initially holds X and that the value of X in memory is 10. Fill in the blanks in the template below.

CPU activity	Bus activity	Contents of A's cache	Contents of B' cache	Contents of X
				10
CPU A reads X				
CPU B reads X				
CPU A writes 20 to X				
CPU B reads X				

(b) Given a cache size of n blocks; let k represent the number of sets if mapped as set associative; find the search times for each of the three cache mapping schemes (direct-mapped, fully associative and set associative).

(8 + 3 = 11 marks)

Q7(a) Represent the number -176.375_{10} in IEEE 32 bit format. Subsequently represent the number in its hexa equivalent. Show all the steps clearly.
(b) Using the numbers $a = -2.7 \times 10^{23}$, $b = 2.7 \times 10^{23}$, and $c = 1.0$, prove that floating point addition is not associative.
(c) Add the floating point numbers 9.76×10^{25} and 2.59×10^{24} assuming 3 digit mantissa (i) with no extra digits for the internal registers and no round digits (ii) the internal registers have two extra digits and rounding is possible. Show the sequence of steps in both cases clearly.
(d) The following scenario shows the sequence of steps involved in exception handling in MIPS. Fill in the blanks.

MIPS instructions that cause overflow (or some other violation) lead to an _____, which sets the _____code. It then switches to the _____ mode (designated by a bit in the _____ register of coprocessor no: _____, register no: _____) and transfers control to a predefined address _____to invoke a routine (_____) for handling the exception.

(2 + 2 + 6 + 4 = 14 marks)