Birla Institute of Technology and Science – Pilani, Hyderabad/Goa Campus
Second Semester 2017-18
CS F342: Computer Architecture Mid-Term Test (Closed Book)

Time: 11:00AM – 12:30PM **Date:** 9th March 2018 **Max. Marks:** 60

Note: Answer all the questions in the same sequence.

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1. Assume that we make an enhancement to floating point unit of a computer that improves the execution time of floating point instructions by a factor of 10. For a given program, **after** enhancing the floating point unit, the floating point instructions take 60% of the enhanced execution time and the other instructions take the remaining 40% of enhanced execution time.

(a) What is the speedup obtained by improving the floating-point unit?

(b) What percentage of the original execution time (Execution time before enhancing) is taken by floating point instructions before enhancing? **[8]**

2. Translate following C statements in to MIPS assembly code using least number of assembly instructions and least number of temporary registers.

(a) B[4] = A[i+j];

(b) f = g + A[B[h]];

(Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that A and B are word arrays and the base address of the arrays A and B are in registers $s6 and $s7, respectively.) **[12]**

3. We begin with a computer implemented in single-cycle implementation. When the stages are split by functionality, the stages do not require the same amount of time. The original machine had a clock cycle time of 14ns. After the stages were split, the measured times were IF, 4ns; ID, 2ns; EX, 2ns; MEM, 4ns; and WB, 2ns. The pipeline register delay is 0.5ns.

(a) What is the clock cycle time of a 5-stage pipelined machine?

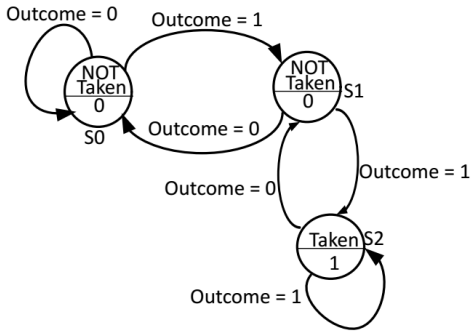
(b) If there were no stalls in a 5-stage pipelined machine, which executes large number of instructions, the CPI is said to be approximately equal to 1. If there is a stall (by one clock cycle) every 4 instructions in this machine what would be the new CPI?

(c) Assuming that there are large number of instructions to be executed and a stall every 4 instructions, what is the speedup of a 5-stage pipelined machine over the single cycle machine? **[10]**

4. Consider the MIPS Assembly code below. Assume that there are two words stored in memory: 21 (15h) is stored at location pointed by $t0 and 8 (8h) is stored at location pointed by $t0 + 4.

```
Main:   lw $s0, 0($t0)
        lw $s1, 4($t0)
B1:     beq $s0, $s1, EXIT
        slt $t3, $s0, $s1 ; set on less than, if ($s0 < $s1) $t3 = 1 else $t3 = 0
B2:     beq $t3, $zero, L2
        sub $s1, $s1, $s0
        j B1
L2:     sub $s0, $s0, $s1
        j B1
EXIT:   sw $s0, 8($t0)
        jr $ra              ;Exits the Main program
```

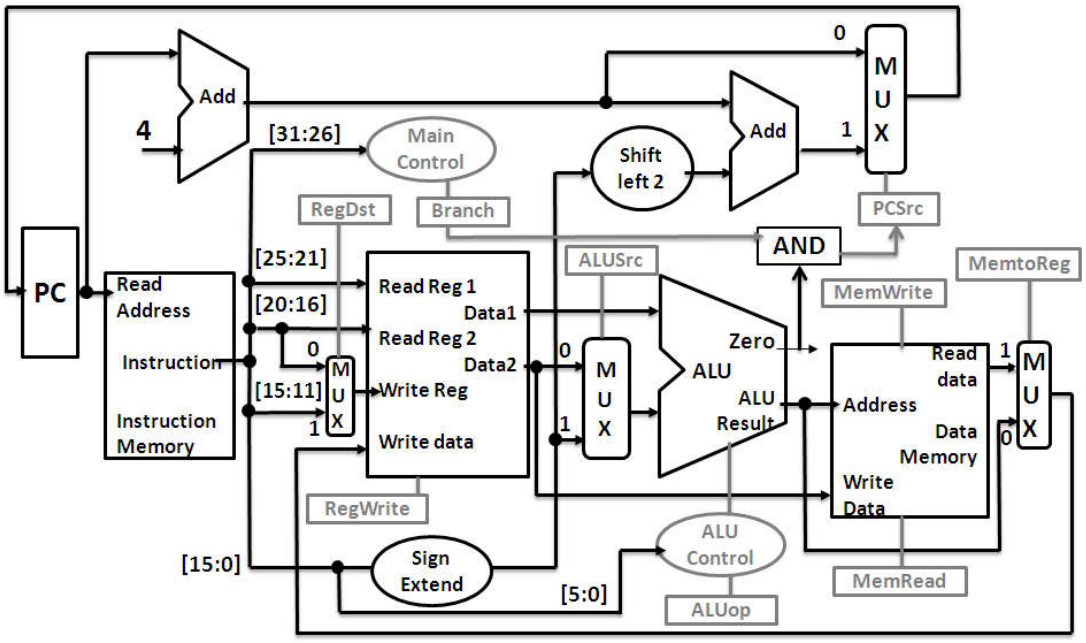
Assume that branch at B1 uses a dynamic 1-bit predictor initialized to **Taken** state, whereas branch at B2 uses a dynamic 2-bit predictor whose FSM is shown below. This predictor is initialized to S2 state.



Determine the predictions and the outcomes for branches at B1 and B2. Also determine the accuracy of prediction for both the branches. The predictions and outcomes for both branches should be in the tabular format as shown below (for branch at B1): (Use **T** for Taken and **N** for Not taken.). **[14]**

Occurrence for Branch at B1	1st	2nd	So on
Prediction for Branch at B1			
Outcome for Branch at B1			

5. Data path and control for a Load, Store, R-type and Branch (beq) instructions of MIPS is shown in the figure below.



(i) The MIPS instruction **lui** loads a 16-bit immediate value in to the upper 16 bits of a 32-bit register. The lower 16 bits of the register are set to zero. The MIPS datapath shown in the figure above does not support this instruction. The instruction format for **lui** instruction is shown below:

Bits	31:26	25:21	20:16	15:0
Field	Opcode (001111)	Rs (not used) (00000)	Rt (Destination Register)	16-bit Immediate Value

For example the instruction format for instruction lui $t0, 0x1234 is as below. After execution of this instruction $t0 will have 0x12340000.

001111	00000	01000	0001 0010 0011 0100

(a) Draw the datapath (digital blocks, additional control signals) that is required to support the **lui** instruction in simplest manner possible. (Draw only the extra datapath and show the additional control signals. Briefly explain the function of blocks used).

(b) Specify the value of all control signals (including the newly added ones if any) when executing **lui** instruction. (Note: you do not have to provide a value for ALUop control signal; instead mention the operation that the ALU should perform for **lui** instruction). **[5 + 5]**

(ii) For the data path shown in figure (without datapath for lui), we would like to know whether partial information of the datapath and control signals can help to deduce the instruction(s) currently under execution. Give all possible instruction(s) for which the following information is true.

(a) "RegDst" signal is "X" (b) "ALUSrc" signal is "1" (c) "MemtoReg" signal is "X" **[6]**
