Computer Architecture

Tutorial - 2

Amdhal’s Law

- In computer architecture ,Amdahl’s law (or Amdahl’s Argument) is a formula which gives the theoretical speedup in latency of the execution of a task at fixed workload that can be expected of a system whose resources are improved .It is named after the computer scientist Gene Amdahl.

The speedup formula is given by ,

$$\text{speedup} = \frac{\text{Execution time without enhancement}}{\text{Execution Time with enhancement}} = \frac{\text{Execution Time}_{old}}{\text{Execution Time}_{new}}$$

$$\text{Execution Time}_{new} = \text{Execution Time}_{old} \times \left((1 - \text{Fraction}_{enhanced}) + (\text{Fraction}_{Enhanced} / \text{Speedup}_{Enhanced})\right)$$

$$\text{overall speedup} = 1 / \left((1 - \text{Fraction}_{enhanced}) + (\text{Fraction}_{Enhanced} / \text{Speedup}_{Enhanced})\right)$$

Examples for Amdahl's law

a) Given , $Speedup_{enhanced} = 20$

$Fraction_{enhanced} = 0.5$

overall speedup =?

overall speedup = 1/((1-0.5) + 0.5/20) = 1.105

b) Given , $Speedup_{enhanced} = 16$

$Fraction_{enhanced} = 0.6$

overall speedup = ?

overall speedup = 1/((1-0.6) + 0.6/16) = 2.286.

Tutorial -2
Performance Metrics

Q1. A program is executed for 1 sec ,on a processor with a clock cycle of 25 nsec and $Throughput_1$ = 20 MIPS.

a) How many cycles are used by an instruction , for the program?

b) Let us assume that ,given some optimization techniques ,the throughput of the program is optimized. In the new case, the 20% of the program instructions is executed with CPI=1,while the fraction of remaining instructions (80%) is executed with the same CPI.How much is the Speed Up from the case (1) to the case (2) ? How much is the $Throughput_2$ expressed in MIPS?

Solution -1

a) CASE 1 :Given , Execution time of program = 1 sec

clock cycle time =25 nsec => clock rate = 1/25 nsec = 0.04 Ghz = 40 Mhz

Throughput_1 = 20 MIPS

CPI = ?

we know Throughput in MIPS = (Clock rate)/CPI x 10^6

=> CPI = clock rate /throughput x 10^6

= 40 x 10^6 / 20 x 10^6 = 2 .

=> CPI of the given program is 2 cycles.

b) CASE 2 :Given , For 20% of program CPI =1.

80% of program CPI =2

case1 , Throughput_1 =20 MIPS

Speedup from case 1 to case 2 =?

Throughput_2 of case2 =?

Solution -1

improvement in CPI of fraction of instructions (fraction of Enhancement) =20/100=0.2

Enhanced CPI = 1 for 20% instructions

Speedup enhanced in CPI for 20% instructions = old cpi /newcpi = 2/1=2.

Overall speedup from case1 to case 2 is given by Amdahl's law

Speedup = 1/((1- fraction enhanced) + fraction enhanced/speedup)

⇒ Speedup = 1/((1- 0.2) +0.2/2) = 1.11

⇒ $Throughput_2$ = speedup x $Throughput_1$ = 1.11 x 20 = 22.2

Tutorial -2
Performance Metrics

Q2. A program is executed for 1 sec ,on a processor with a clock cycle of 100 nsec and $CPI_1 = 1.5$.

a) How much is the $Throughput_1$ expressed in MIPS ?

b) Let us assume that ,given some optimization techniques ,30% of the program instructions is executed with CPI =1 ,while the fraction of remaining instrcutions (70%) is executed with the same CPI.HOW much is the Throughput expressed in MIPS ? How much is the speedup from case(1) to the case(2) ?

Solution -2

a) Given , Execution time of program =1 sec

clock cycle time = 100 nsec => clock rate = 10 MHz

$CPI_1 = 1.5.$

$Throughput_1 = ?$

we know Throughput in MIPS = (Clock rate)/CPI x 10^6

=> $Throughput_1 = (10 \times 10^6) / 1.5 \times 10^6 = 10/1.5 = 6.67$

b) Fraction of instructions for which CPI is enhanced (Fraction Enhanced)= 30/100 = 0.3 .

Enhanced cpi =1

Speedup in CPI = CPI_{old} / CPI_{new} = 1.5 /1 =1.5

overall speedup from case1 to case2

using (Amdahl's law) =1/((1-0.3)+ 0.3/1.5)= 1.11

Solution 2

b) contd…

overall speedup in terms of speedup is given by speedup = $Throughput_2$ / $Throughput_1$

=> $Throughput_2$ = speedup x $Throughput_1$ = 1.11 x 6.67 = 7.4

Tutorial -2
Performance Metrics

Q3.

a) A program is executed for 1 sec ,on a processor with a clock cycle of 25 nsec and $\text{Throughput}_1 = 30$ MIPS.How much is the CPI_1 for this program?

b) Let us consider a computer executing the following mix of instructions:

Instructions	Frequency	Clock cycles
ALU	75	1
LOAD	10	8
STORE	10	4
BRANCH	5	3

Tutorial -2
Performance Metrics

Q3. b) contd

i)how much is the CPI average (1) assuming a clock period of 3 nsec ?

How much is the Throughput expressed in MIPS ,in the case(1)?

ii) How much is the speedup assuming that,introducing an optimized data cache ,load instructions require 2 clock cycles ?

iii) How much is the Speedup assuming that, introducing an optimized branch unit,branch instructions require 1 clock cycles?

iv) How much is the speedup assuming to introduce 4 ALUs working in parallel ?

v) How much is the speedup assuming to introduce all together the above optimizations?

Solution-3

a) Given , execution time of program =1 sec.

$\text{Throughput}_1 = 30$ MIPS

CCT = 25nsec => clock rate= 40 MHz

$CPI_1 = ?$

=> cpi = clock rate / (MIPS x 10^6)

=> $CPI_1 = 40 \times 10^6 /(30 \times 10^{6)} = 1.33.$

Solution-3

Instructions	Frequency	Clock cycles
ALU	75	1
LOAD	10	8
STORE	10	4
BRANCH	5	3

b) Given , clock period = 3 nsec

=> clock rate = 333 MHz.

i.) Average cpi = 75/100 * 1 + 10/100 * 8 + 10/100 * 4+ 5/100 * 3 = 2.1 .

ii) MIPS = Clock rate / (cpi x 10^6)

= (333 * 10^6)/ (2.1* 10^6)

= 158.57

Solution-3

b)

ii.) How much is the speedup assuming that,introducing an optimized data cache ,load instructions require 2 clock cycles ?

sol . $CPI_2 = CPI_{2\ average} = 0.75*1 + 0.1 * 2 + 0.1 * 4 + 0.05 * 2 = 1.45$

speedup = $CPI_1 / CPI_2 = 2.1/1.45 = 1.448$

iii.) How much is the SpeedUP assuming that,introducing an optimized branch unit,branch instructions require 1 clock cycles?

Sol. $CPI_3 = CPI_{3\ average} = 0.75*1 + 0.1 * 8 + 0.1 * 4 + 0.05 * 1 = 2$

speedup = $CPI_1 / CPI_3 = 2.1/2 = 1.05.$

Solution-3

b)

iv.) How much is the speedup assuming to introduce 2 ALUs working in parallel ?

sol. $CPI_4 = CPI_{4\ average} = 0.1875 * 1 + 0.1 * 8 + 0.1 * 4 + 0.05 * 3 = 1.54$

$speedup = CPI_1 / CPI_4 = 2.1/1.54 = 1.36.$

v) How much is the speedup assuming to introduce all together the above optimizations?

sol. $CPI_5 = CPI_{5\ average} = 0.1875 * 1 + 0.1 * 2 + 0.1 * 4 + 0.05 * 1 = 0.8375$

$speedup = CPI_1 / CPI_4 = 2.1/0.8375 = 2.51$

Tutorial -2
Performance Metrics

Q4. You have a system that contains a special processor for doing floating-point operations. You have determined that 50% of your computations can use the floating-point processor . The speedup of the floating point processor is 15.

a) compute the overall speedup achieved by using the floating-point processor.

b) Compute the overall speedup achieved if you modify the compiler so that 75% of the computations can use the floating-point processor.

Solution-4

a) Given ,

$\text{Fraction}_{\text{enhanced}} = 0.5$, $\text{speedup}_{\text{enhanced}} = 15$.

overall speedup = ?

overall speedup = 1/((1-0.5) + 0.5/15) = 1/(0.5 + 0.033) = 1.876.

b) Given ,

$\text{Fraction}_{\text{enhanced}} = 0.75$, $\text{speedup}_{\text{enhanced}} = 15$.

overall speedup = ?

overall speedup = 1/((1-0.75) + 0.75/15) = 1/(0.25 + 0.05) = 3.33.