Computer Architecture (CS F342) Test-2 Date: 09 October 2020 (Friday) Weightage: 15% Mode: Open Book

The question paper contains a total of 14 questions. The duration of the test is 30 minutes. The exam will start at 4:10 PM and end at 4:40 PM.
Each question carries different points and is mentioned beside each question. Each wrong answer will be awarded a negative of 25%. Please fill in the student information in the first section and then start answering the questions.

* Required

1. Email address *

Student Information

2. Write your name: *

3. Institute Id: *

4. Declaration: I declare that I have not consulted or shared my answers with anyone. I have maintained academic honesty. I am liable to penalization if found otherwise. Write your name below to agree: *

Questions

5. Q1. Assume that the number 12.125 is represented using the conventional IEEE-754 standard. Which of the following operations below converts the number +12.125 to +2.25 x 2^(-108). 4 points

Mark only one oval.

- left shift by 1 position
- left shift by 3 position
- right shift by 2 position
- Arithmetic shift right by 2 position

6. Q2. In a multi-cycled architecture, the sequence of micro-instructions (RTL) that are triggered when the following instructions get executed are : add $1,$2,$3. (i) Reg1 <- $2, Reg2 <- $3 (ii) PC <- PC +4 (iii) IR <- MEM[PC] (iv) $3 <- Reg1 + Reg2 1 point

Mark only one oval.

- (i)->(ii)->(iii)->(iv)
- (ii)->(iii)->(i)->(iv)
- (i)->(iii)->(ii)->(iv)
- (iii)->(ii)->(i)->(iv)

7. Q3. The number and type of multiplexers that will be required to select registers (from a register file) for a system with a register file of 16 registers and that supports only single operand instructions are (e.g. Accumulator based systems) 1 point

Mark only one oval.

- 1, 4X1
- 0, 16X1
- 2, 16X1
- 1, 16X1

8. Q4. Assuming that memory read operations take 5ns, ALU operation takes 3ns, shift operation takes 1ns, sign-extend operation takes 1ns, register read operation takes 2ns, and register write takes 2ns, then the total time to execute a 'lw' operation in MIPS is 2 points

Mark only one oval.

- 11sec
- 13sec
- 14sec
- 9sec

9. Q5. What will be the size of a MIPS instruction, if the number of (programmer visible) registers in MIPS is changed to 40. 1 point

Mark only one oval.

- 30
- 32
- 35
- 36

10. Q6. If the number of (programmer visible) registers in MIPS is changed to 40, what is the range of displacement for a conditional branch instruction, if the size of instruction remains unchanged? 1 point

Mark only one oval.

- +-8kbytes
- +-32kbytes
- +-64kbytes
- +-16kbytes

11. Q7. What will be the error if you perform the standard default rounding for the number 0.17 represented using 1 bit of sign, 3 bits of exponent, and 5 bits of mantissa? 4 points

Mark only one oval.

- 1.375X10^(-2)
- 1.875X10^(-3)
- 9.6875X10^(-3)
- 1.25X10^(-3)

12. Q8. How many normalized floating point numbers can be represented using 1 bit for sign, 3 bits for exponent and 5 bits for mantissa. 1 point

Mark only one oval.

- 384
- 448
- 512
- 508

13. Q9. The number of different operations possible when two signed numbers are added or subtracted are 1 point

Mark only one oval.

- 4
- 8
- 10
- 16

14. Q10. If α (\alpha) is the % of a program code which can be executed simultaneously by n processors in a computer system. The remaining code can be executed sequentially by a single processor. Each processor has an execution rate of x MIPS and all the processors are of equal capacity. The effective MIPS rate when the code is executed using n processors is 2 points

Mark only one oval.

- x/[(1-α)+α /n]
- x/[(1-α)+n]
- x/(1-n)
- x/(1-α)

15. Q11. Add the following floating point numbers A and B in IEEE-754 single precision format. A=00000110001000000000000000000001; B=10000110001000000000000000000001. Then the value of S = A + B is 2 points

Mark only one oval.

- 0
- positive overflow
- positive underflow
- NaN

16. Q12. Assume two registers $t2 and $t3 contain 0x80000000 and 0xD0000000, respectively. Consider the following two MIPS instructions to be executed independently. add $t1, $t2, $t3 , sub $t1, $t2, $t3. What will be the output ? 2 points

Mark only one oval.

- overflow, no overflow
- no overflow, no overflow
- no overflow, overflow
- overflow, overflow

17. Q13. Mr. Singh is entrusted to write a code that can provide a speedup of 1.6 by his manager. He achieves 95% optimization with CPI=1, while the rest is executed with previous (original) CPI =1.5, and returns home dreaming of a big appraisal. If the code is executed for 1 sec, on the processors with a clock cycle of 100 nsec and CPI = 1.5, what will be the new throughput after speedup? 4 points

Mark only one oval.

- 9.76 MIPS
- 6.76 MIPS
- 7.25 MIPS
- 8.0 MIPS

18. Q14. Assume that a certain floating point representation has 1 sign bit, 4 bits for the exponent and 7 bits for the significand . What is value where positive underflow occurs and what is the maximum error that can occur while representing a floating point number? 4 points

Mark only one oval.

- 2^(-6)-2^(-13) and 1
- 2^(-7)-2^(-14) and 0.0000001
- 2^(-7)-2^(-13) and 0.00001
- 2^(-7) and 0.0000001