EE309

PROJECT - 1

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Components Used

1) LS1
2) LS7
3) SE6
4) SE9
5) RF
6) PC
7) T1
8) T2
9) Flag
10) ALU
11) MUX-16
12) MUX-3

Hardware Flowcharts

S0

PC → I MemA, Alu_a
+1 → Alu_b
Alu_c → T1
I MemD → IR

S1

T1 → PC, RF_D3
"111" → RF_A3

S2

IR_{11-9} → RF_A1
IR_{8-6} → RF_A2
RF_D1 → Alu_a
RF_D2 → Alu_b

S3

IR_{5-3} → RF_A3
Alu_c → RF_D3

S4

IR_{11-9} → RF_A1
IR_{8-6} → RF_A2
RF_D1 → Alu_a
RF_D2 → LS1 → Alu_b

S5

IR_{11-9} → RF_A1
RF_D1 → Alu_a
IR_{5-0} → SE6 → Alu_b

S6

IR_{8-6} → RF_A3
Alu_c → RF_D3

L0

$IR_{11-9} \rightarrow RF\_A3$
$IR_{8-0} \rightarrow LS7 \rightarrow RF\_D3$

L1

$IR_{8-6} \rightarrow RF\_A2$
$RF\_D1 \rightarrow Alu\_a$
$IR_{5-0} \rightarrow SE6 \rightarrow Alu\_b$

L2

$Alu\_c \rightarrow \not{\emptyset} MemA$
$\not{\emptyset} MemD \rightarrow RF\_D3$
$IR_{11-9} \rightarrow RF\_A3$

L3

$Alu\_c \rightarrow \not{\emptyset} MemA$
$IR_{11-9} \rightarrow RF\_A1$
$RF\_D1 \rightarrow \not{\emptyset} MemW$

B1

$PC \rightarrow Alu\_a$
$IR_{5-0} \rightarrow SE6 \rightarrow Alu\_b$
$Alu\_c \rightarrow T1$

B2

$T1 \rightarrow RF\_D3$
$IR_{11-9} \rightarrow RF\_A3$

B3

$PC \rightarrow Alu\_a$
$IR_{8-0} \rightarrow SE9 \rightarrow Alub$
$Alu\_c \rightarrow T1$

B4

$IR_{8-6} \rightarrow RF\_A2$
$RF\_D2 \rightarrow T1$

$IR_{11-9} \rightarrow RF\_A1$
$RF\_D1 \rightarrow Alu\_a$
$IR_{8-0} \rightarrow SE9 \rightarrow Alu\_b$

B5

$Alu\_c \rightarrow T1$

B6

$IR_{11-9} \rightarrow RF\_A1$
$RF\_D1 \rightarrow T1$

M0

$T1 \rightarrow \cancel{D}MemA, Alu\_a$
$\cancel{D}MemD \rightarrow T2$
$+1 \rightarrow Alu\_b$
$Alu\_c \rightarrow T1$

M1

$T1 \rightarrow \cancel{D}MemA, Alu\_a$
$T2 \rightarrow \cancel{D}MemW$
$+1 \rightarrow Alu\_b$
$Alu\_c \rightarrow T1$

M2

Instructions	State Sequence
ADD	s0 → s1 → s2 → s3
ADC	s0 → s1 if C is set s2 → s else ib
ADZ	s0 → s1 if Z is set s2 → s3 else ib
ADL	s0 → s1 → s4 → s3
ADI	s0 → s1 → s5 → s6
NDU	s0 → s1 → s2 → s3
NDC	s0 → s1 if C is set s2 → s3 else ib
NDZ	s0 → s1 if Z is set s2 → s3 else ib
LHI	s0 → s1 → L0
LW	s0 → s1 → L1 → L2
SW	s0 → s1 → L1 → L3
LM	s0 → s1 | depends on the lower
SM	s0 → s1 | byte of IR.
BEQ	s0 → s1 → s2 if Z is set B1 else ib
JAL	s0 → s1 → B2 → B3 → s1
JLR	s0 → s1 → B2 → B4 → s1
JRI	s0 → s1 → B5 → B6 → s1