Register Set:

General Purpose Registers:

reg 8	reg 16	reg 32
al, ah	ax, bx	eax, ebx
bl, bh	cx, dx	ecx, edx
cl, ch	si, di	esi, edi
dl, dh	sp, bp	esp, ebp

Flag register

16 bit — flags

32 bit — eflags.

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floating point:

R0 – R7

st(7) st(0) — 80 bit

MMX Reg:

mm0 – mm7, 8, 64 bit

SSE Registers.

xmm0, xmm7, 8, 128 bit reg.

Debug Register: Debugger

dr0 – dr7, 8 : Debug

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Model Specific reg: MXCSR

Ring-0 registers:

- Segment Registers:

  cs ds ss es fs gs

  code data stack extra — 16 bit

- Control Registers

  cr0 - cr4 (5, 32 bit control reg.)

  cr0[0] — 0 — Real
  cr0[0] — 1 — Protected

- Table Registers:

  GDTR = Global Descriptor Table Register
  LDTR = Local Descriptor Table Reg
  IDTR = Interrupt Descriptor table reg
  TR = Task Register

App	Kernel
7	3

$100 $-100 $0776 $0xa0b0c0d0
$'A' $var_name

%reg_name

%al %ah %bl %bh %cl %ch
%dl %dh

%ax %bx %cx %dx %si %di %sp %bp

%eax %ebx %ecx %edx %esi %edi %esp %ebp

%st(0) %st(7)

%mm0 %mm7

%xmm0 %xmm7