A CMOS Line Driver with 80-dB Linearity for ISDN Applications

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Abstract—**A high-performance CMOS line driver for ISDN *U*-interface transceiver applications has been designed and fabricated. Careful study of requirements and trade-offs affecting linearity, power efficiency, and quiescent current presented in this paper has resulted in a circuit structure featuring a highly linear input/output characteristic and well-controlled quiescent current. The prototype line driver is capable of delivering a $5V_{pp}$ signal of up to 80 kHz to a 60-Ω load while exhibiting linearity in the order of 77 ± 5 dB and operating from a single 5-V power supply. Linearity better than 70 dB is maintained for load resistances as low as 20 Ω.**

I. Introduction

THE system performance of full-duplex echo canceler based data transceivers is limited by the nonlinear distortion introduced by the analog front end [1]. Canceling the distortion generated by the analog circuitry, in particular the buffer amplifier, requires the addition of a complex nonlinear echo canceler. A line driver with linearity sufficient to eliminate or simplify the nonlinear echo canceler could result in significant savings in terms of power and silicon area and therefore is a decisive factor for the cost-effective monolithic implementation of a full-range ISDN *U*-transceiver.

The problems associated with the design of this type of line driver include maintaining linearity for relatively high bandwidth, which requires preserving substantial loop gain up to high frequencies while insuring stability under widely varying load conditions. Other important design issues are well-controlled quiescent output current and high-power efficiency. Finally, low output impedance is required to drive the relatively low load impedance and also to suppress the coupling of impulse noise from the line to the transceiver [2]. These constraints combined with the present-day MOS technology shortcomings of low transconductance, poor device matching, and relatively low ratio of power supply voltage to threshold voltage pose a challenging design problem.

This paper describes a CMOS line driver capable of delivering a $5V_{pp}$ signal of up to 80 kHz to a load of less than 60 Ω while maintaining linearity in the order of 77 ± 5 dB and operating from a single 5-V power supply.

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II. Requirements and Considerations

The line driver described in this paper is intended for a *U*-interface transceiver complying with the specifications defined by American National Standards Institute (ANSI) [3]. The line code is a four-level memoryless code (2B1Q) with a power spectral density peak at about 40 kHz. Fig. 1 shows two transceivers communicating over a twisted-pair line. The line driver buffers the transmitter from the line and is coupled to the line through line interface circuitry consisting of a step-up transformer and termination resistors. The total value of the termination resistors is equal to the reflected line impedance:

$$RT = \frac{R_U}{n^2} \tag{1}$$

where RT corresponds to the total termination resistance, R_U is the line impedance and is equal to 135 Ω, and n is the transformer turns ratio. Thus, to provide the $2.5V_p$ pulses on the line, as called for by the standard, the line driver has to output double the peak line pulse amplitude:

$$V_{\mathrm{OUT}_{pp}} = 10\ \mathrm{V}/n \tag{2}$$

where $V_{\mathrm{OUT}_{pp}}$ corresponds to the line driver peak-to-peak output voltage swing. Note that the transformer coupling provides the flexibility towards tailoring the required maximum output voltage to the line-driver capabilities through the choice of the transformer turns ratio.

The choice of the transformer turns ratio directly affects the line-driver power efficiency. Fig. 2 shows the average power drawn from the supply due to the load as a function of the output voltage swing. As expected, power efficiency improves as the output voltage swing is increased (the transformer turns ratio is decreased).

The load impedance exercised by the line driver is also a function of the transformer turns ratio. The effective nominal load is given by

$$R_{\mathrm{Load}|\mathrm{nom}} = \frac{2R_U}{n^2}. \tag{3}$$

The effective nominal load is also illustrated in Fig. 2. The nominal load accounts for only one component of the current flowing in the line driver, namely, the near-end signal. The far-end transmitter can induce currents in the line driver with maximum levels in the order of the peak near-end current. In addition, the power spectral density

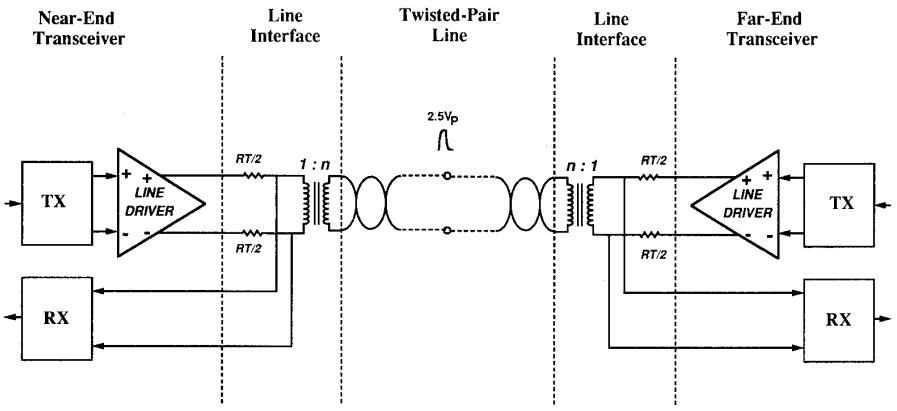

Fig. 1. The line driver in the overall *U*-transceiver system.

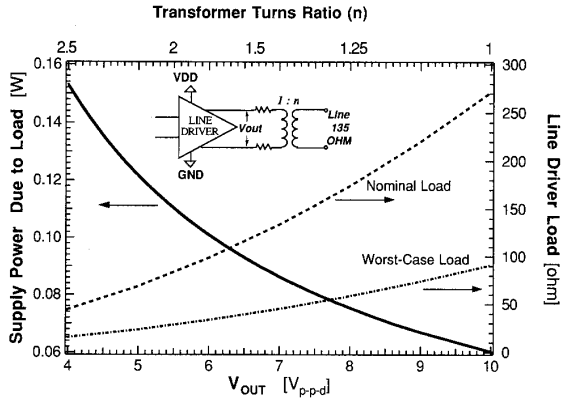

Fig. 2. Average power drawn from the supply due to the load (nominal and worst-case load exercised by the line driver).

of the 2B1Q line code is nonzero at dc, where the magnetizing inductance of the transformer appears as a short circuit. The resulting dc *wander* adds a third component to the line-driver current. The sum of these three components could vary widely; at one extreme the three components could sum up to zero and thus the effective load approaches infinity. The other extreme corresponds to the case where all the three components are of the same polarity, and at their peak values the resulting worst-case load could be as low as

$$R_{\text{Load}}|_{\text{worst-case}} \approx \frac{R_{\text{Load}}|_{\text{nom}}}{3}. \tag{4}$$

Substituting for $R_{\text{Load}}|_{\text{nom}}$ from (3)

$$R_{\text{Load}}|_{\text{worst-case}} \approx \frac{2R_U}{3n^2} \tag{5}$$

as shown in Fig. 2. Note that the line driver stability has to be insured throughout the entire range of load variations of

$$\frac{2R_U}{3n^2} \le R_{\text{Load}} \le \infty. \tag{6}$$

III. Circuit Configuration and Operation

The block diagram of the buffer amplifier is shown in Fig. 3. The line driver has a fully differential topology and is composed of two class-A/B output stages preceded by a preamplifier and connected in a feedback loop. Each output stage is constructed of large complementary common-source devices driven by error amplifiers EP and EN.

In this circuit topology, the main source of nonlinearity is identified as the distortion incurred by the output devices which exercise the largest voltage swings in the circuit. To first order, the closed-loop nonlinearity is determined by the output device distortion attenuated by the open-loop gain:

$$HD_{\text{Closed-Loop}} \approx \frac{HD_{\text{Output Devices}}}{A_{\text{Open-Loop}}} \tag{7}$$

where *HD* corresponds to the harmonic distortion. Thus, to effectively suppress the distortion caused by the output devices, high open-loop gain is desired. The open-loop gain is the product of the preamplifier gain, error amplifier gain, transconductance of the output devices, and the load impedance:

$$A_{\text{Open-Loop}} = A_{\text{Preamp}} \times A_{EP,EN} \times gm_{\text{Output Devices}} \times R_{\text{Load}}. \tag{8}$$

The level of the required open-loop gain is dependent on the extent of nonlinearities generated by the output devices plus the additional nonlinearities produced by the preamplifier and the error amplifiers. One way to suppress the nonlinearities caused by the output devices is to employ a class-A/B topology for the preamplifier [4]. Class-A/B amplifiers typically can be designed for higher dc gain than class-A amplifiers, however, their input/output characteristic tends to be extremely nonlinear. Also, to date such amplifiers have had lower bandwidth compared to the bandwidth achievable with class-A type amplifiers. Here, we have chosen to use a folded-cascode [5] class-A structure for the preamplifier with a moderate dc gain of 500–1000. This structure has the advantage of a highly

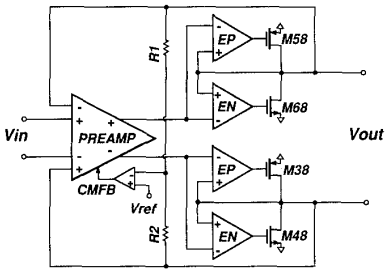

Fig. 3. Line-driver block diagram.

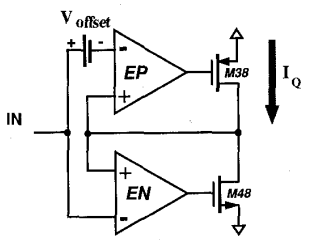

Fig. 4. Effect of the input-referred offset voltage of the error amplifier on the output device quiescent current.

linear input/output characteristic, and can be designed to have higher bandwidth for superior high-frequency linearity.

One important aspect of line-driver design is that the quiescent current in the output transistors must be well-controlled to prevent crossover distortion at one extreme of its variations and excessive power dissipation at the other extreme. The primary source of quiescent current variation is the input-referred offset voltage of the error amplifiers. In Fig. 4 the input-referred offset voltage of EP, the error amplifier driving the p-channel output device, is considered and is modeled as a small voltage source, V_{offset}, at the input of the amplifier. An estimate of the maximum quiescent current variation ΔI_Q is found to be

$$\frac{\Delta I_Q}{I_Q} \approx \frac{2V_{\text{offset}}A_{\text{EP}}}{(V_{GS} - V_T)_{M38}} \tag{9}$$

where A_{EP} corresponds to the dc gain of the error amplifier EP driving the p-channel output device. Assuming a maximum offset voltage of $V_{\text{offset}}|_{\max} \approx 3$ mV for the error amplifier and a gate overdrive voltage of about $(V_{GS} - V_T)_{M38} = 150$ mV for the output device, allowing 30% fluctuation for the quiescent current, and substituting in (9), it is found that the open-loop gain of the error amplifiers must be constrained to less than about 8 [6].

Given that the combined dc gain of the preamplifier and error amplifiers in this case amounts to 65 to 75 dB, the effect of the $gm_{\text{Output Device}} \times R_{\text{load}}$ is considered next. Assuming the output devices operate in the saturation region:

$$gm_{\text{Output Devices}} \propto \sqrt{I}. \tag{10}$$

Substituting $I \propto n$ and $R_{\text{Load}} \propto 1/n^2$ from (3) yields

$$gm_{\text{Output Devices}} \times R_{\text{Load}} \propto \frac{1}{n\sqrt{n}}. \tag{11}$$

Thus, for a given output device size, the dc gain associated with the combination of the output device transconductance and the effective load increases as the transformer turns ratio is decreased (output voltage swing increased). Further insight into the trade-offs associated with the choice of the output device sizes and transformer turns ratio is obtained from Fig. 5, where two different load lines are drawn on the I_{ds}–V_{ds} characteristics of the output devices. The case where the top n-channel output device, M_{68}, is sinking the current sourced by M_{38}, the bottom p-channel output device is considered. Load line (*a*) corresponds to the worst-case load assuming a transformer turns ratio of $n = 2$. The output device sizes are chosen so that both devices operate in the saturation mode throughout the entire voltage swing for $n = 2$. Load line (*b*) corresponds to the lower transformer turns ratio of $n = 1.25$. Note that for the same output device sizes as case (*a*), both devices enter triode mode at the extremes of the voltage swing. As the output devices enter triode mode, transconductance decreases rapidly resulting in substantially lower open-loop gain and, hence, higher distortion. It can be shown that with the limited preamplifier gain and the gain restriction set on the error amplifiers, the output devices should operate in the saturation region, where the transconductance is higher, to achieve better than 70-dB overall linearity. Based on the above discussion, an estimate of the minimum required W/L for the p-channel output device as a function of the transformer turns ratio, so that the output devices operate in the saturation region under the most severe loading conditions, is computed to be

$$\frac{W}{L} \geq \frac{6\hat{V}_U}{R_U \dfrac{\mu C_{ox}}{2}} \times \frac{n}{\left(\dfrac{V_{DD}}{2} - \dfrac{\hat{V}_U}{n}\right)^2} \tag{12}$$

where $\hat{V}_U$ is the peak line voltage of 2.5 V and R_U is the line impedance, which equals 135 Ω. The minimum required W/L for the p-channel output device is computed from (12) and illustrated in Fig. 6 assuming a minimum power supply voltage of 4.75 V and $\mu_p C_{ox} = 40\ \mu\text{A/V}^2$. Well-behaved quiescent conditions dictate a minimum overdrive voltage of at least a few hundred millivolts for the output devices. Fig. 6 also illustrates the quiescent power dissipated by the output devices with an assumed overdrive voltage of 150 mV. The third curve in Fig. 6 corresponds to the average power drawn from the supply due to the load. From Fig. 6 it is concluded that for output voltage swings larger than $6.6V_{pp}$ ($n \leq 1.5$), high linearity dictates extremely large output device sizes. This in turn results in excessive quiescent power dissipation, loss of bandwidth due to the large capacitance associated with the output devices, and large silicon area. At the other extreme, output voltage swings smaller than $4V_{pp}$ ($n \geq$

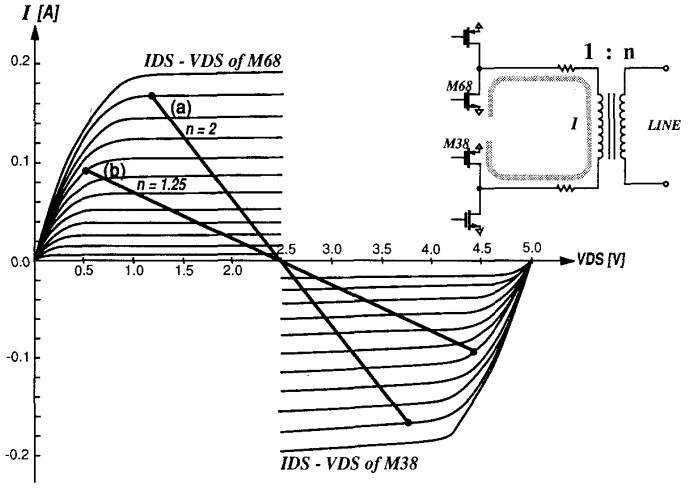

Fig. 5. Load lines in the I_{ds}–V_{ds} plane for the output devices M_{38} and M_{68}.

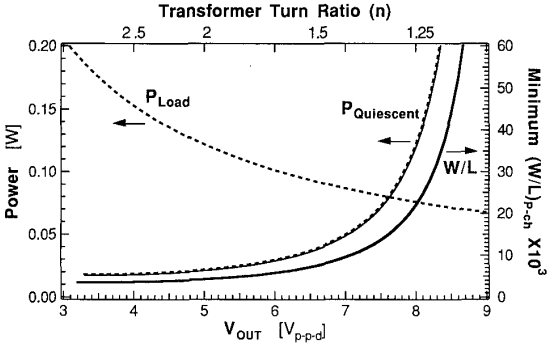

Fig. 6. Minimum required W/L, quiescent power consumed by the output devices, and average power drawn from the supply due to the load.

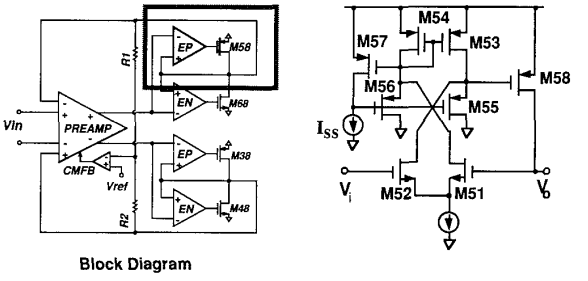

Fig. 7. Circuit schematic of the error amplifier driving the p-channel output device.

2.5) result in poor power efficiency. Thus, with this circuit topology and considering the linearity versus power dissipation trade-offs, a transformer turns ratio in the range of

$$1.5 < n < 2.5 \tag{13}$$

or an output voltage swing of

$$4\ \text{V} < V_{\text{OUT}_{pp}} < 6.6\ \text{V} \tag{14}$$

is within reason.

Fig. 7 shows the schematic for one error amplifier (EP) and the corresponding output transistor. Considering the above-mentioned trade-offs, an output voltage swing of $5V_{pp}$ was chosen, dictating a minimum W/L of about 5000 for M_{58}, the p-channel output device. The error amplifier is made of input differential pair M_{51} and M_{52} and current mirrors M_{53} and M_{54}. Load transistors M_{55} and M_{56} limit the dc gain to about 7. Note that the gain of the error amplifier is determined by the ratio of device sizes:

$$A_{\text{EP}} = \frac{gm_{M51,52}}{gm_{M55,56}}. \tag{15}$$

The quiescent current I_Q is also accurately set by the ratio of device sizes and the current source I_{ss}:

$$I_{Q_{M58}} = I_{ss} \times \frac{W_{M58}}{W_{M57}} \tag{16}$$

The complete circuit schematic of the line driver is shown in Fig. 8. Transistors M_1–M_{16} form the folded-cascode preamplifier. The preamplifier has two sets of balanced inputs in order to avoid loading the previous stage; differential-mode feedback is provided through one set of inputs configuring the line driver in the balanced voltage-follower mode while the other set is used as the input to the previous stage. The error amplifiers EP driving the p-channel output devices are composed of M_{31}–M_{35} and M_{51}–M_{55}; similarly, M_{41}–M_{45} and M_{61}–M_{65} are the error amplifiers driving the n-channel output devices (EN). The size of the n-channel devices M_{48} and M_{68} was chosen to match the transconductance of their p-channel counterparts. The output common-mode voltage is sensed by R_1 and R_2 and corrected by the amplifier composed of M_{20}–M_{24}.

Frequency compensation is a critical aspect of the design. Notice that as shown in Fig. 3, this circuit topology incorporates more than one feedback loop. Thus, to ensure overall stability, the stability criteria should be sat-

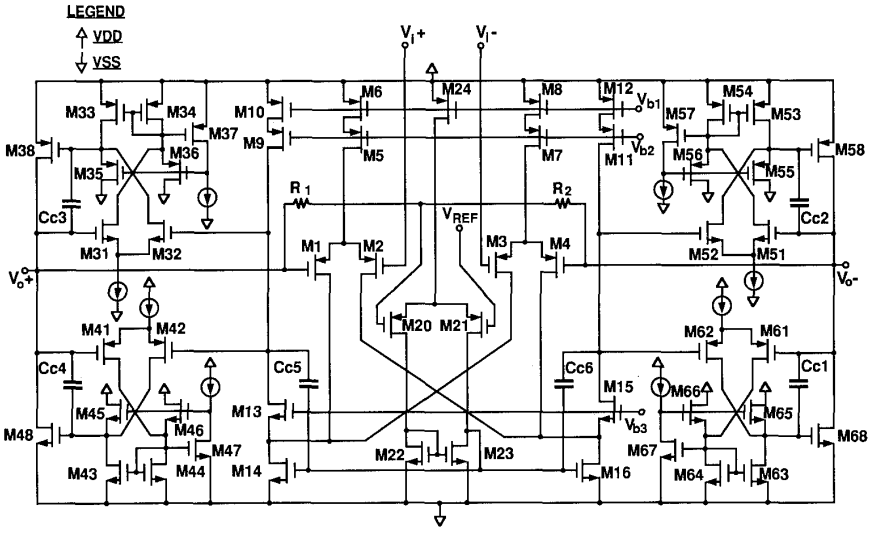

Fig. 8. Line-driver overall circuit schematic.

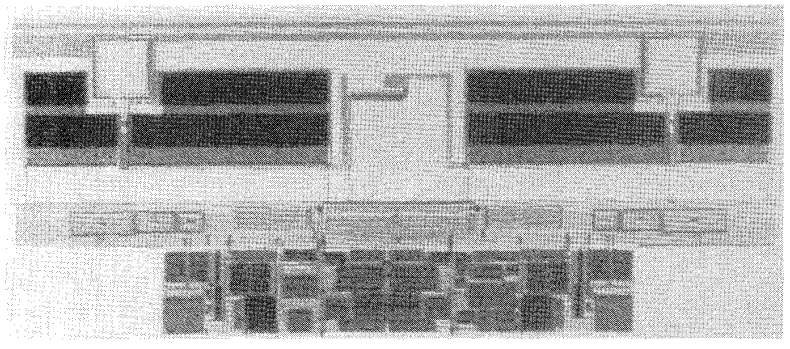

Fig. 9. Photomicrograph of the line driver.

isfied for both the inner loops and the outer loop for the entire range of load variations. Here, the output stages are compensated by C_{c1}–C_{c4}. Because of the large sizes of the output devices and hence large transconductances, the right half-plane zero [7] associated with the output devices is located at frequencies high enough so that their phase-shift contribution at the unity-gain frequency is negligible. Therefore no attempt was made to move the zero to the left-hand plane as is typically done for MOS amplifiers. The ratio of C_{c1}, C_{c4} to C_{c2}, C_{c3} is chosen to equalize the bandwidth for positive and negative signal excursions. The closed-loop dominant pole is determined by C_{c5} and C_{c6} in conjunction with the transconductance of the input devices. The location of the dominant pole is chosen based on several factors. First, high open-loop gain is required to suppress the dominant nonlinearities, in this case the third harmonic distortion. Thus, the maximum frequency of the third harmonic, 3×40 kHz, imposes an upper bound on the value of C_{c5} and C_{c6}. The upper limit for the dominant pole is set by the minimum required phase margin and the location of the lowest frequency nondominant pole.

In addition, by connecting the bottom plates of C_{c5} and C_{c6} to the common gate of M_{14} and M_{16}, the common-mode pole associated with this node is pushed to higher frequencies (pole splitting), thus improving the high-frequency common-mode rejection performance of the circuit.

IV. Experimental Results

The line-driver prototype is operated from a single 5-V supply and occupies an active area of 1.3 mm^2 in a 1.75-μm CMOS technology.

Fig. 9 shows the photomicrograph of the line driver. The circuit layout has a fully balanced structure. Matching of the transistors on the two balanced sides of the circuit is of significant importance; in particular, the matching of the input differential pairs M_1, M_2 and M_3, M_4 is a critical factor for the effective suppression of harmonic distortion. Hence, these four transistors are located side by side and are chosen to have channel lengths larger than the minimum possible length. To minimize thermal feedback effects, special attention was paid to preserve bal-

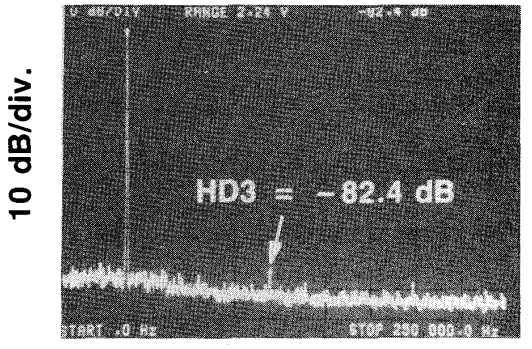

Fig. 10. Measured output spectrum of the prototype in response to a 40-kHz sinusoid signal and 60-Ω load and output voltage swing of $5V_{pp}$.

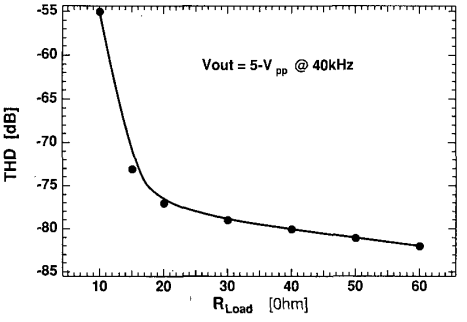

Fig. 11. Measured total harmonic distortion.

TABLE I
LINE-DRIVER PERFORMANCE SUMMARY
(V_{DD} = 5 V at T = 25°C)

Total Harmonic Distortion (V_{out} = $5V_{pp}$ at 40 kHz)	−82 dB for R_L = 60 Ω −77 dB for R_L = 20 Ω −73 dB for R_L = 15 Ω
Power Supply Rejection at 40 kHz	80 dB
Quiescent Power	36 mW
Closed-Loop Bandwidth	10 MHz
Active Area	1.3 mm^2

ance in thermal gradients associated with the line driver and the surrounding circuitry. Note that the output devices are built into the output bonding pads to keep the signal loss due to the series resistance associated with the output nodes to a minimum.

The measured output spectrum in response to a 40-kHz sinusoid and 60-Ω load exhibits a third harmonic distortion component at the −82-dB level as shown in Fig. 10. As expected, due to the fully balanced circuit topology and layout, the even harmonics are negligible compared to the odd harmonics. The measured total harmonic distortion for a $5V_{pp}$ 40-kHz signal as a function of the load impedance is shown in Fig. 11. Note that linearity better than 70 dB is maintained up to the worst-case load of 20 Ω. The rapid linearity degradation observed for loads smaller than 15 Ω is attributed to the output devices entering the triode region.

The performance of the line driver is summarized in Table I.

V. CONCLUSION

A CMOS line driver intended for ISDN *U*-interface transceiver applications has been described. Requirement considerations and trade-offs affecting linearity, power efficiency, and quiescent current were studied. A circuit structure featuring a highly linear input/output characteristic and well-controlled quiescent current was proposed and implemented. The prototype line driver is capable of delivering a $5V_{pp}$ signal to a 60-Ω load while exhibiting linearity in the order of 77 ± 5 dB and operating from a single 5-V power supply. Linearity better than 70 dB is maintained for load resistances as low as 20 Ω.

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