Experiment Report:
Study of Various Flip-Flop Circuits

Abhijnan Saraswat Gogoi
Roll no.: 2411072
PHY241 Course

7th November, 2025

Abstract

The experiment investigates the operation of RS, clocked RS, D, and JK flip-flop circuits using 7400-series logic ICs. These sequential circuits store one bit of data through feedback and exhibit state-dependent behaviour. The observed results verified bistability in the RS flip-flop, synchronous control in the clocked and D types, and toggling action in the JK flip-flop. The experimental observations agreed with the theoretical predictions.

1 Objectives

To construct and study the operations of the following circuits:

- RS Flip-Flop and clocked RS Flip-Flop
- D Flip-Flop
- JK Flip-Flop

2 Theory

So far, circuits encountered primarily involved combinatorial logic, where the output depends solely on the current inputs. However, many applications, such as counters, require the next output to depend on the current state (or output) stored previously. These circuits, which store/remember their current output or state, are known as **sequential logic circuits**. Sequential logic requires the ability to store the current state, that is, memory is required.

Memory is fundamentally achieved through a concept called feedback, where the output of a gate is routed back into its input. If Boolean gates are arranged correctly, they can store an input value. The memory elements used in these sequential circuits are called **flip-flops**. A flip-flop circuit stores a single bit of binary information and has two outputs: Q for the normal value and Q' for the complement value of the stored bit.

2.1 RS Flip-Flop

The RS flip-flop is the simplest possible memory element. It can be constructed using either two NAND gates or two NOR gates. The inputs R and S are referred to as the **Reset** and **Set** inputs, respectively. The outputs Q (normal output) and Q' (complement output) are complements of each other. The binary state of the flip-flop is determined by the value of Q. When $Q = 1$ and $Q' = 0$, the flip-flop is in the **set state** (or 1-state). When $Q = 0$ and $Q' = 1$, it is in the **reset/clear state** (or 0-state).

In this experiment, we have used NOR gates for construction (see figure 1a). The truth table for the RS flip-flop is given as follows:

Table 1: RS Flip-Flop Characteristic Table

R	S	Q	Q'	comment
0	0	Q_{n-1}	Q'_{n-1}	hold state
0	1	1	0	
1	0	0	1	
1	1	–	–	indeterminate

The R=1 and S=1 is an **unstable/indeterminate condition** because both outputs attempt to go to 0, which violates the requirement that Q and Q' must be complements. Since it is impossible to predict the final

output state, this condition must be avoided in normal operation, representing one of the main disadvantages of the RS flip-flop.

2.2 Gated or Clocked RS Flip-Flop

In sequential logic, it is often necessary for a bistable RS flip-flop to change state only when specific conditions are met, regardless of the S and R inputs. This is achieved by creating a Gated RS Flip-flop, typically by connecting a 2-input AND gate in series with each input terminal (S and R) of the RS NOR Flip-flop (see figure 1b). This modification introduces an extra conditional input called the **Enable (EN)** input.

When the Enable input (EN) = 0, the outputs of the two AND gates are at logic 0, regardless of S and R. This latches the outputs Q and Q' into their last known state. When $EN = 1$, the two AND gates become transparent to the S and R signals, and the circuit operates as a normal RS bistable flip-flop.

The Enable input can be connected to a clock timing signal, resulting in a "Clocked SR Flip-flop" which adds clock synchronization. The output change (Q_{n+1}) is summarized based on the previous output (Q_n) and the current inputs, assuming the clock input is at logic 1.

Table 2: Gated RS Flip-Flop Characteristic Table (EN/Clock = 1)

Q_n	R	S	Q_{n+1}
0	0	0	0 (Hold)
0	1	0	0
0	0	1	1
0	1	1	Indeterminate
1	0	0	1 (Hold)
1	1	0	0
1	0	1	1
1	1	1	Indeterminate

2.3 D Flip-Flop

The RS flip-flop is rarely used in actual sequential logic because of its undefined output when $R = S = 1$. The D flip-flop (where D stands for **data**) is a modification designed to resolve this issue.

The D flip-flop has only a single data input D. This D input is connected to the S input of an internal RS flip-flop, while the inverse of D ($\bar{D}$) is connected to the R input (see figure 1c). This arrangement ensures that R and S can never simultaneously be 1, thus eliminating the indeterminate state.

Like the Gated RS flip-flop, the D flip-flop includes an Enable (EN) input to allow for a holding state. The EN input is AND-ed with the D input. When $EN = 0$, the R and S inputs of the internal RS flip-flop are both 0, and the state is held, irrespective of D. When $EN = 1$, the S input equals D, and the R input is the inverse of D. Consequently, the output Q follows D. When EN returns to 0, the circuit remembers the most recent input D.

Table 3: D Flip-Flop Characteristic Table (EN/Clock = 1)

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

2.4 JK Flip-Flop

The JK flip-flop (named after Jack Kilby) is the most versatile and commonly used flip-flop. Like the RS flip-flop, it has two data inputs, J and K, and an EN/clock pulse input (CP). Unlike the RS flip-flop, the JK flip-flop has **no undefined states**.

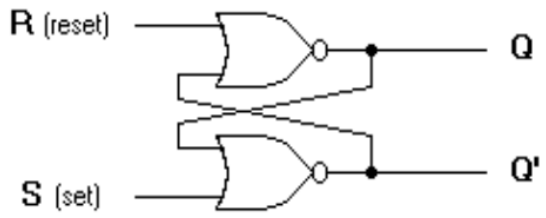
The fundamental difference in the JK flip-flop's design is the inclusion of **feedback paths** to the input AND gates: Q is AND-ed with K and CP, and Q' is AND-ed with J and CP (see figure 1d).

The characteristics of the JK flip-flop are as follows:

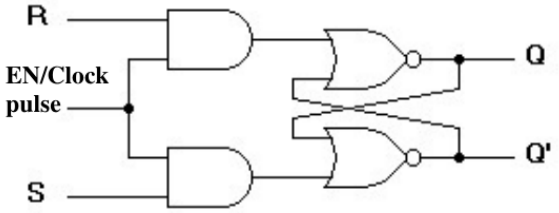
- **Set/Reset**: If one input (J or K) is 0 and the other is 1, the output is set or reset (by J and K respectively), similar to the RS flip-flop.
- **Hold State**: If both inputs are 0, the flip-flop remains in its same state when a clock pulse occurs, and the CP has no effect on the output.
- **Toggle State**: If both inputs are high ($J = 1, K = 1$), the flip-flop changes state (toggles) whenever a clock pulse occurs. The output will toggle repeatedly until the CP goes back to 0. This rapid oscillation is undesirable and led to the development of improved forms of this flip-flop, such as the Master-Slave JK Flip-Flop.

Table 4: JK Flip-Flop Characteristic Table

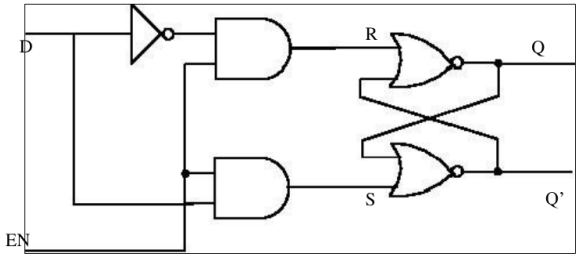
Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1 (Toggle, $\bar{Q}_n$)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0 (Toggle, $\bar{Q}_n$)



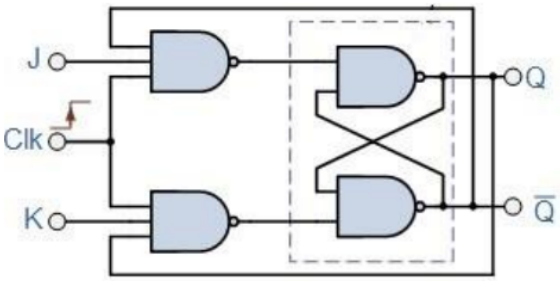
(a) RS Flip-Flip circuit



(b) Gated RS Flip-Flip circuit



(c) D Flip-Flip circuit



(d) JK Flip-Flip circuit

Figure 1: Circuit diagrams

3 Materials Required

(i) ICs (NOR-7402, 2-input AND-7408, 3-input NAND-7410, NAND-7400, NOT-7404), (ii) Breadboard, (iii) Connecting wires, (iv) DC power supply (5V), (v) Resistors (two 1kΩ), (vi) LED (two).

4 Observations

Table 5: RS Flip-Flop

R	S	Q	Q'	
0	1	1	0	
0	0	1	0	(hold)(after R,S = 0,1)
1	0	0	1	
0	0	0	1	(hold)(after R,S = 1,0)
1	1	0	0	(indeterminate)

Table 6: Gated RS Flip-Flop

Q_n	R	S	Q_{n+1}	
0	0	0	0	(hold)
0	0	1	1	
0	1	0	0	
0	1	1	–	(indeterminate)
1	0	0	1	(hold)
1	0	1	1	
1	1	0	0	
1	1	1	–	(indeterminate)

Table 7: D Flip-Flop

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Table 8: JK Flip-Flop

Q_n	R	S	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

5 Results

From the constructed circuits and observations, the following results were obtained:

- The RS flip-flop circuit correctly demonstrated the bistable property — maintaining its previous state when both inputs were 0, setting $Q = 1$ when $S = 1$, and resetting $Q = 0$ when $R = 1$. The indeterminate condition was verified for $R = S = 1$.
- The clocked (or gated) RS flip-flop operated only when the enable (clock) input was high. The circuit successfully held its previous state when $EN = 0$, validating its clock-controlled operation.
- The D flip-flop output Q followed the input D when $EN = 1$, and retained the last value of D when $EN = 0$. This confirmed its function as a data latch and eliminated the indeterminate state of the RS flip-flop.
- The JK flip-flop behaved as expected, performing set, reset, hold, and toggle operations. When $J = K = 1$ and a clock pulse was applied, the output toggled, confirming its edge-triggered and feedback-controlled operation.

The experimental truth tables matched with the theoretical characteristic tables for each type of flip-flop.

6 Discussion

The experiment demonstrated the basic principles of sequential logic circuits, where outputs depend not only on current inputs but also on the circuit's previous state.

The RS flip-flop verified the concept of bistability but also illustrated a limitation — the undefined condition when both inputs are high. The clocked RS flip-flop introduced synchronization, showing how clock or enable inputs regulate state changes to occur only under controlled timing conditions.

The D flip-flop provided a practical improvement over the RS type by ensuring that only one input line determines the state, effectively eliminating ambiguity. This feature makes it widely used in registers and memory elements for digital systems.

The JK flip-flop further extended functionality through feedback connections. The toggle action (for $J = K = 1$) highlighted its application in counters and frequency dividers.

7 Conclusions

The study successfully verified the working principles of RS, clocked RS, D, and JK flip-flops. Each flip-flop type was observed to store one bit of information, and the logical relationships between inputs and outputs were experimentally confirmed. The progression from RS to D to JK flip-flop illustrated the evolution of design aimed at improving stability, eliminating undefined states, and achieving synchronous control.

These circuits form the fundamental building blocks for complex sequential systems such as counters, shift registers, and memory storage units.

8 Precautions

1. The 74-series ICs interpret an unconnected (floating) input as HIGH; hence, all unused inputs must be grounded to prevent unpredictable behaviour.
2. Ensure firm and correct connections on the breadboard according to the IC pin configurations before powering the circuit.
3. Apply power supply only after verifying the wiring to avoid IC damage due to incorrect connections.
4. Use a regulated 5V DC supply, as over-voltage can permanently damage TTL ICs.