**Literature Survey**

**1.Ultra-Low Power Bandgap Voltage Reference**

**Overview**

This document presents a summary of the paper titled *"An Ultra Low Power Bandgap Operational at Supply From 0.75 V"* by Vadim Ivanov, Ralf Brederlow, and Johannes Gerber. The paper introduces a novel ultra-low-power reverse bandgap voltage reference capable of operating with supply voltages as low as 0.75 V, consuming only 200 nA of current. It is designed for integration into microprocessor systems and low-power battery applications.

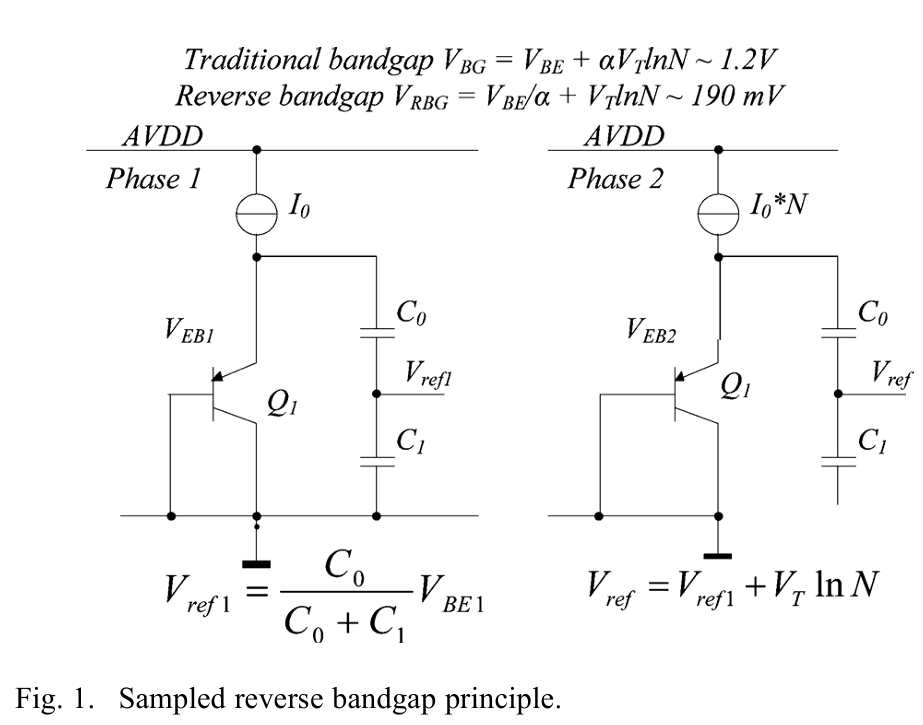
**Key Contributions**

1. **Innovative Reverse Bandgap Design**:
   * Utilizes a substrate PNP bipolar transistor in diode configuration.
   * Features a switched-capacitor voltage sampling scheme to generate temperature-stable voltage.
2. **Low-Power Consumption**:
   * Operates with an average current consumption of 15-20 nA (core) and 200 nA (total).
   * Achieves ultra-low energy consumption via discontinuous operation with a sample-and-hold (S/H) circuit.
3. **Accuracy**:
   * Untrimmed accuracy of 2.5% across a temperature range of -20 to 85°C.
   * Trimmed accuracy of 0.5%.
4. **Compact Design**:
   * Total chip area of 0.07 mm² using a 130 nm CMOS process.
   * Avoids costly trimming processes while maintaining performance.
5. **Flexibility and Integration**:
   * Compatible with systems requiring 256 mV and 900 mV references.
   * Suitable for on-chip ADCs and power-on-reset (POR) comparators.

**Design Details**

**1.Reverse Bandgap Core**

**Principle:** Combines proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) components

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**Implementation:** Uses low-gain substrate PNP transistors (common in CMOS processes) to generate a 186 mV reference voltage.

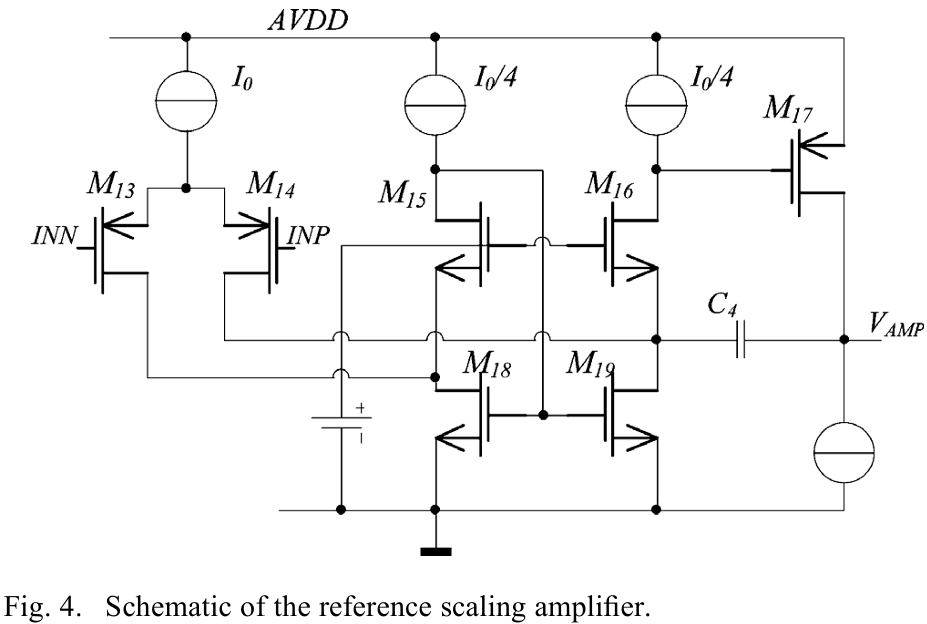
**Advantages:**

* High accuracy without high-gain PNP or NPN transistors.
* Operates with a supply voltage as low as 0.75 V.

**2.Scaling and Buffering**

**Scaling Amplifier:**

* Amplifies the 186 mV reference to 256 mV and 900 mV levels.
* Features auto-zeroing to minimize offset-induced errors**.**

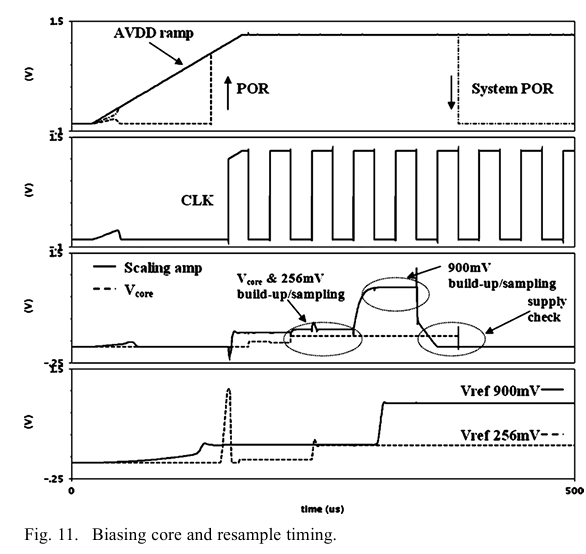
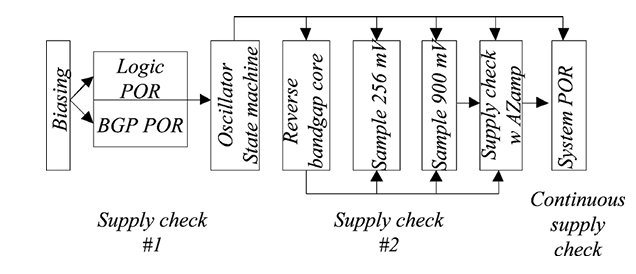
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**Sample-and-Hold Circuit:**

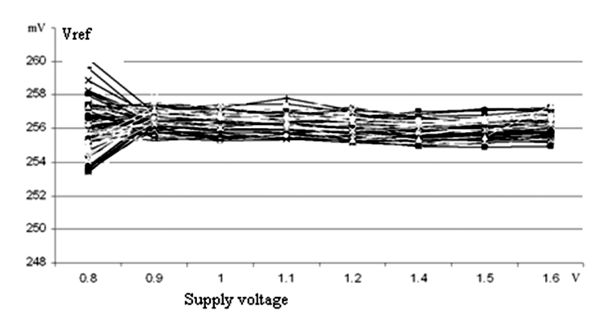
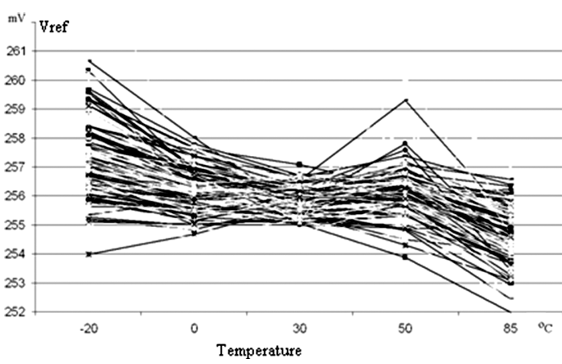
* Maintains reference voltage during inactive periods.
* Uses a low-leakage design to ensure long hold times (100 ms).

**Startup and Power Management**

* Incorporates a three-step startup procedure to ensure reliable operation:
  1. Biasing core activation.
  2. Comparator checks for supply voltage.
  3. Reference core and state machine activation.



**Experimental Results**



1. **Performance**:
   * Temperature stability comparable to classic bandgap references.
   * Supply voltage variation within acceptable limits.
2. **Area and Power Efficiency**:
   * 70,000 µm² layout, with resistors occupying 30% of the area.
   * Total power consumption: 170 nW.
3. **Production Variability**:
   * Untrimmed variation: 3% (3 sigma).
   * Trimmed variation: <0.5% (3 sigma).

**Comparison with Existing Solutions**

* **Advantages**:
  + Operates at significantly lower supply voltages.
  + Higher precision and lower power consumption compared to prior designs.
* Limitations:
  + Ripple during the sampling process, although not critical for intended applications.

**Conclusion**

This paper introduces a groundbreaking approach to ultra-low-power voltage references suitable for digital CMOS processes. The design achieves a remarkable balance between power efficiency, accuracy, and integration, making it a valuable component for modern battery-powered systems. The proposed techniques can pave the way for more energy-efficient and compact mixed-signal systems.

**2. Precision-Aware Subthreshold-Based MOSFET Voltage Reference**

**Overview**

This summary is based on the article *"Design of Precision-Aware Subthreshold-Based MOSFET Voltage Reference"* by Shuzheng Mu and Pak Kwong Chan. The paper introduces a novel subthreshold-based MOSFET voltage reference that provides low power consumption and high precision, demonstrating advancements in temperature compensation and process sensitivity for sensor circuits.

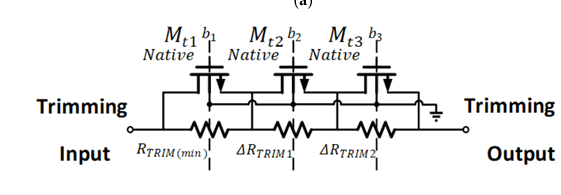
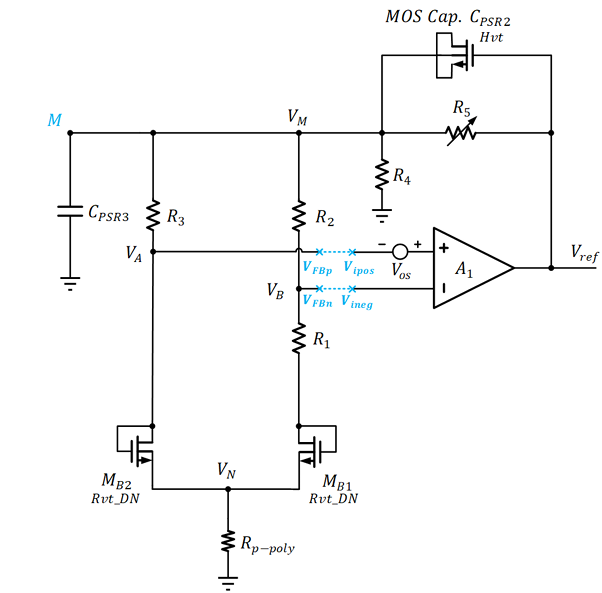
**Key Contributions**

1. **Novel Voltage Reference Design:**
   * Employs subthreshold-based MOSFETs rather than BJTs, enabling lower power consumption.
   * Achieves output stability through second-order temperature compensation.
2. **Low Power and High Precision:**
   * Consumes 9.6 μW at a supply voltage of 1.2 V.
   * Achieves a temperature coefficient (T.C.) of 3.0 ppm/°C with second-order compensation**.**
3. **Process and Power Supply Sensitivity:**
   * Process sensitivity of 0.75% after trimming.
   * Power Supply Rejection (PSR) of 71.65 dB at 100 Hz.
4. **Simplified Circuit Architecture:**
   * Minimal trimming requirements.
   * Uses fewer components than traditional designs

**Design Details**

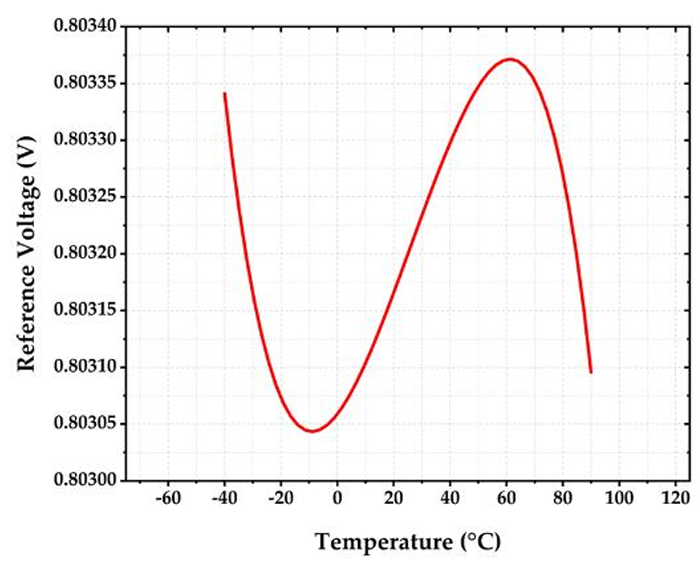
**Subthreshold-Based MOSFET Design**

1. **Operating Principle**: Utilizes the exponential relationship of subthreshold MOSFET currents to replace BJTs.

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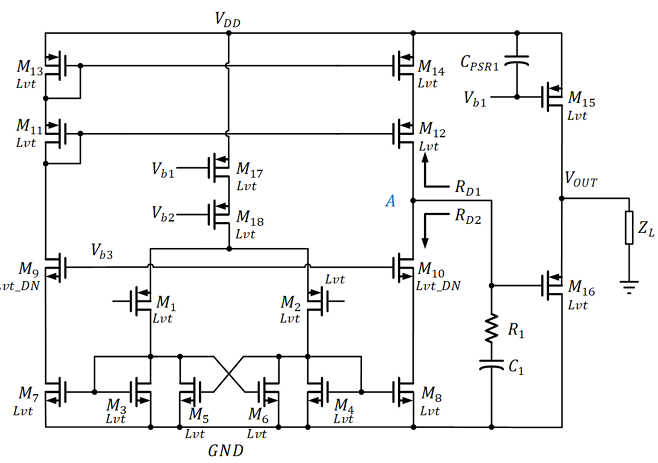
2.**Temperature Compensation**:

* PTAT and CTAT components cancel first-order and second-order temperature effects.
* Incorporates resistors with different temperature coefficients to achieve precise compensation.



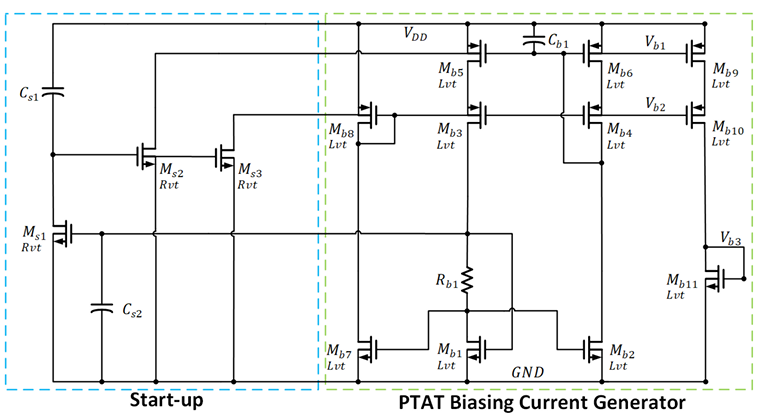
**Circuit Features**

1. **Voltage Reference Output**: Achieves an 800 mV output with high stability across temperatures.
2. **Operational Amplifier**: High-gain topology with bias circuits to enhance PSR and stability.



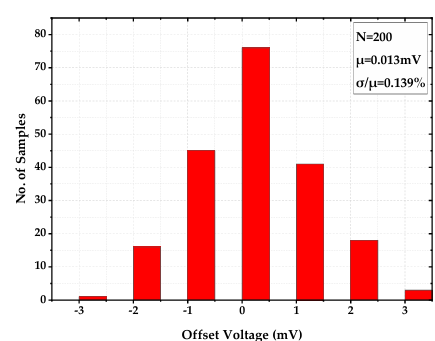
**3.Biasing Circuit**:

* 1. Generates PTAT currents to stabilize amplifier performance under varying conditions.
  2. Reduces startup time and improves supply independence.

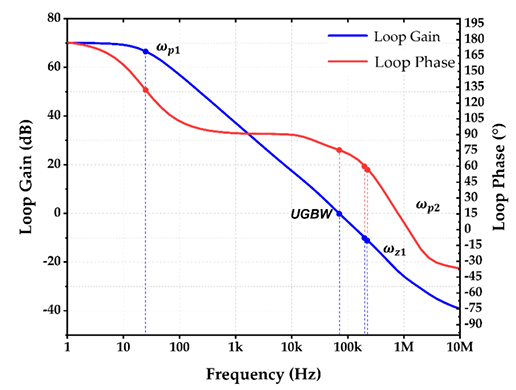


**Experimental Results**

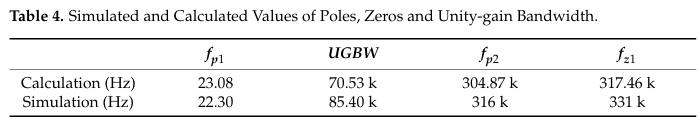
1. **Temperature Performance**:
   1. T.C. of 3.0 ppm/°C after second-order compensation (-40°C to 90°C).
   2. Demonstrates robustness across a wide temperature range.
2. **Power Consumption**:
   1. Total power consumption: 9.6 μW.
   2. Split between voltage reference circuit, operational amplifier, and biasing circuit.



1. **Monte Carlo Simulations**:
   1. Verified T.C. variation: 12.5 ppm/°C (mean) with a standard deviation of 7.99 ppm/°C.
   2. Offset voltage: 0.013 mV (mean), indicating minimal impact on output precision.

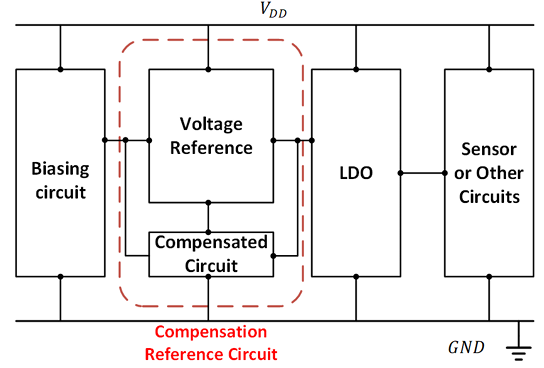
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1. **Comparison with Existing Works**:
   1. Superior precision and lower power consumption compared to other subthreshold MOSFET and BJT-based references.

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**Applications**

This design is ideal for:



* Sensor circuits with stringent accuracy requirements.
* Analog circuits demanding low power and high precision.
* Low-energy devices like biomedical implants and wireless sensor nodes.

**Conclusion**

The proposed subthreshold-based MOSFET voltage reference combines high precision, low power, and robust temperature stability in a simplified circuit architecture. Its design demonstrates significant improvements over conventional approaches, making it highly suitable for next-generation sensor and analog systems.

**3.Ultra-Low Voltage Subthreshold CMOS Voltage Reference**

**Overview**

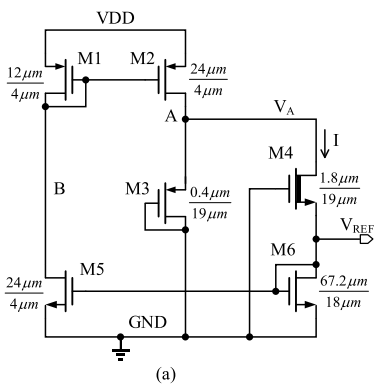
This summary is based on the article *"A 1-nW Ultra-Low Voltage Subthreshold CMOS Voltage Reference With 0.0154%/V Line Sensitivity"*. The paper introduces a novel subthreshold CMOS voltage reference designed for ultra-low power consumption and high insensitivity to supply voltage variations, making it ideal for Internet-of-Things (IoT) applications.

**Key Contributions**

1. **Innovative Voltage Reference Design**:
   * Utilizes a novel self-regulating circuit to minimize line sensitivity (LS).
   * Operates entirely in the subthreshold region without amplifiers or passive components.
2. **Exceptional Performance Metrics**:
   * Achieves a line sensitivity of 0.0154%/V over a supply voltage range of 0.5–1.8 V.
   * Power consumption as low as 1 nW at 25°C.
3. **High Precision**:
   * Temperature coefficient (T.C.) of 89.83 ppm/°C with minimal variation.
   * Demonstrates competitive power supply ripple rejection (PSRR) at multiple frequencies.
4. **Compact and Scalable Design**:
   * Fabricated in a standard 0.18 μm CMOS process with an active area of just 0.005 mm².

**Design Details**

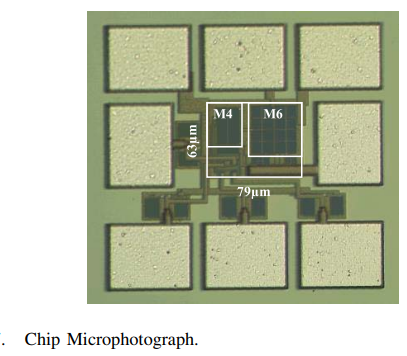
**Circuit Architecture**

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* **Self-Regulating Mechanism:**
* Eliminates the channel-length modulation effect in traditional 2-T CMOS designs.
* Incorporates a diode-connected transistor to stabilize voltage at critical nodes.
* **Subthreshold Operation:**
* Uses transistors with complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) characteristics to achieve temperature compensation

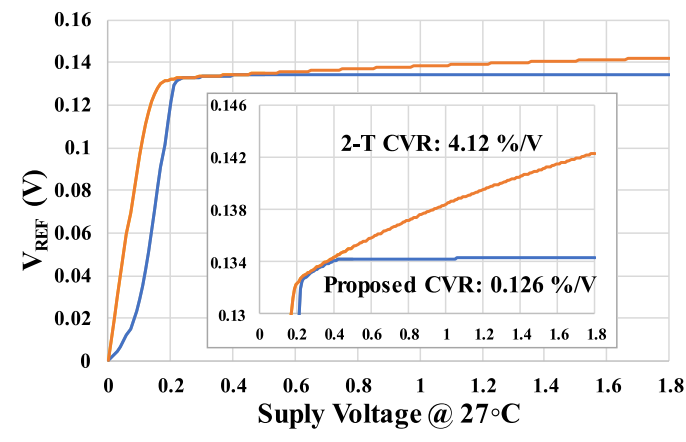
**Trimming Circuit**

* Adjusts the width of specific transistors to fine-tune the reference voltage and temperature characteristics.
* Minimizes area consumption by trimming one transistor instead of multiple.

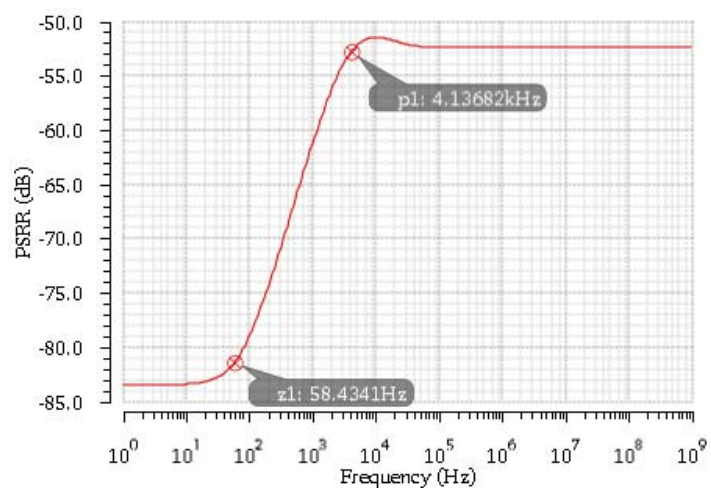


**Experimental Results**

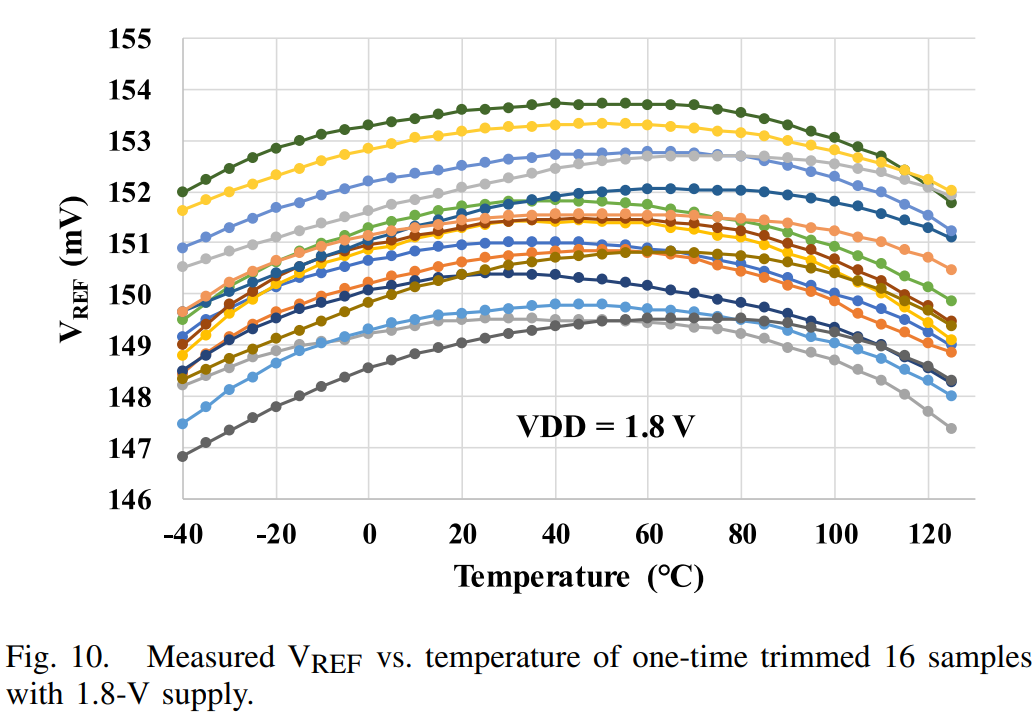
1. **Line Sensitivity:**
   * Demonstrates significant LS improvement compared to prior designs (0.0154%/V vs. 4.12%/V).



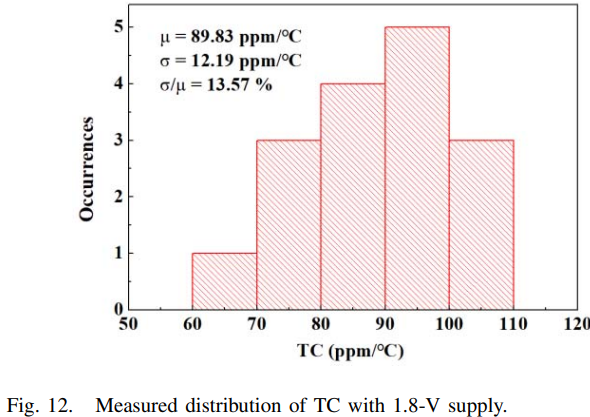
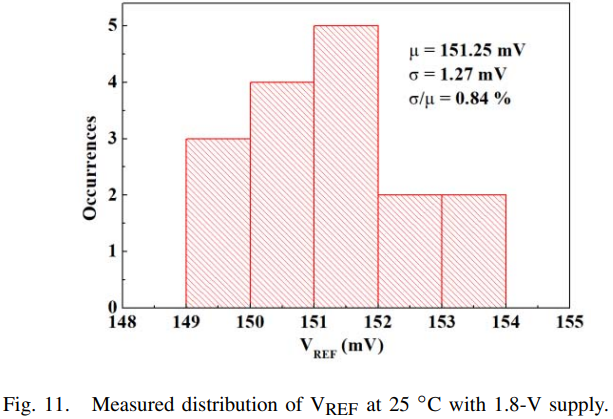
1. **Power Supply Ripple Rejection:**
   * Achieves -73 dB PSRR at 10 Hz, reducing to -49.8 dB at 1 MHz.



1. **Temperature Performance:**
   * Consistent output voltage over a wide temperature range (-40°C to 125°C).
   * Average reference voltage: 151 mV with a coefficient of variation of 0.84%.



1. **Monte Carlo Analysis:**
   * Low standard deviation in T.C. (12.19 ppm/°C) across tested samples, confirming robustness.



1. **Comparison with State-of-the-Art:**
   * Outperforms previous designs in LS and power efficiency while maintaining a compact form factor.

**Applications**

The proposed design is suitable for:

* IoT devices powered by ambient energy harvesting.
* Ultra-low-power sensors for biomedical or environmental monitoring.
* Systems requiring long-term operation without battery replacement.

**Conclusion**

The proposed subthreshold CMOS voltage reference achieves ultra-low power consumption (1 nW), exceptional line sensitivity (0.0154%/V), and high precision in a compact 0.005 mm² chip. Its novel self-regulating circuit ensures robust performance across voltage and temperature variations, making it ideal for IoT and low-power applications.

**4.Subthreshold Voltage Reference with DIBL Compensation**

**Overview**

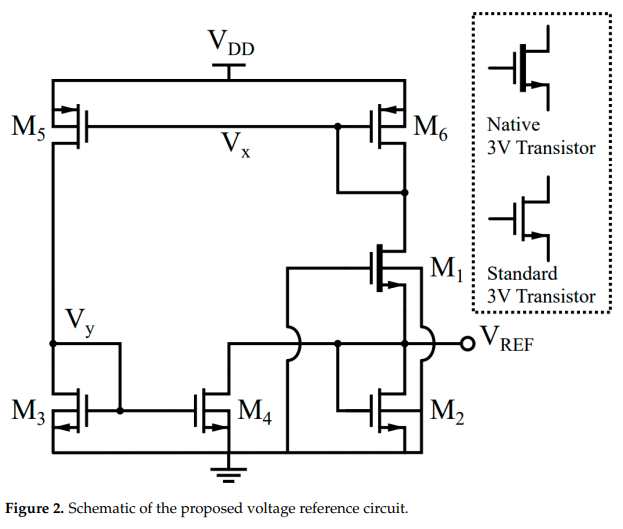
The paper *"A 21.4 pW Subthreshold Voltage Reference with 0.020 %/V Line Sensitivity Using DIBL Compensation"* presents an ultra-low-power voltage reference designed for energy-constrained applications, such as IoT and biomedical systems. This design innovatively uses drain-induced barrier lowering (DIBL) compensation to achieve high line sensitivity and stability while consuming only 21.4 pW at 0.6 V.

**Key Contributions**

1. **Innovative Voltage Reference Design**:
   * Employs a two-transistor (2-T) core with native NMOS and standard NMOS transistors.
   * Implements DIBL effect compensation to enhance line sensitivity (LS) without complex circuits.
2. **Exceptional Energy Efficiency**:
   * Achieves a power consumption of just 21.4 pW.
   * Operates over a supply voltage range of 0.6–1.8 V.
3. **Superior Performance**:
   * Line sensitivity of 0.020%/V after trimming, among the best for subthreshold references.
   * Temperature coefficient (T.C.) of 24.8 ppm/°C across -20 to 80°C.
4. **Simplified Architecture**:
   * Requires no self-biasing feedback loops or startup circuits, reducing circuit complexity and area.
5. **Compact Design**:
   * Occupies an area of only 0.003 mm² in 180 nm CMOS technology.

**Design Details**

**Circuit Architecture**

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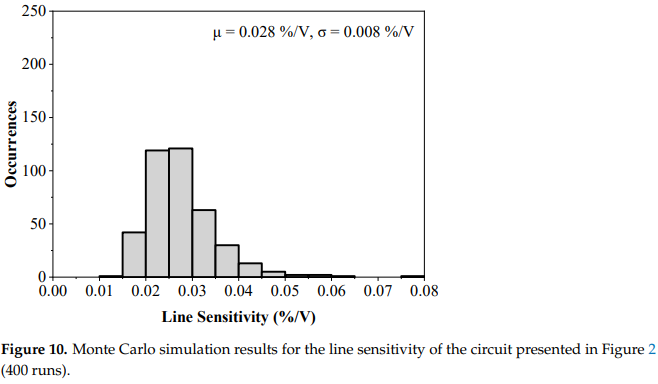
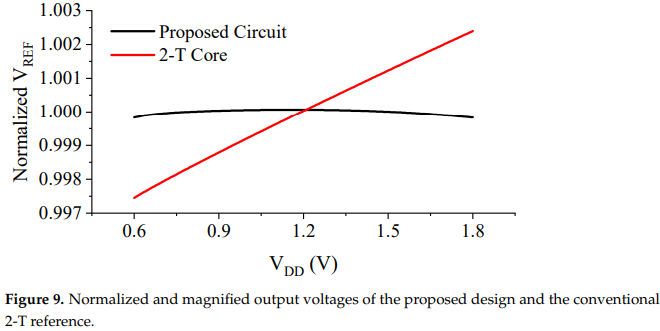
* **DIBL Compensation:**
  + Corrects the impact of the drain voltage on the threshold voltage using auxiliary transistors.
  + Generates a stable biasing current independent of the supply voltage.
* **2-T Core:**
  + Consists of a native NMOS transistor (M1) and a standard NMOS transistor (M2).
  + Produces a stable reference voltage derived from their threshold voltage difference.

**Trimming Circuit**

* A 4-bit trimming circuit adjusts current mirror ratios to minimize LS under process variations.

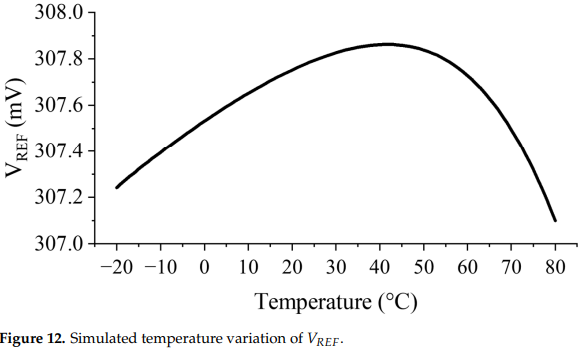
**Experimental Results**

1. **Line Sensitivity:**

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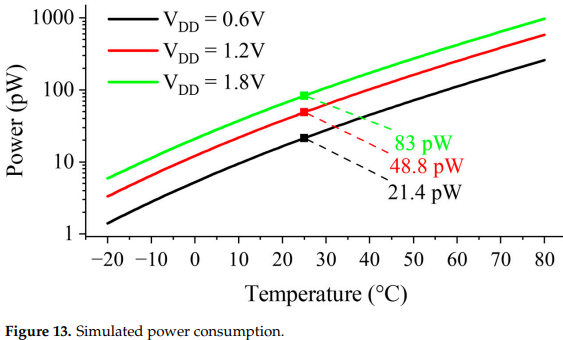
* + Untrimmed LS: 0.035%/V.
  + After trimming: LS reduced to 0.020%/V.

1. **Temperature Coefficient:**

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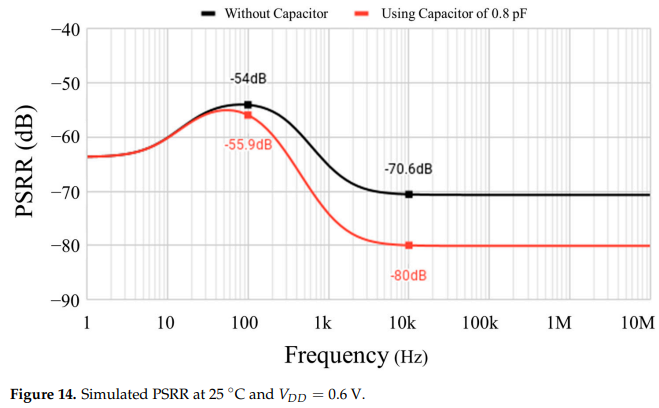
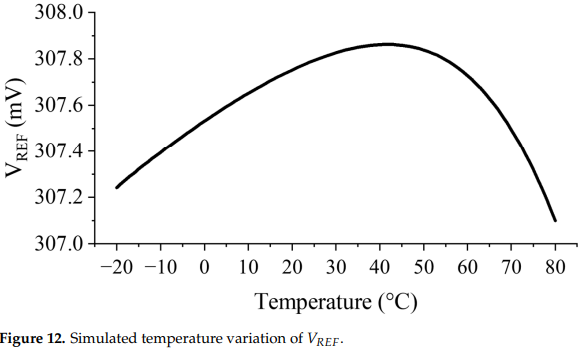
* + Simulated T.C. of 24.8 ppm/°C at 0.6 V.

1. **Monte Carlo Analysis:**
   * Verified robustness across 400 samples, maintaining LS within 0.035%/V.
2. **Power Efficiency:**

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* + Consumes 21.4 pW at 0.6 V, increasing to 83 pW at 1.8 V.

1. **Comparison with Existing Works:**
   * Outperforms previous designs in LS, power consumption, and area efficiency.

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**Applications**

The proposed design is highly suited for:

* Ultra-low-power IoT sensors.
* Biomedical implants requiring minimal energy consumption.
* Battery-operated systems with tight area and power constraints.

**Conclusion**

The proposed subthreshold voltage reference achieves ultra-low power consumption (21.4 pW), excellent line sensitivity (0.020%/V), and robust temperature stability (24.8 ppm/°C). Its compact, simplified design eliminates the need for complex circuits, making it ideal for energy-constrained applications like IoT and biomedical systems.

**REFERENCE**

1. **Y. Osaki, T. Hirose, M. Yano, and T. Kuroda, "An Ultra Low Power Bandgap Operational at Supply From 0.75 V," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 11, pp. 1301–1305, Nov. 2017, doi: 10.1109/TCSII.2017.2737679.**
2. **M. Azimi, M. Habibi, and H.-R. Karimi-Alavijeh, "Design of Precision-Aware Subthreshold-Based MOSFET Voltage Reference," *Journal of Low Power Electronics and Applications*, vol. 11, no. 3, pp. 21–29, 2021, doi: 10.3390/jlpea11030021.**
3. **Y. Osaki, T. Hirose, M. Yano, and T. Kuroda, "A 1-nW Ultra-Low Voltage Subthreshold CMOS Voltage Reference With 0.0154%/V Line Sensitivity," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 6, pp. 2232–2236, Jun. 2019, doi: 10.1109/TCSI.2019.2904567.**
4. **M. Shahpasandi, H. Yu, and J. Woo, "A 21.4 pW Subthreshold Voltage Reference with 0.020 %/V Line Sensitivity Using DIBL Compensation," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 1, pp. 15–24, Jan. 2023, doi: 10.1109/JSSC.2022.3189104.**
5. **Lee, D. Sylvester, and D. Blaauw, "A Subthreshold Voltage Reference With Scalable Output Voltage for Low-Power IoT Systems," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1443–1447, May 2017, doi: 10.1109/JSSC.2016.2642218.**