FPGA Image Processing

Task 1: Implementation of Pixel Summation Algorithm for the Image using Verilog HDL.

Approach:

- In the first step we have to convert the RGB image to .hex pixel image format. We can use python or MATLAB for doing this task.
- In the second step we have to processes this .hex pixel image according to our required output using Verilog HDL.
- In the third step we have to reconstruct this .hex pixel image output file after the processing again with python or MATLAB.

Step 1:

- Conversion of RGB image to .hex pixel file as the pixel manipulation of the image cannot be done using the Verilog HDL if the image is present in any standard forms like .jpg, .png, .bmp etc.,
- It is preferred to use bitmap (.bmp) format image for the image processing rather than any other standard formats like .jpg, .png etc.,

.jpg format → Contains lossy compression which permanently discards less important data and removes high frequency data to reduce file size. It causes Altering pixel values, Chroma subsampling and Quantization. These compression techniques effect the .hex pixel data when converted form .jpg form to .hex form.

.png format → Contains lossless compression without losing data but contains an alpha channel along with the RGB channels (RGBA format) which controls the transparency (opacity) of the pixel of the image. This alpha channel will he lost when the .png image is converted to .hex format for the processing.

.bmp format → Contains only the raw pixel data without any compression inside the .bmp image which is convenient for the processing and accurate reconstruction of the image for better results.

- These compression characteristics of the .jpg and .png format images has limitations while reconstructing the .hex image file again to its own format. So it is preferrable to use .bmp file for the image processing.
- So this .bmp image file is converted to .hex image file which contains the only raw pixel data and meta data file is also saved separately which contains the data like height, width and format of the image which are required at the time of reconstruction of the image.

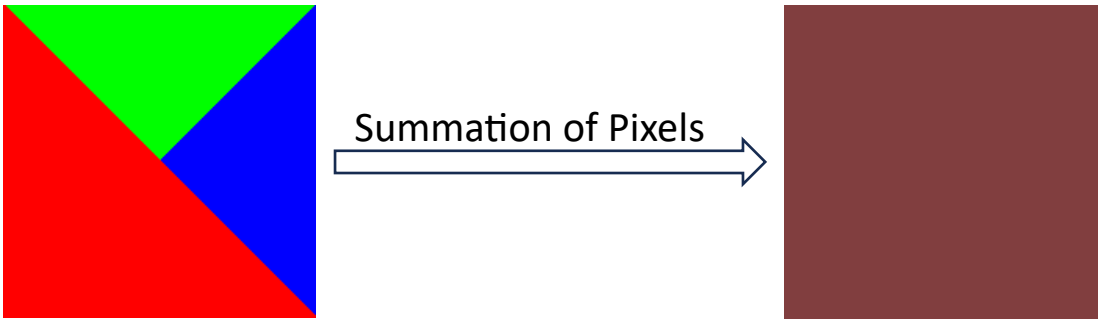
Step 2:

- The .hex image pixel file which is generated in the step 1 is given as an input to Verilog program for the pixel manipulation of the image.
- The pixels are modified according to the algorithm specified in the Verilog program.
- Then the output result of the manipulated pixel .hex file (Summation of pixel output) is saved as specified in the Verilog program.

Step 3:

- The output .hex image file obtained in the Step 2 is again reconstructed as the image of same height and width of the initial image using the same process as step 1.

Result:



Input .bmp file

Output .bmp file

Vivado Simulation Result: