

FIFO BUFFER ON FPGA

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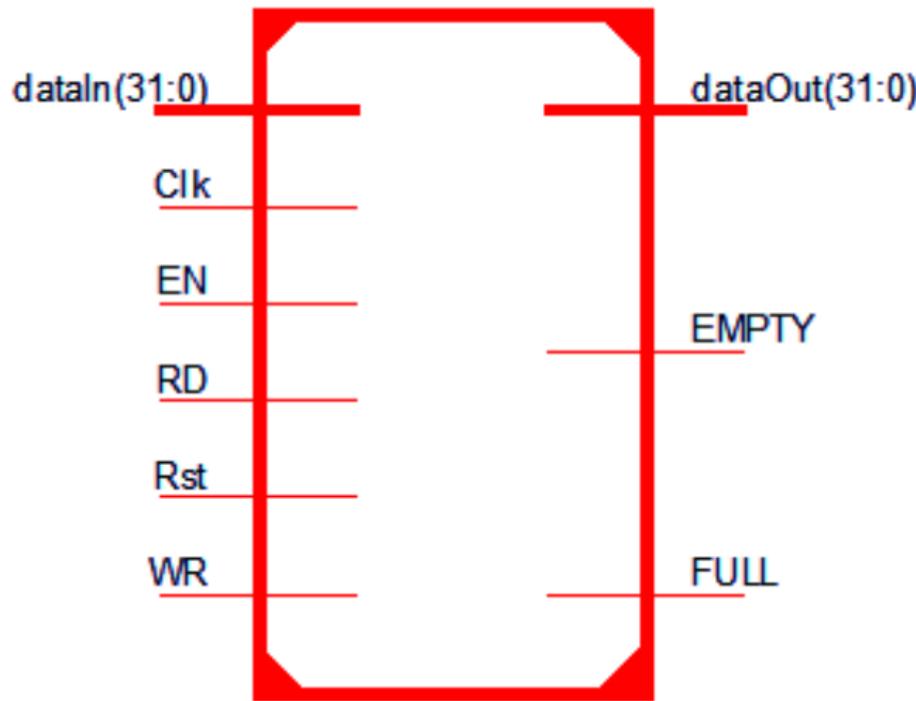
EE16BTECH11001

April 26, 2019

INTRODUCTION

- In this project we have implemented an FIFO buffer on icoboard, which is used for serial communications, video storage and transmission, matrix multiplications.
- FIFO(First In First Out) buffer implemented takes 2 inputs write and read. If write is enabled data is taken as input if buffer is not full. If read is enabled it gives out the first entered element in the buffer if buffer is not empty. It also has two flags Empty, Full which are enabled when buffer is empty, full respectively.

FIFObuffer



Implementation

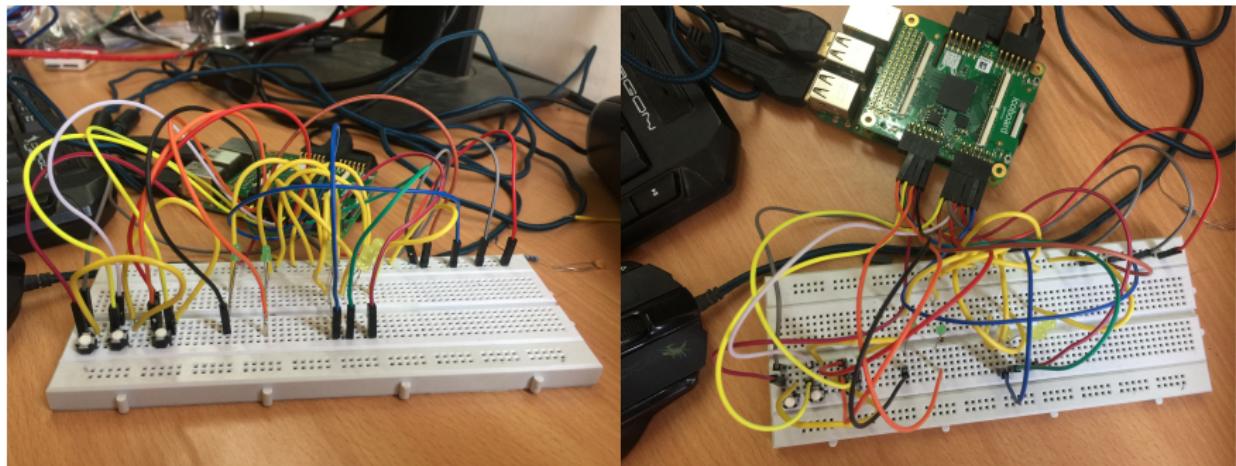
Here is the algorithm to implement FIFO buffer:

- First allocate required memory for the buffer. And initialize two registers that is read register and write register which shows which position to read or which position to write. Initially buffer will be empty so both registers have value 0 (starting position of buffer).
- whenever write is enabled the write register increases its value by 1 and checks whether write register and read register have same value. If so buffer is full and takes input from data input pins.
- whenever read is enabled the read register increases its value by 1 and checks whether write register and read register have same value. If so buffer is empty. And gives output through data output pins.
- Whenever reset is enabled read and write registers will be assigned 0, empty will be HIGH, full will be LOW.

Hardware Implementation

- As we are using icoboard as fpga, We use inbuilt clock for clock input.
- We assign icoboard io pins to our required inputs and outputs and same pins are written .pcf file which contains pin configurations of icoboard.
- We connect buttons to reset, read , write inputs.
- Connect LED's to all outputs(empty, full, data out pins)

Circuit



THANK YOU!!