Institute of Engineering and Technology (IET) JK Lakshmipat University, Jaipur

Design & Analysis of Arithmetic Circuit from Reversible Logic Gates:

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Submitted To:
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Acknowledgment:

I would like to express my sincere gratitude to the Semiconductor Research Center at Punjab Engineering College (PEC), Chandigarh for providing access to Cadence design tools, which have been instrumental in the successful completion of this work. The resources and support available at the center have greatly contributed to my understanding and implementation of VLSI design methodologies using Cadence Virtuoso.

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1. Introduction

As the scaling of CMOS technology progresses below 45 nm, challenges such as increased power dissipation, leakage currents, and short-channel effects become significant. Traditional irreversible logic circuits suffer from fundamental energy loss

as described by Landauer's principle, which states that each bit of information lost results in a minimum energy dissipation of *kTln(2)* joules.

Reversible logic, by contrast, provides a one-to-one mapping between input and output vectors, thereby eliminating information loss and minimizing energy dissipation. These properties make reversible logic an ideal approach for low-power, high-efficiency arithmetic circuit design, particularly when implemented using emerging nanotechnologies like Carbon Nanotube Field Effect Transistors (CNTFETs).

In this work, reversible logic gates such as Toffoli, Peres, and Fredkin are utilized to construct arithmetic units such as adders. The circuits are modeled and simulated using Cadence Virtuoso, where CNTFET device models are integrated through Verilog-A to analyze and compare performance parameters like power consumption, delay, and Power Delay Product (PDP).

2. Problem Statement

Irreversible logic circuits inherently lose information during computation, leading to energy dissipation. With the continuous shrinking of technology nodes, the impact of this energy loss is amplified due to leakage currents and switching activity.

Reversible logic provides an alternative design approach that preserves information and reduces heat dissipation. However, synthesizing reversible arithmetic circuits efficiently remains a challenge due to constraints such as garbage outputs, quantum cost, and circuit depth.

The objective of this work is to design reversible arithmetic circuits and analyze their performance focusing on power, delay, and PDP.

3. Objectives

1. To design reversible logic gates such as Toffoli, Peres, and Feynman.
2. To construct arithmetic circuits including **reversible full adder and reversible multiplier**.
3. To simulate and verify the functionality of reversible circuits.
4. To calculate and compare performance parameters such as **power, delay, and PDP**.
5. To study how reversible logic can contribute to low-power future computing architectures.

4. Methodology:

4.1 Reversible Logic Gates Used

- **Toffoli Gate (CCNOT Gate):**
  A 3×3 reversible gate used for implementing controlled inversion and AND logic functions, making it useful in arithmetic and control circuits.

- **Peres Gate:**
  A 3×3 reversible gate known for its low quantum cost and high efficiency in adder design due to combined XOR and controlled operations.

- **Feynman Gate:**
  A 2×2 reversible gate commonly used for XOR operations and signal copying, enabling fan-out without breaking the reversibility condition.

4.2 Circuit Design Steps

1. **Design of Reversible Gates:**
   - Toffoli, Peres and Feynman gates designed and verified logically.
2. **Adder Construction:**
   - Reversible Full Adder using a combination of Toffoli gates.
3. **Simulation Setup:**
   - Transient analysis simulations performed.
   - Supply voltage typically sets around 0.9–1.8 V.
   - Performance metrics extracted: Power, Delay.

5. Modules Implemented :

1. **Implementation of Toffoli Gate:**
   - Verified logic operation through transient simulation.
   - Outputs confirmed one-to-one mapping property.

2. **Implementation of Peres Gate:**
   - Designed and simulated successfully using CNTFET transistors.
   - Verified functional correctness.

3. **Design of Reversible Full Adder:**

   - Constructed using a combination of Toffoli, Peres and Feynman gates.

- Functional verification completed.

4. **Simulations Performed:**
    - Transient performed on all gates.
    - Comparative power and delay measurements taken.

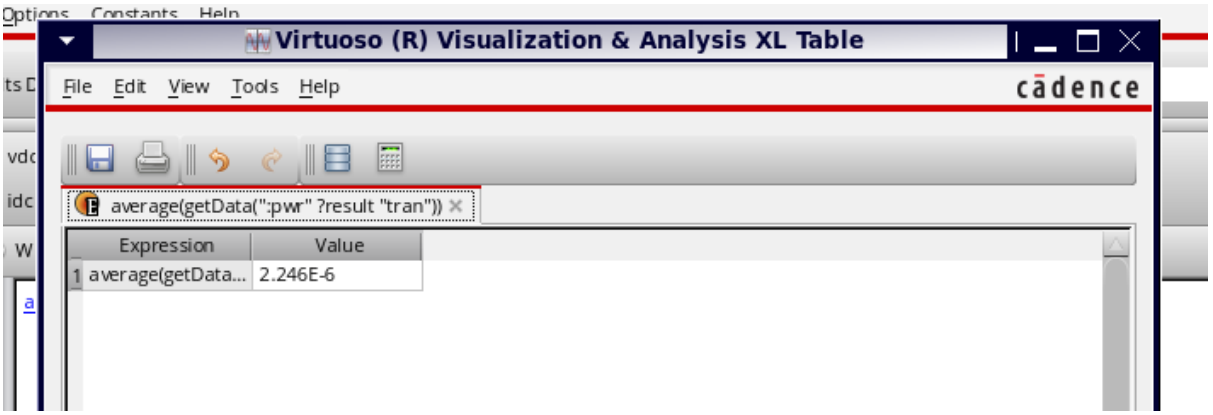
6. Results:

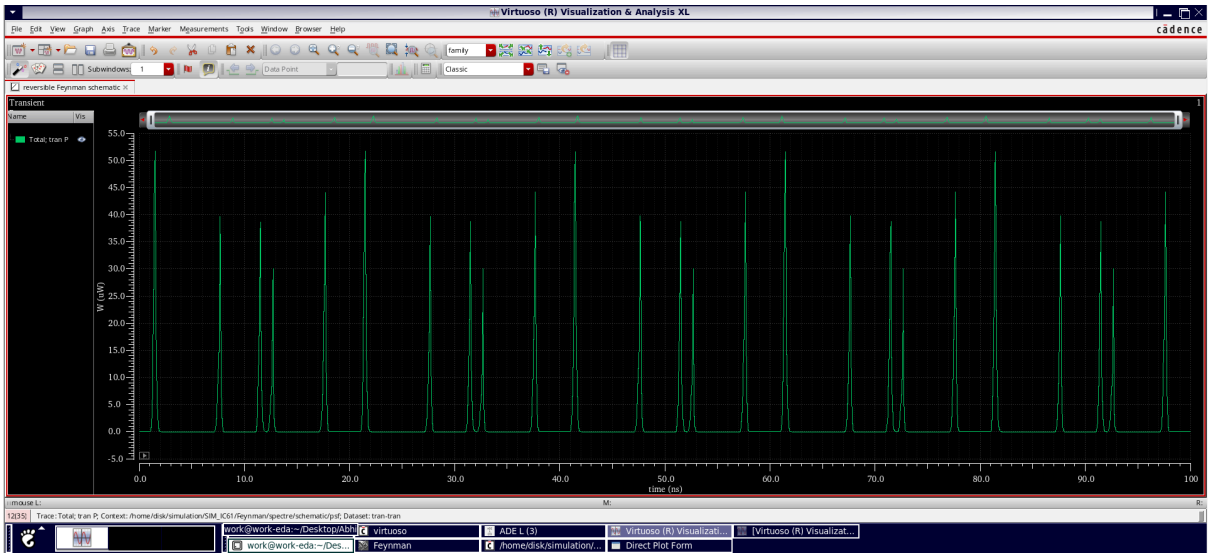
- Peres gate design achieved the lowest quantum cost and transistor count.
- Simulations confirm successful logical and transient behavior.

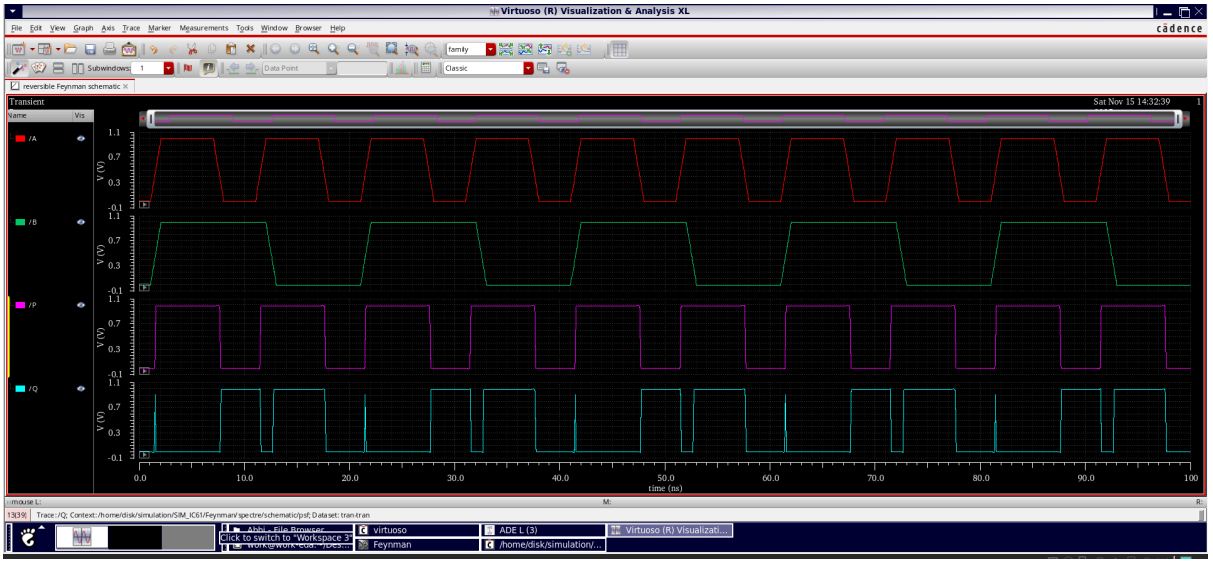
7. Simulations:

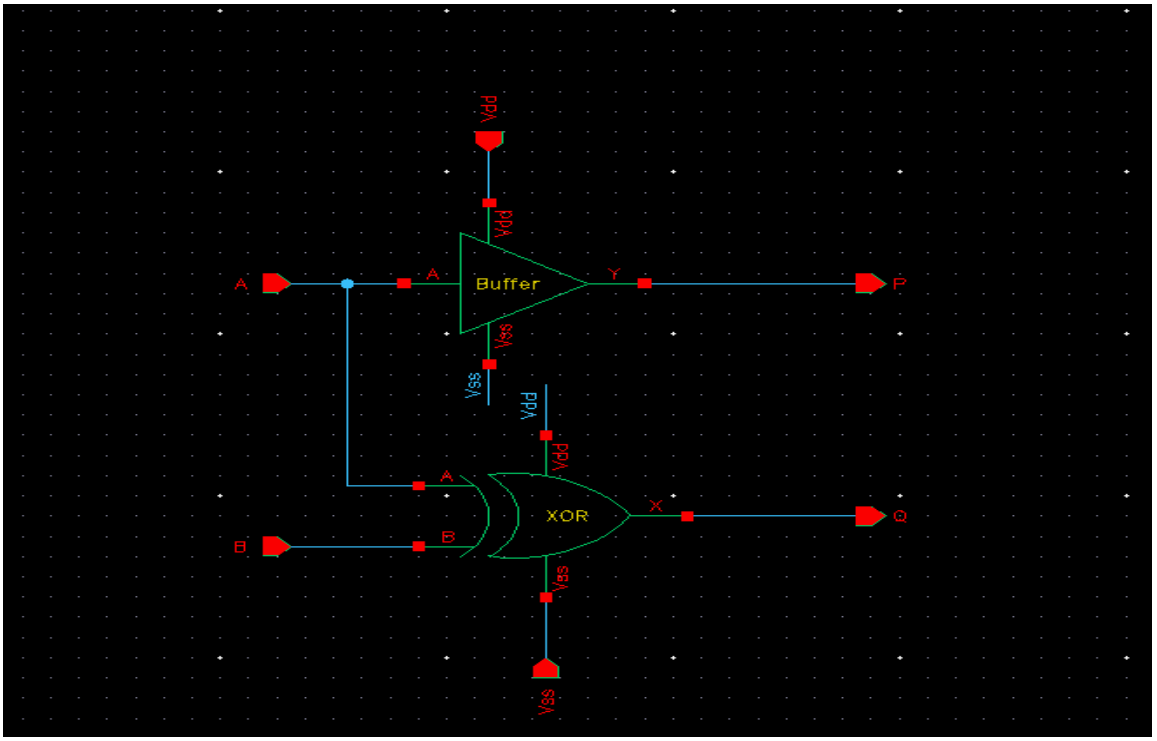
Feynman gate:

Power Dissipation:





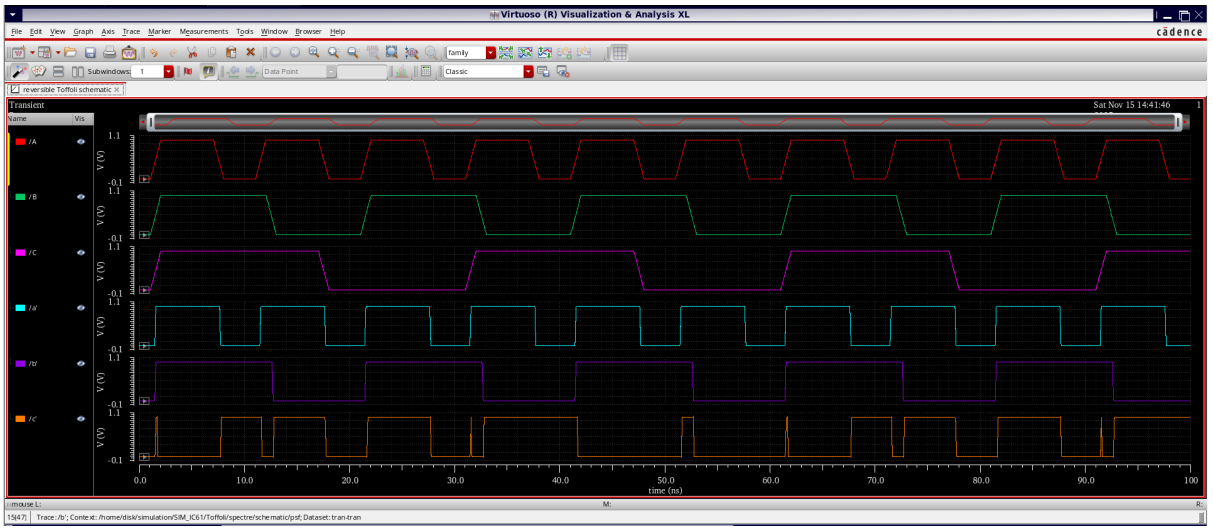




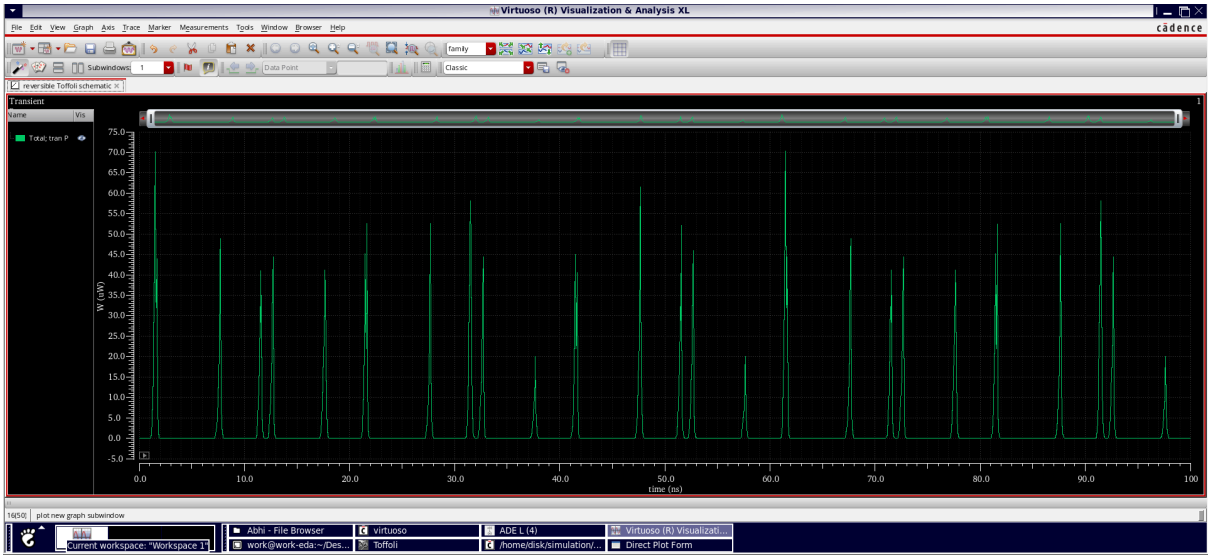
Delay:

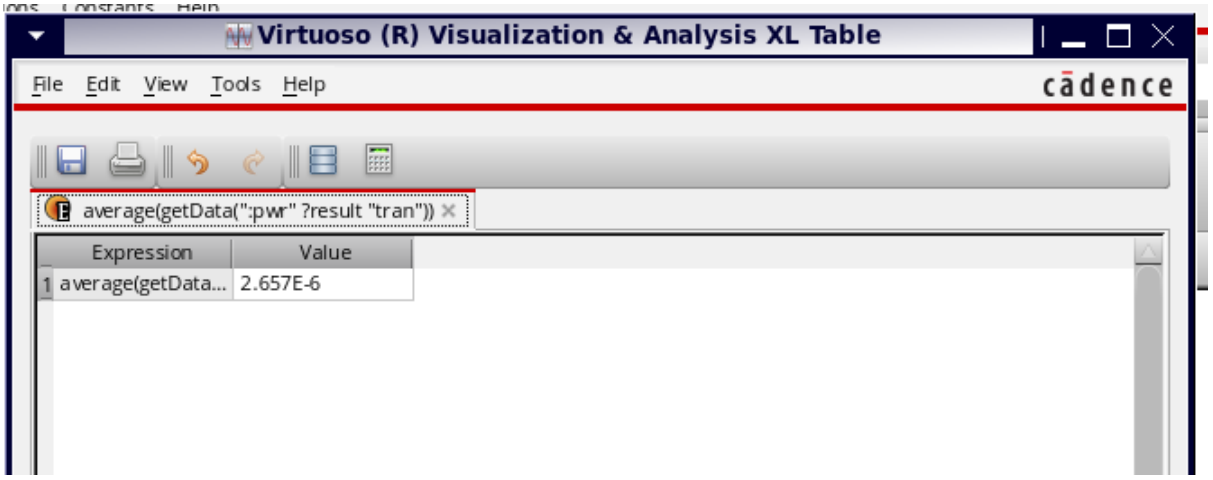
Inputs	P	Q
A	0.018ns	5.05ns
B	5.04ns	7.548ns

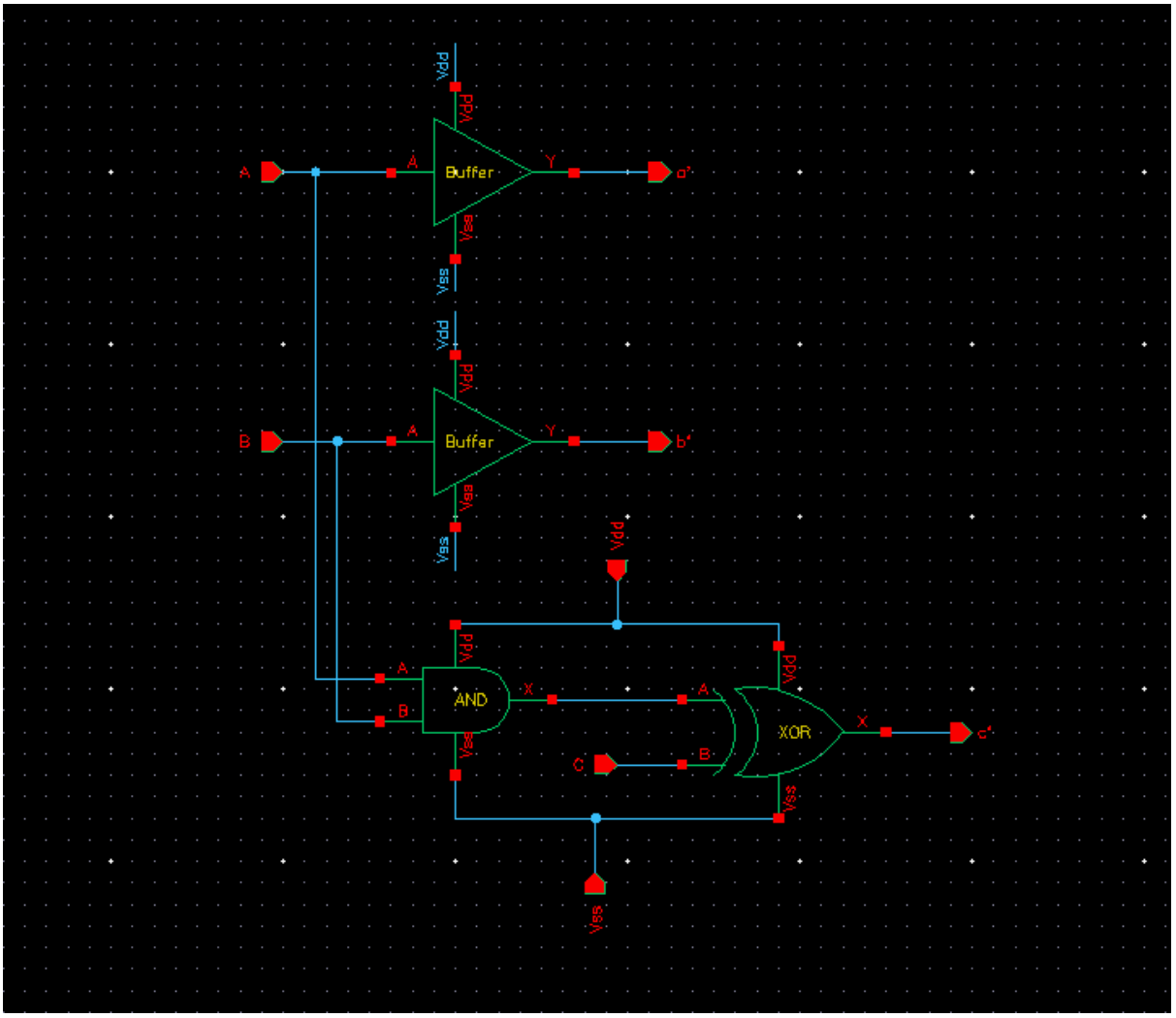
Toffoli Gate:



Power Dissipation:



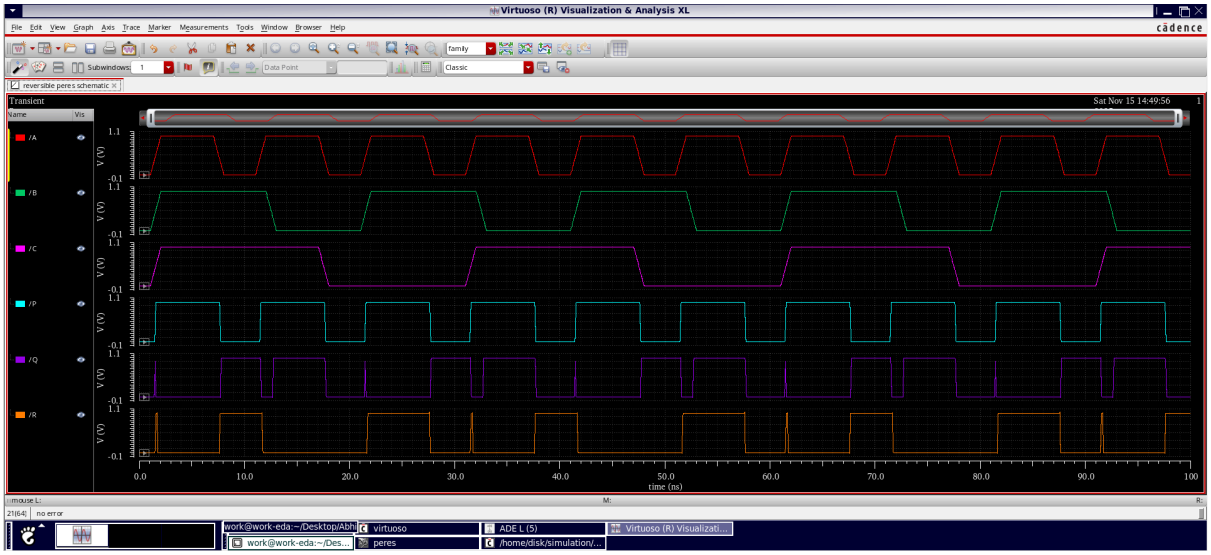




Delay:

Inputs	a’	b’	c’
A	0.21ps	2.52ns	2.43ns
B	2.52ns	0.018ns	4.934ns
C	2.52ns	5.01ns	66.88ps

Peres gate:



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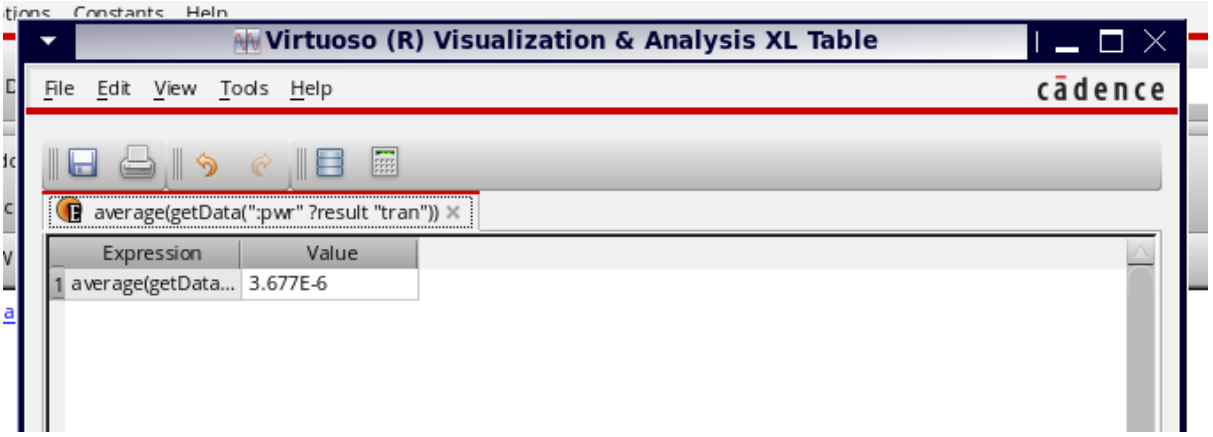
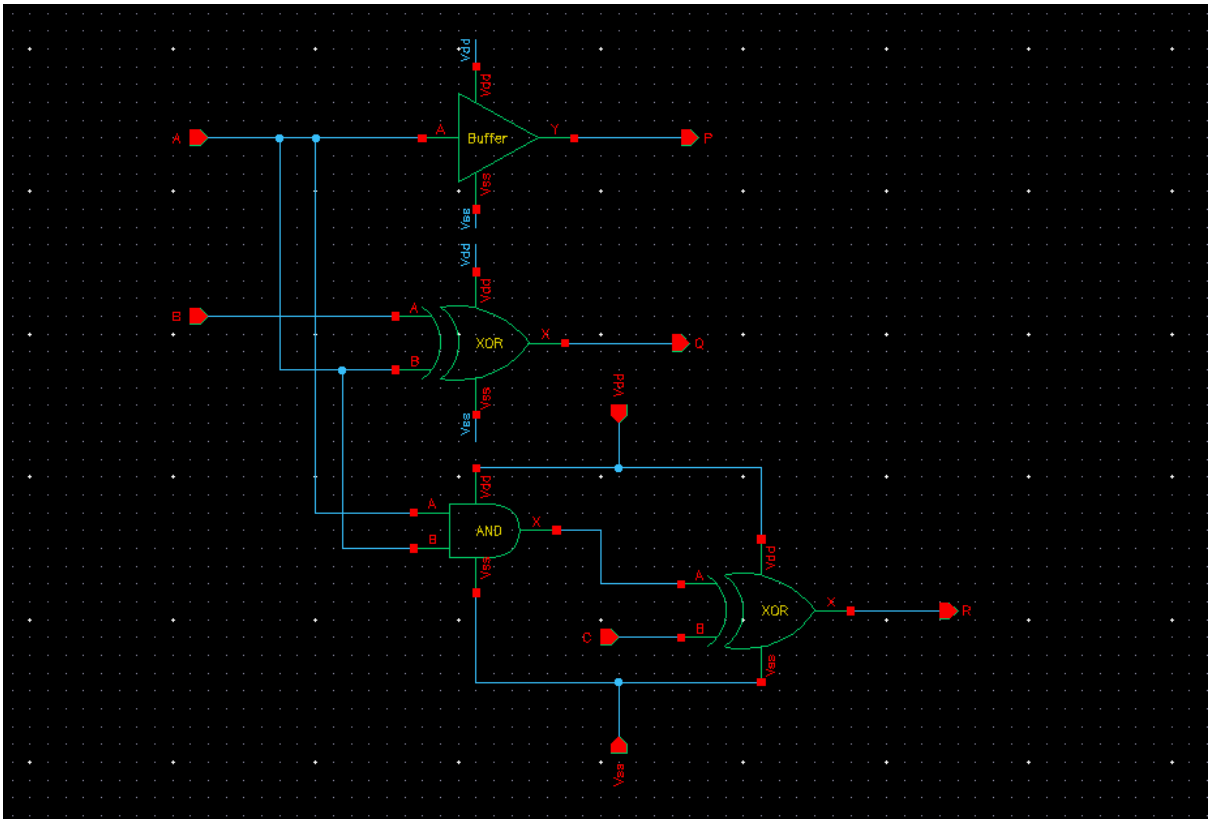
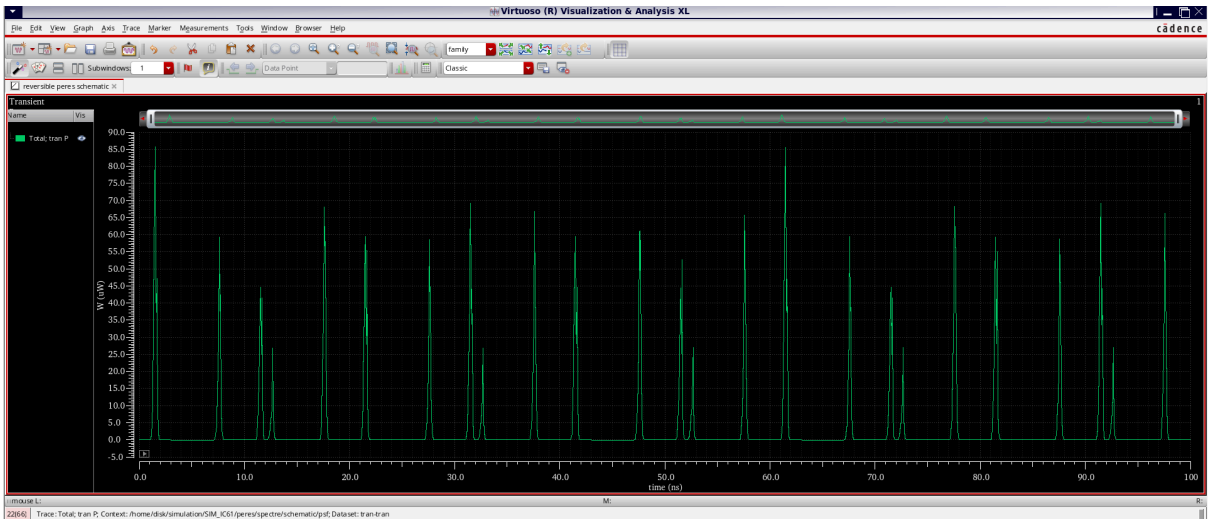


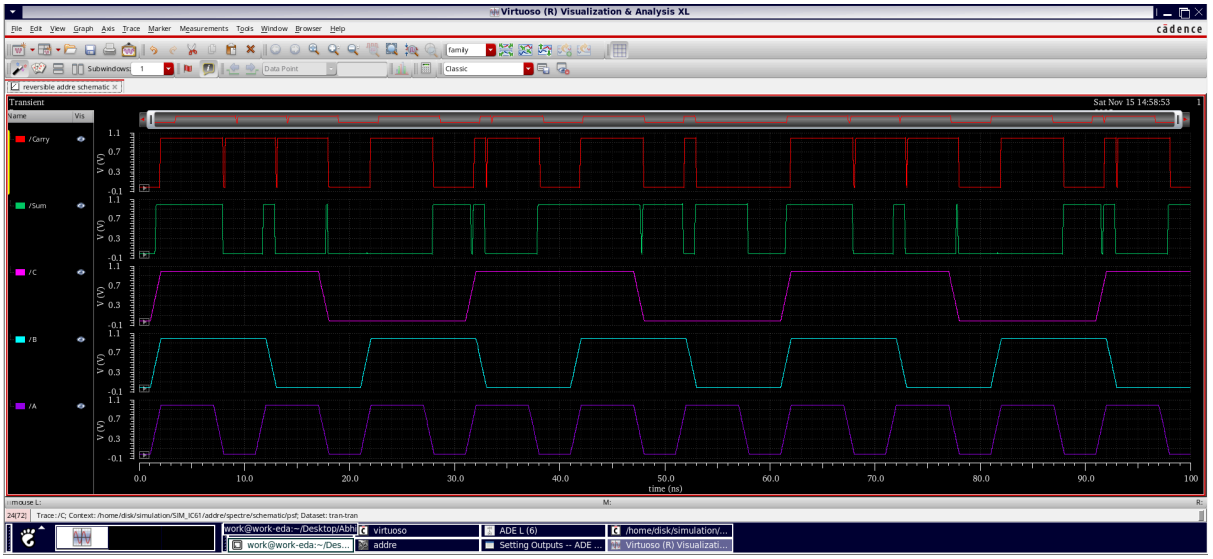


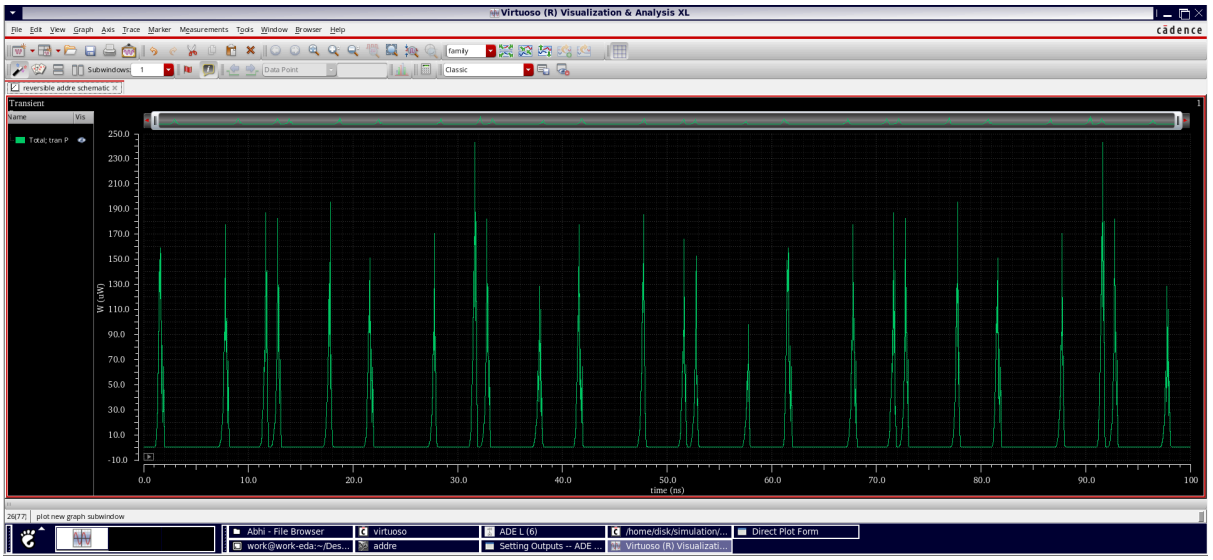


Delay:

Inputs	P	Q	R
A	0.271ns	7.548ns	2.43ns
B	2.479ns	5.049ns	4.934ns
C	4.979ns	2.549ns	7.534ns

Adder90nm:





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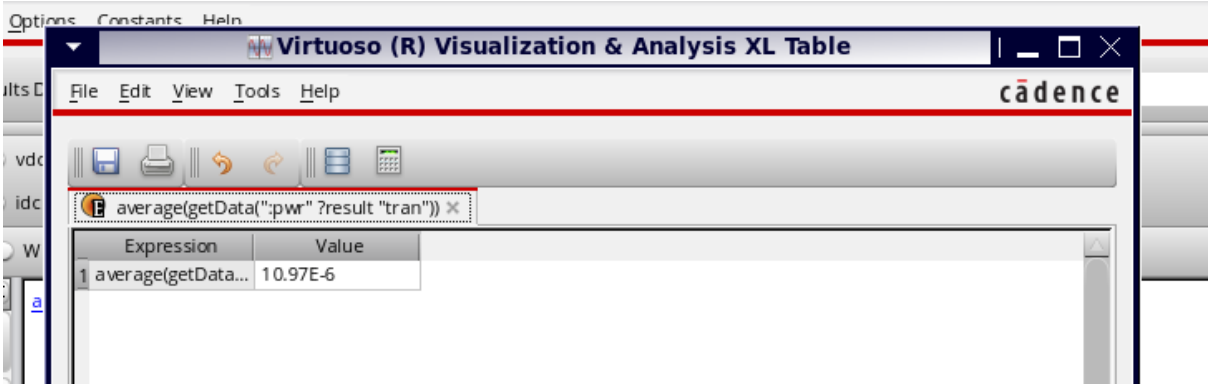
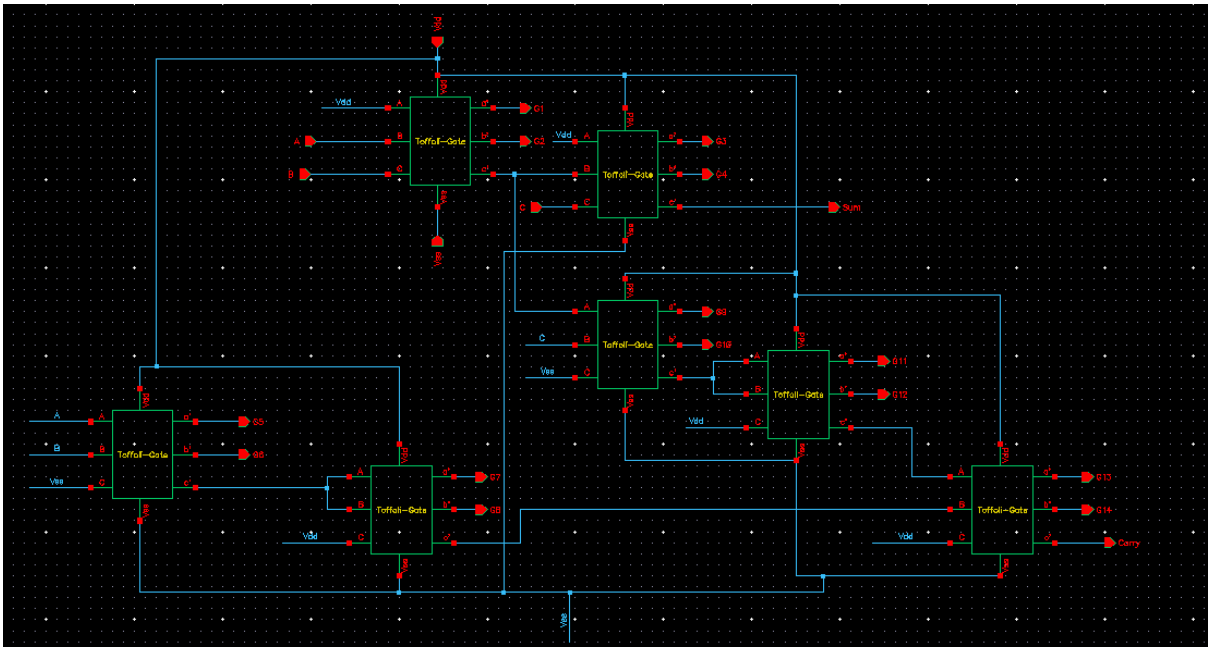
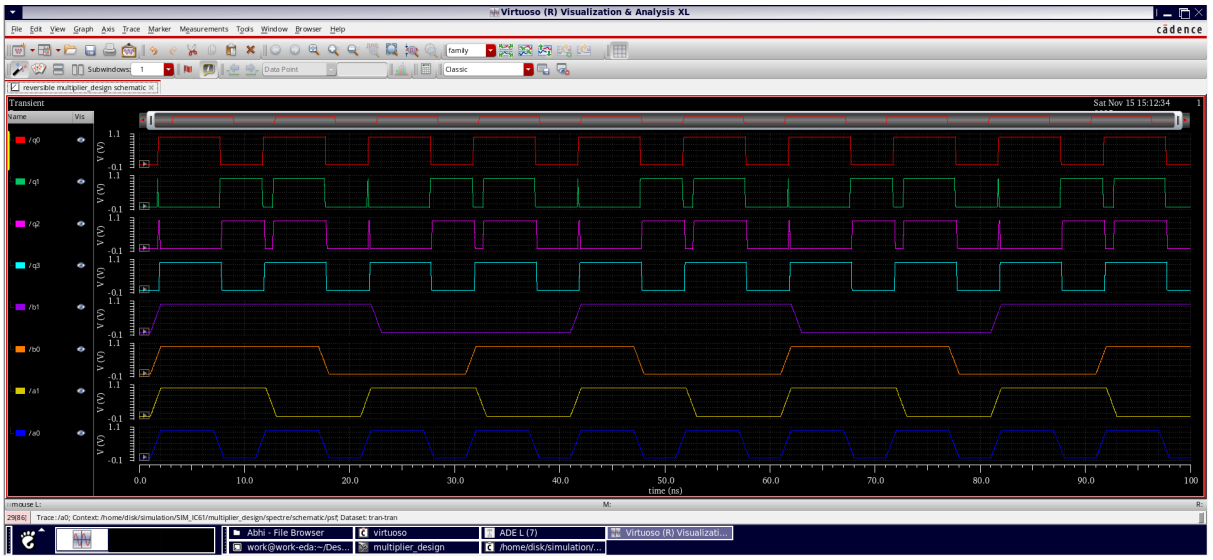


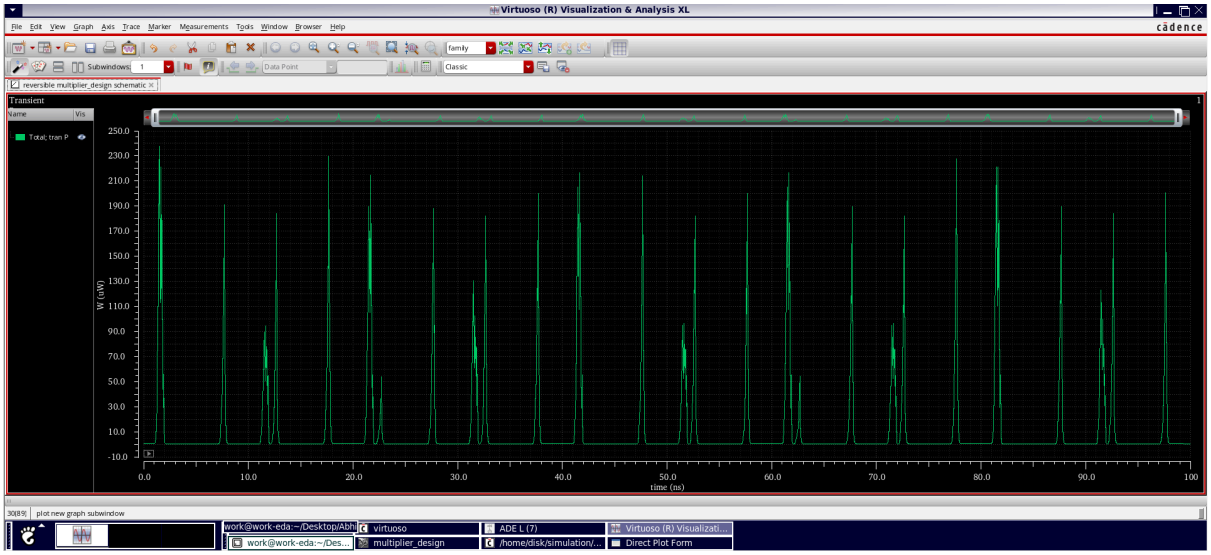


Delay:

Inputs	Sum	Carry
A	0.13ns	0.3225ns
B	2.37ns	2.33ns
C	4.87ns	4.68ns

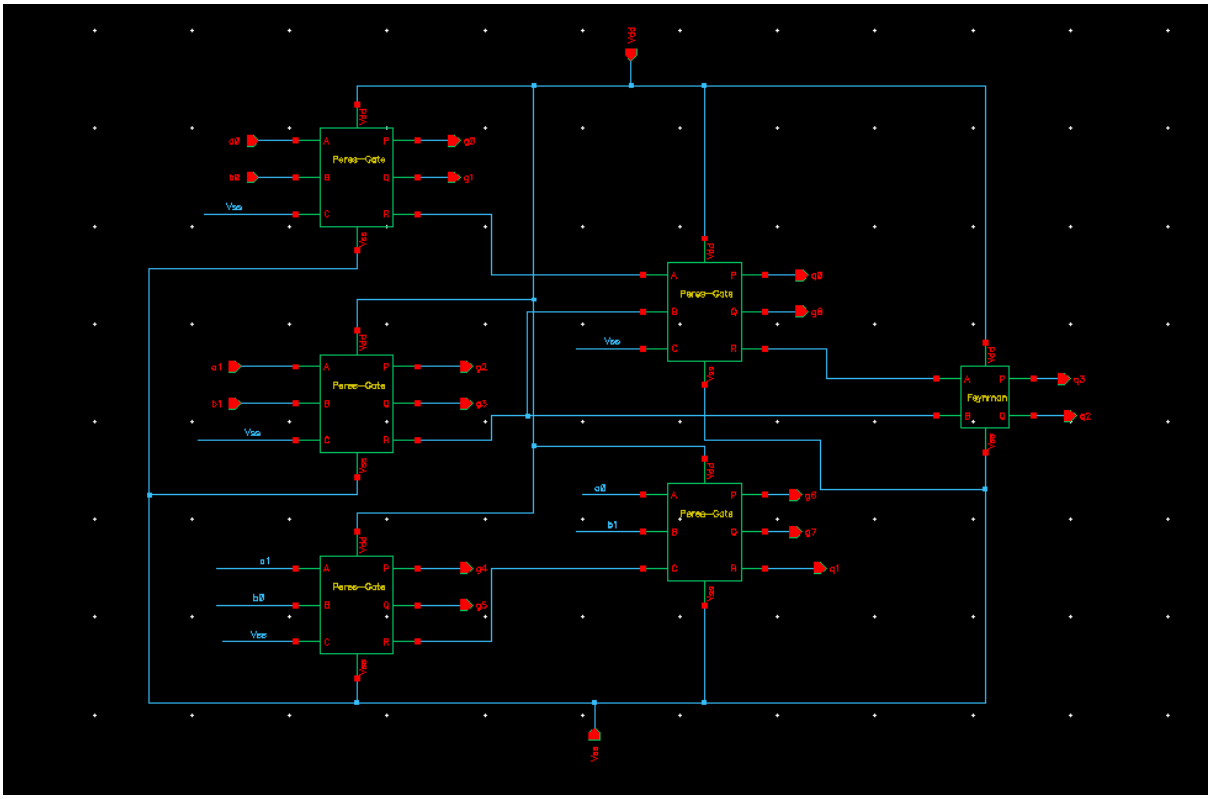
Multiplier_90nm:



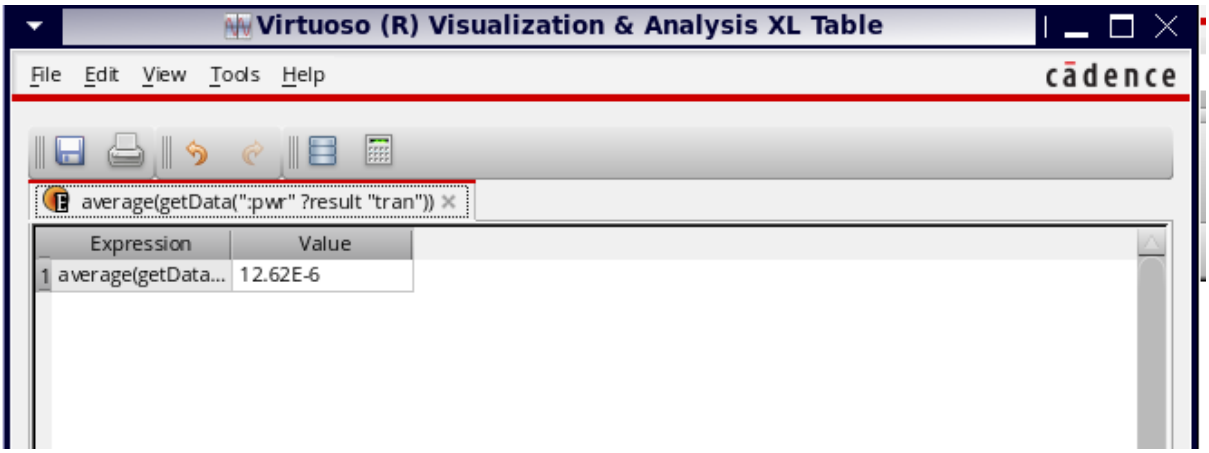


Delay:

Inputs	q0	q1	q2	q3
a0	0.1375ns	2.373ns	2.26ns	0.2475ns
b0	4.8605ns	7.375ns	7.2655ns	4.7545ns
a1	2.3625ns	4.87ns	4.1767ns	2.252ns
b1	7.361ns	9.875ns	9.7655ns	14.509ns

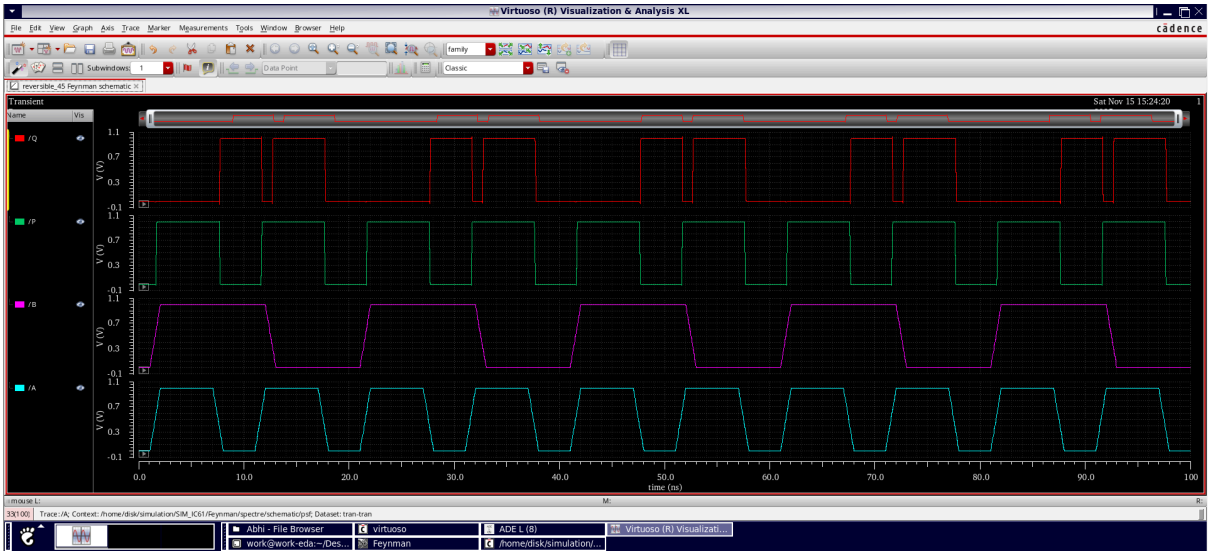


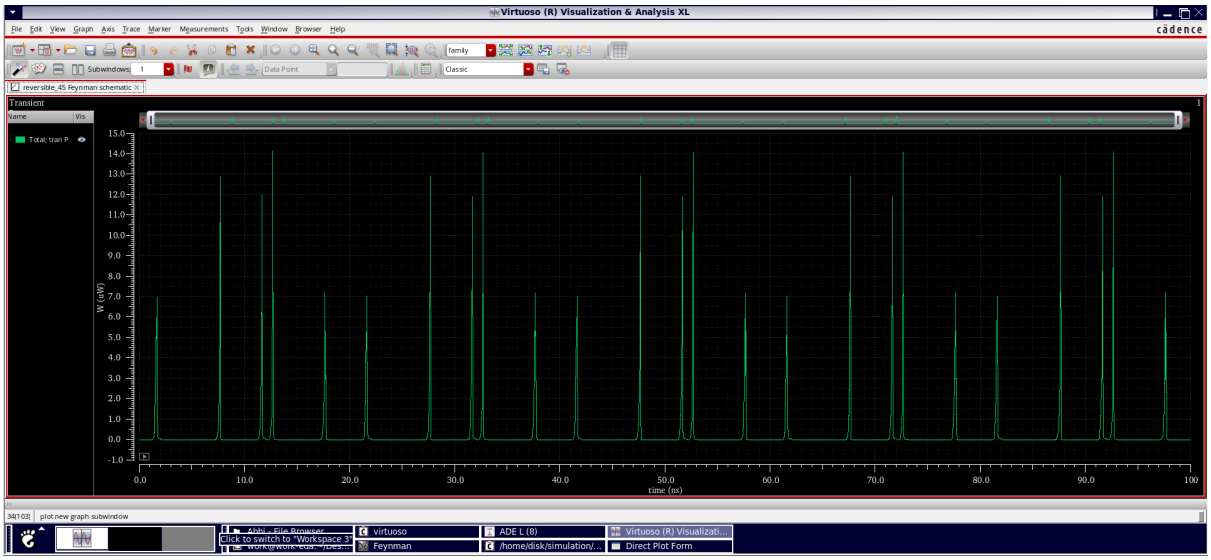
Power Dissipation:



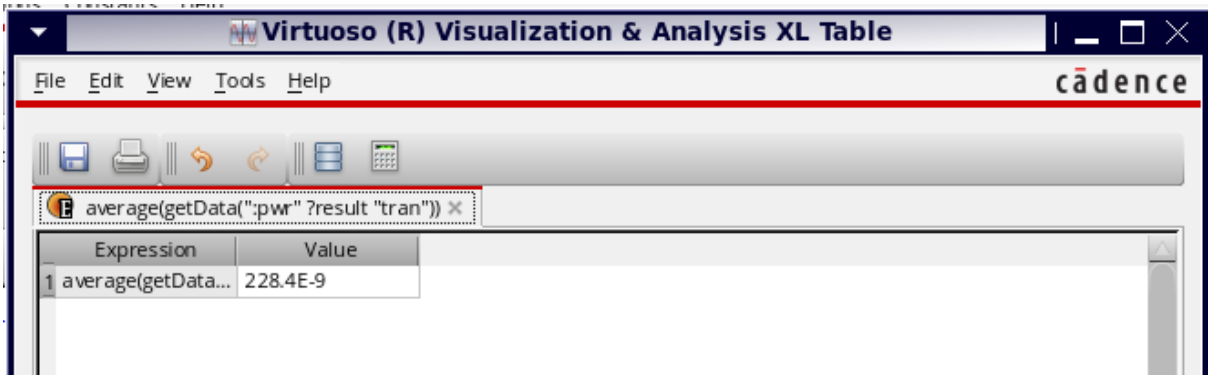
45nmtech:

Feynman gate:



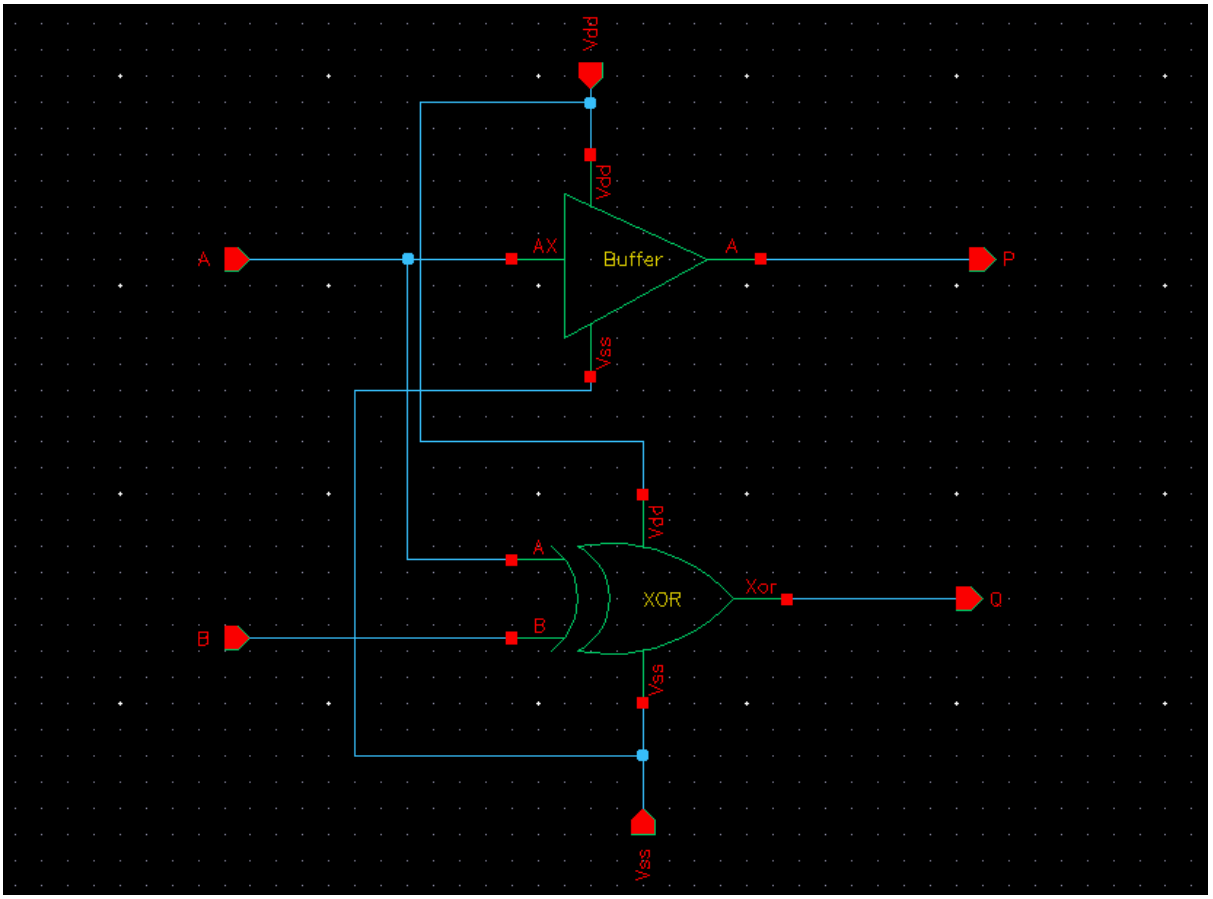


Power Dissipation:

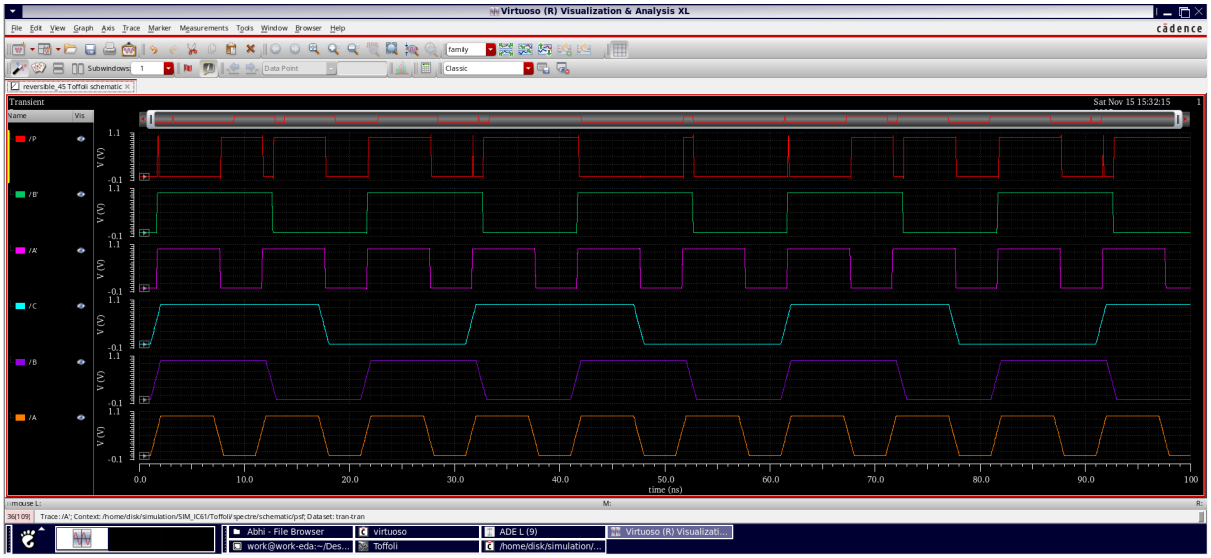


Delay:

Inputs	P	Q
A	0.125ns	7.536ns
B	4.966ns	5.037ns



Toffoli Gate:


Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Sat Nov 15 15:32:15
/P
/B'
/A'
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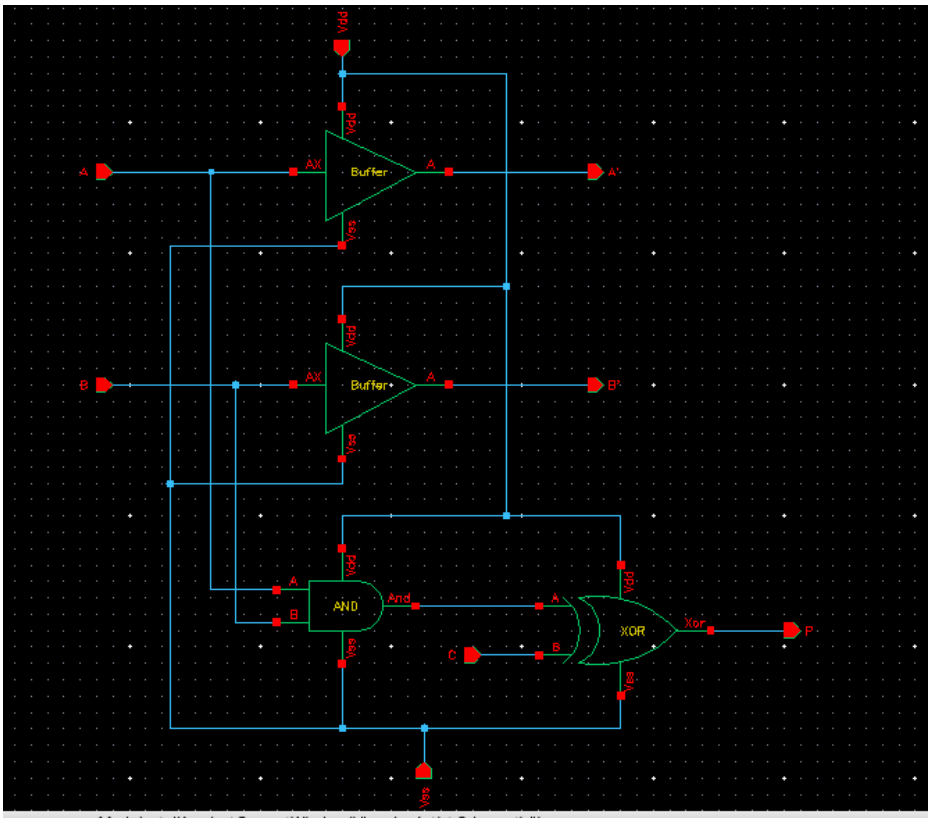
Vdd
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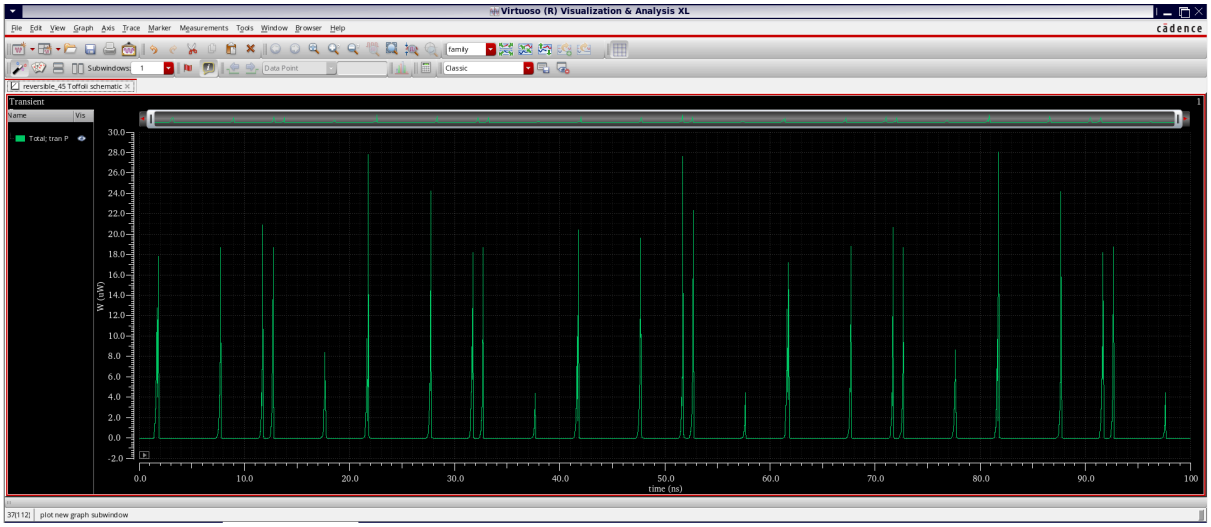
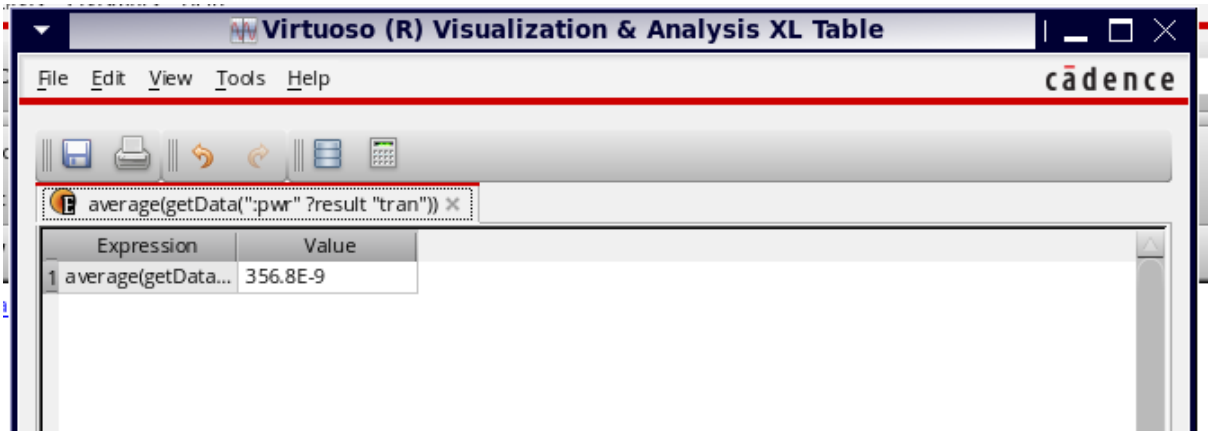


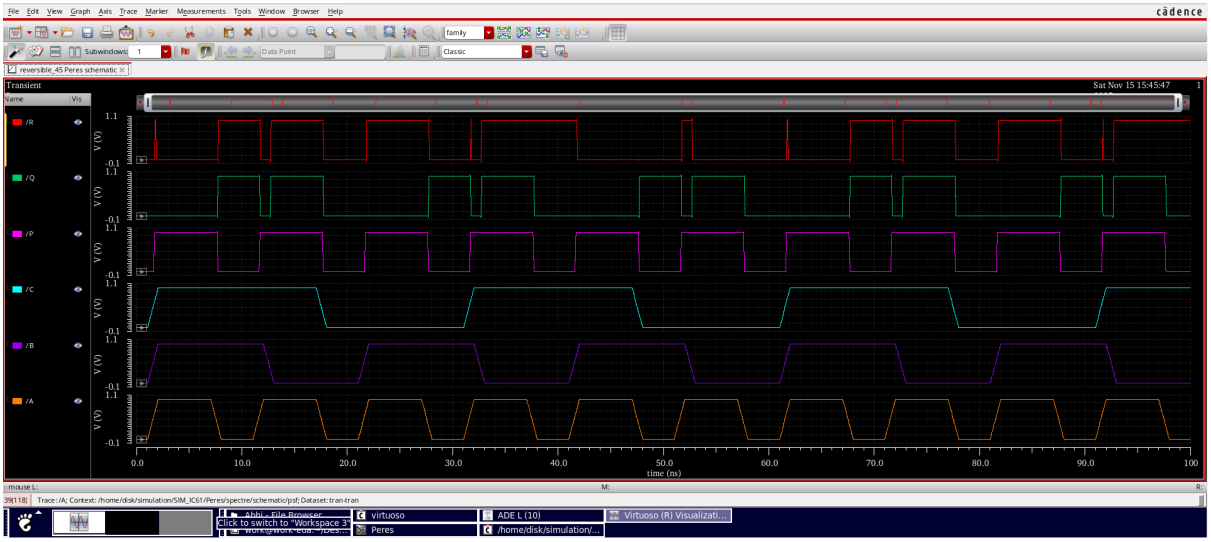
Delay:

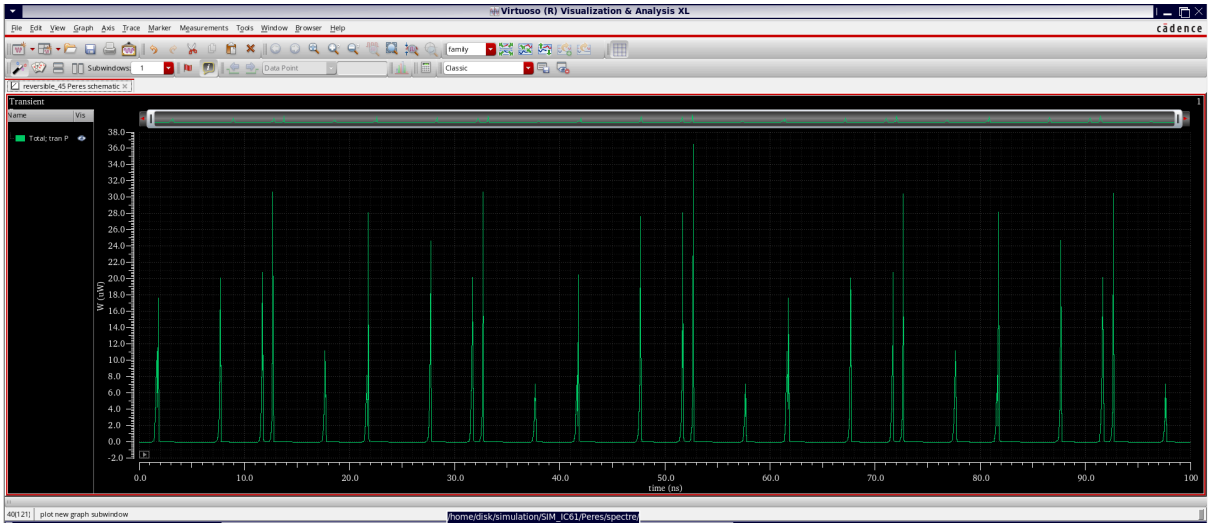
Inputs	A’	B’	P
A	0.0125ns	2.5105ns	2.456ns
B	2.487ns	0.0105ns	4.948ns
C	4.988ns	2.49ns	7.446ns

Power Dissipation:



Peres Gate:





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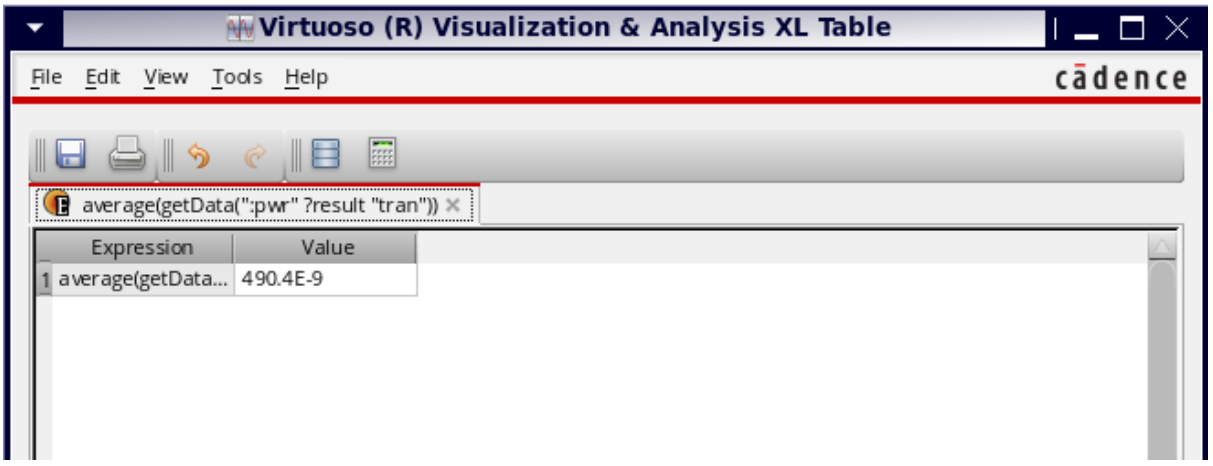
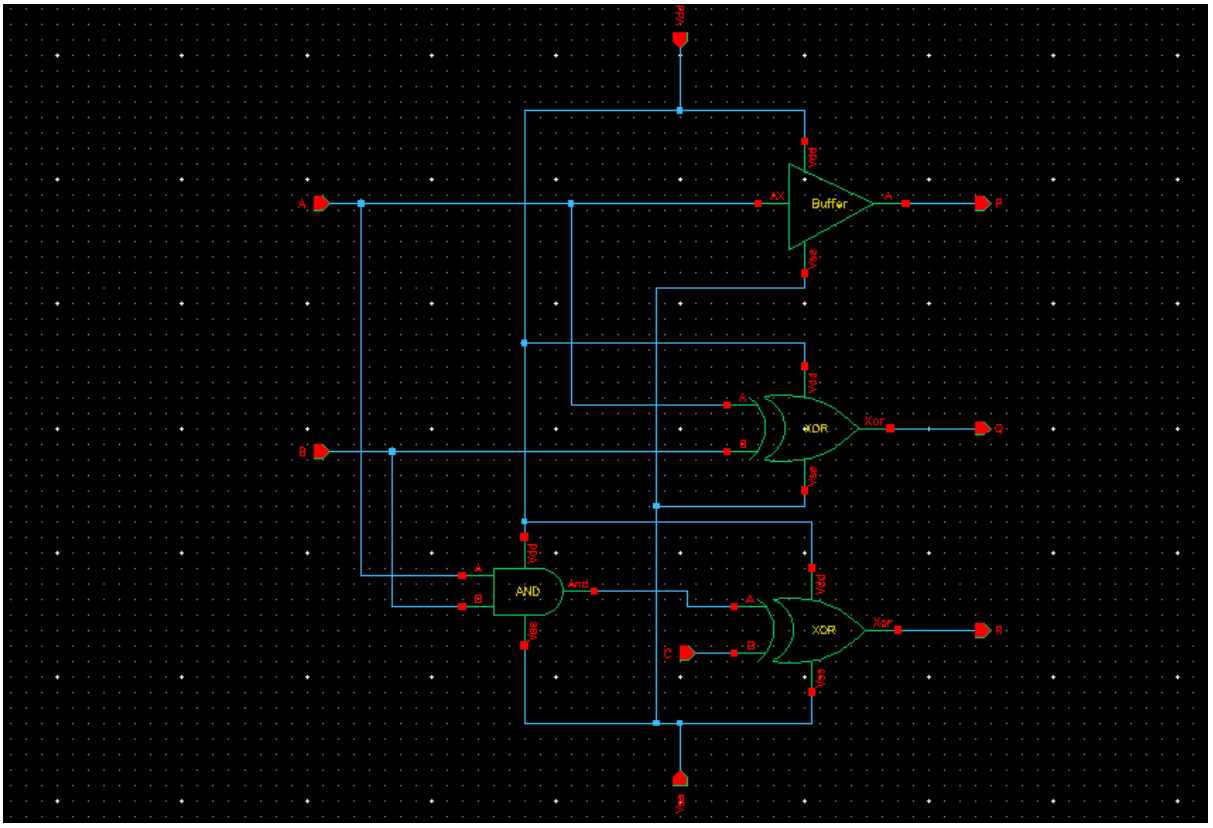
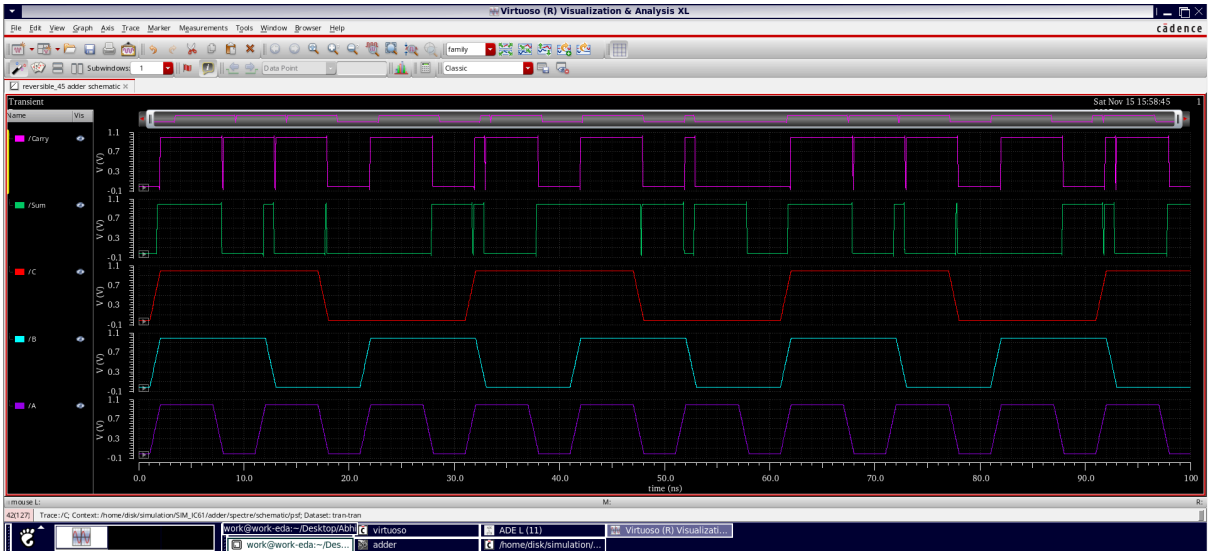


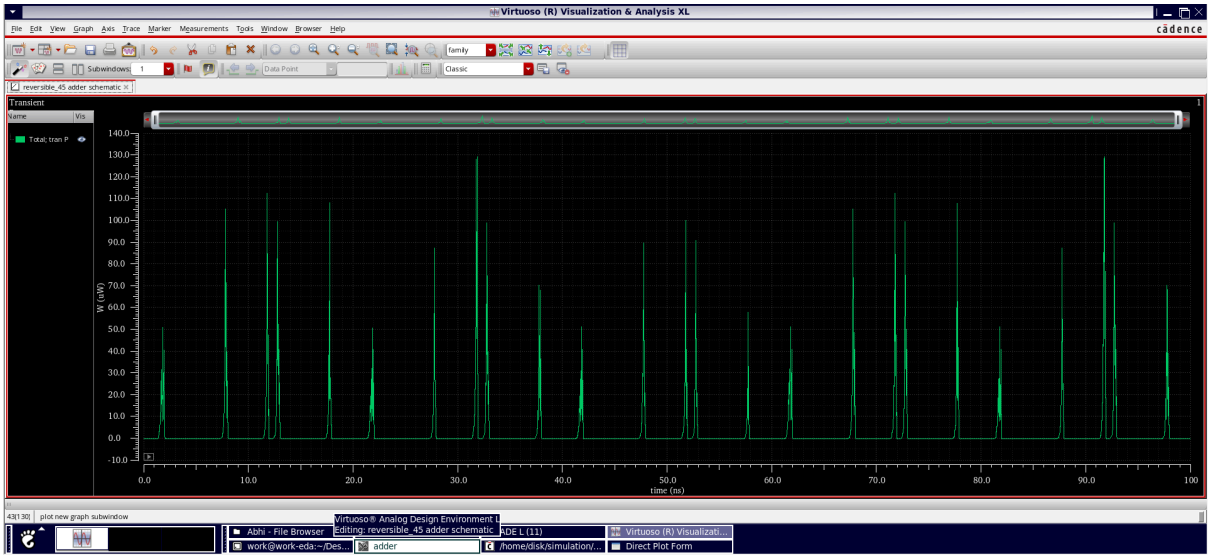


Delay:

Inputs	P	Q	R
A	0.0125ns	7.53ns	2.44ns
B	2.4875ns	5.037ns	4.948ns
C	4.988ns	2.537ns	7.446ns

Adder_45nm:





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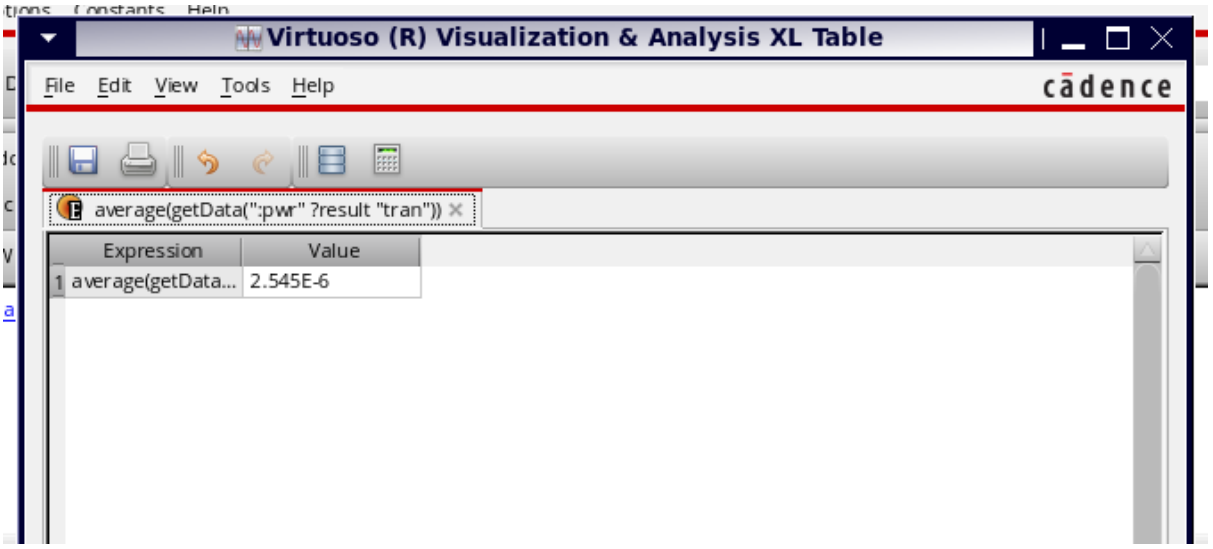
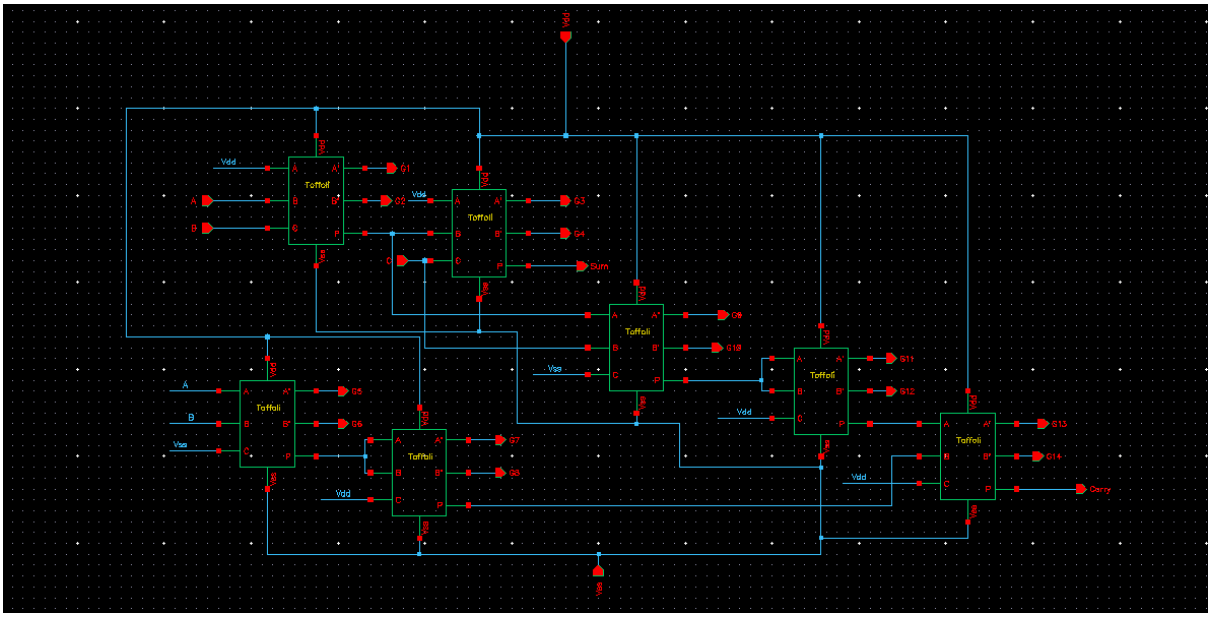
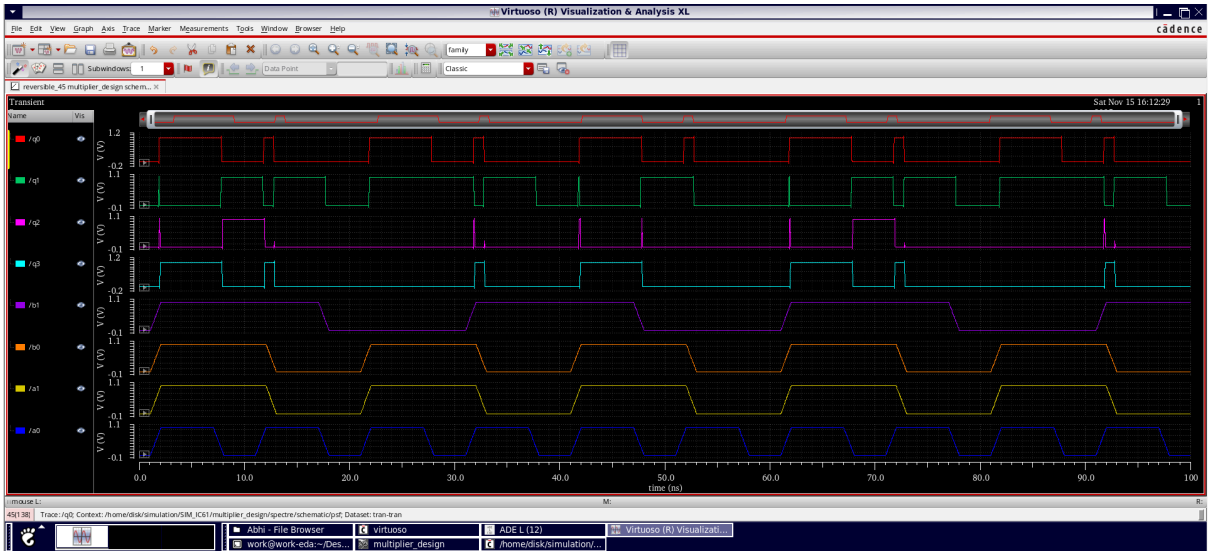


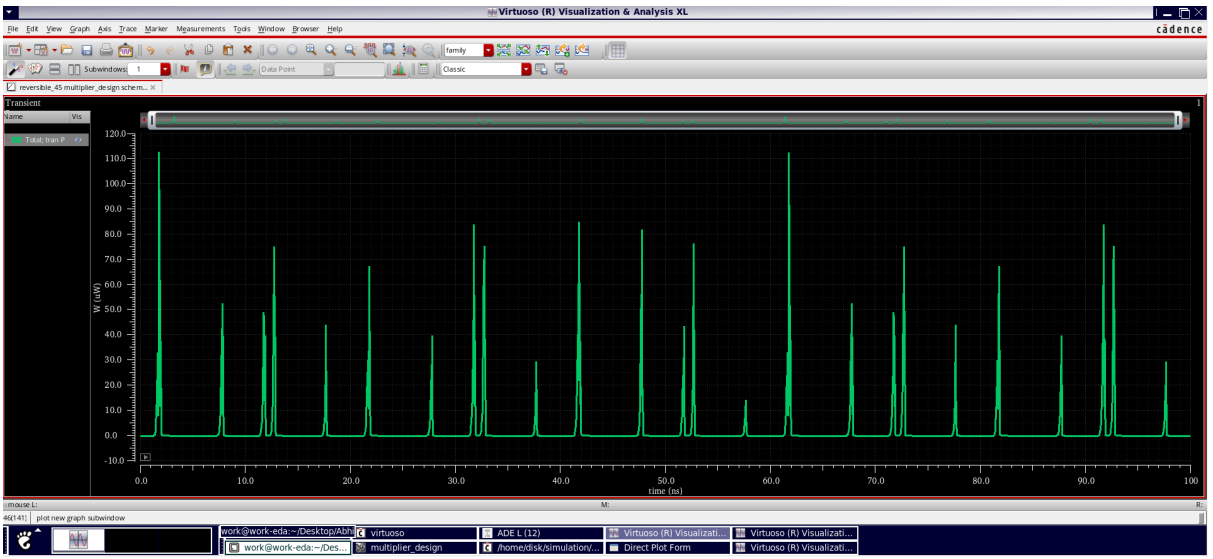
Delay:

Inputs	Sum	Carry
A	0.0925ns	0.229ns
B	2.4075ns	2.271ns
C	4.906ns	4.772ns

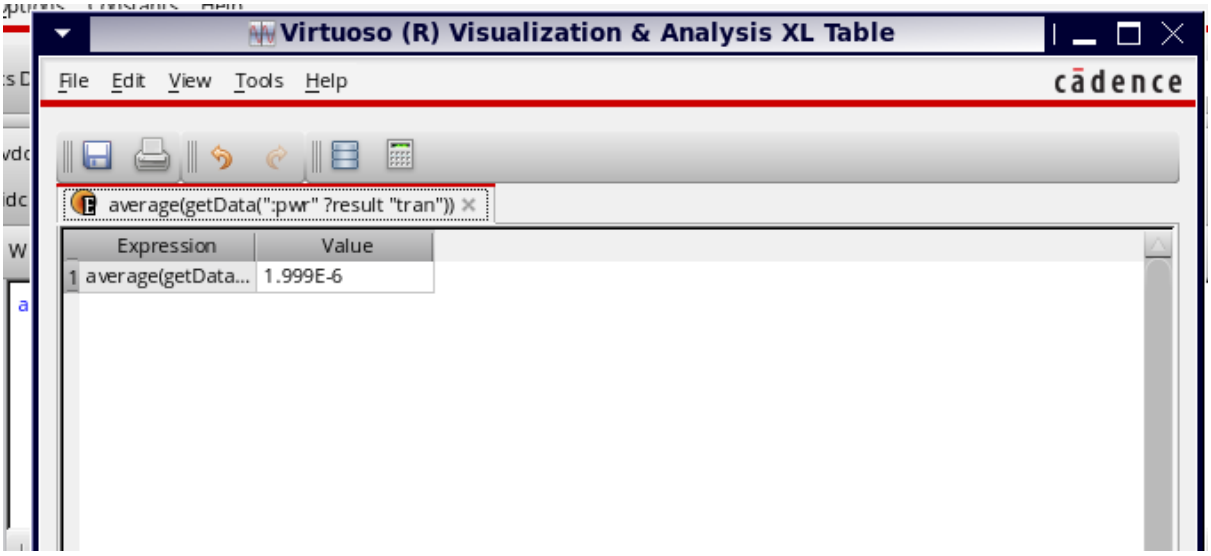


Multiplier_45nm:



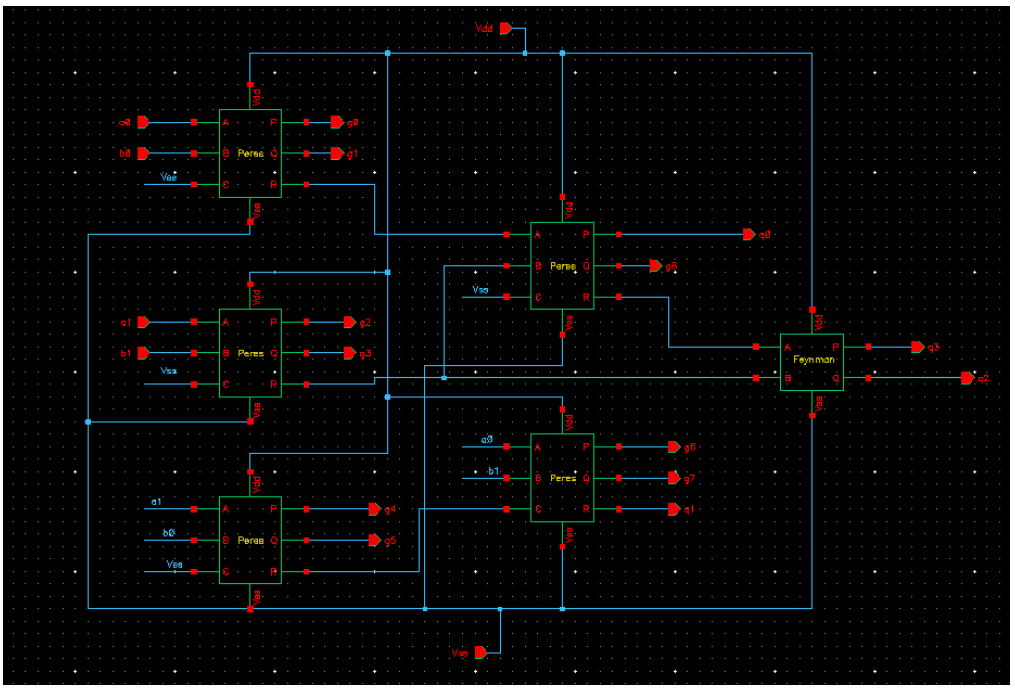


Power Dissipation:



Delay:

Inputs	q0	q1	q2	q3
a0	0.097ns	4.807ns	4.653ns	0.1851ns
b0	4.9035ns	7.4019ns	7.328ns	4.8205ns
a1	2.448ns	4.9019ns	4.826ns	2.3185ns
b1	7.4039ns	9.901ns	9.828ns	7.3205ns



8. Challenges:

1. Minimizing garbage outputs and constant inputs while keeping circuit depth low.

2. Designing reversible multiplier with optimized quantum cost.

3. Ensuring signal copying without violating reversibility constraints.

4. Deriving power–delay trade-off in a reversible logic framework.

9. Future Work:

- Design more complex arithmetic units such as **Reversible ALU, DCT units, and dividers**.

- Optimization of reversible circuits based on quantum cost, garbage count, and delay.

- Implementation of sequential reversible systems such as reversible flip-flops and registers.

- Exploration toward quantum computing and nanotechnology platforms.

10. Conclusion:

The project successfully demonstrates the design and analysis of reversible arithmetic circuits. Functional reversible gates, full adder, and multiplier were developed and simulated. Analysis of **power, delay, and PDP** confirms that reversible logic has strong potential for low-power and high-performance computing. The achieved results validate reversible logic as a promising alternative to irreversible CMOS architectures and highlight its role in future computational systems.

10. References:

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