Institute of Engineering and Technology (IET) JK Lakshmipat University, Jaipur

Design & Analysis of Arithmetic Circuit from Reversible Logic Gates:

Faculty Guide:
Dr. Gaurav Mani Khanal

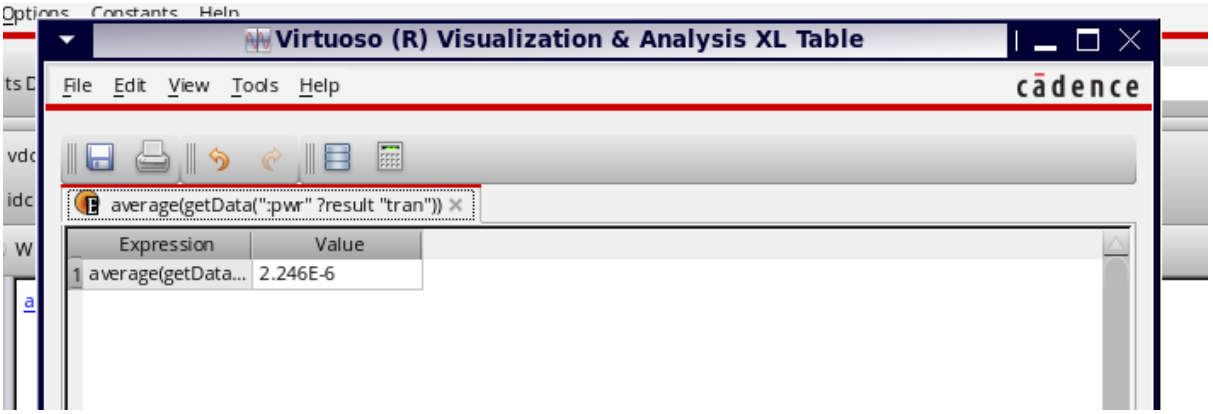
Student:
Abhimanyu sharma (2022Btech003)

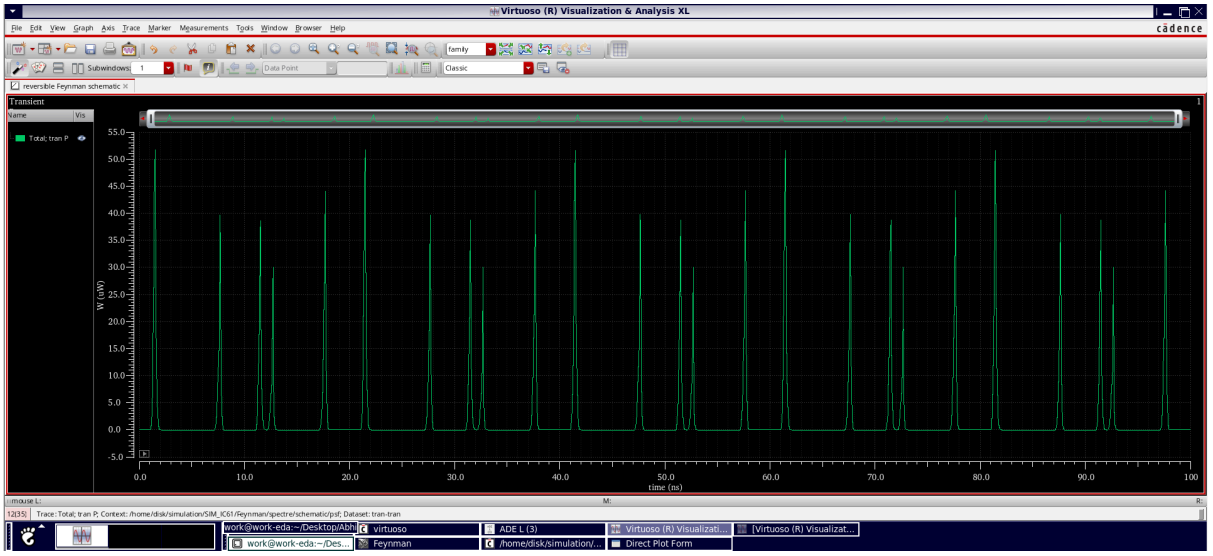
Submitted To:
Dr. Gaurav Raj

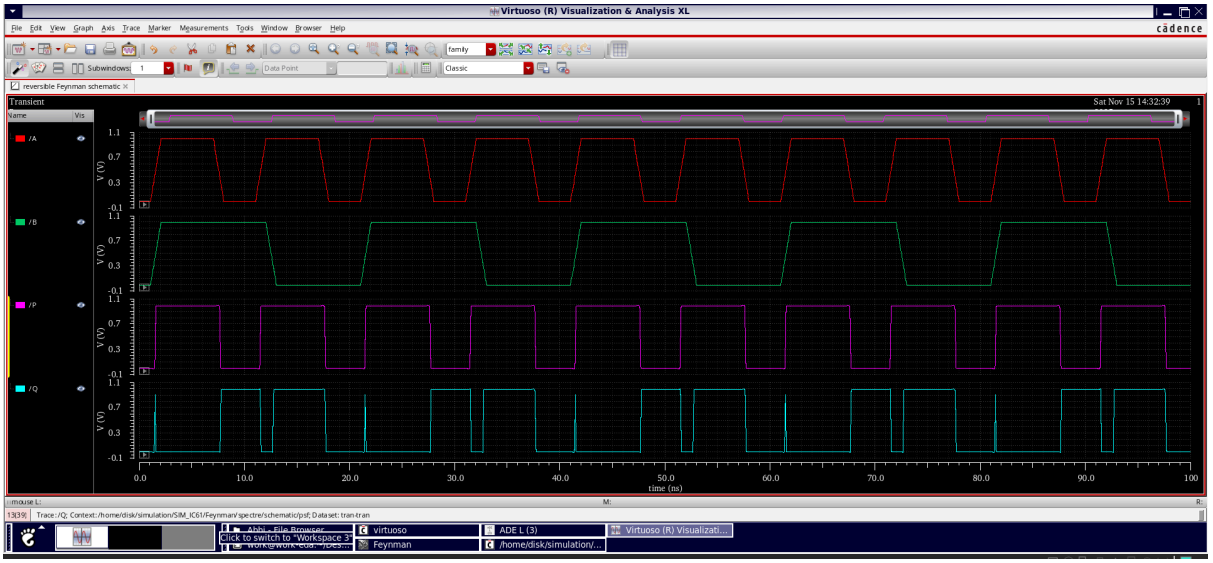
Work:

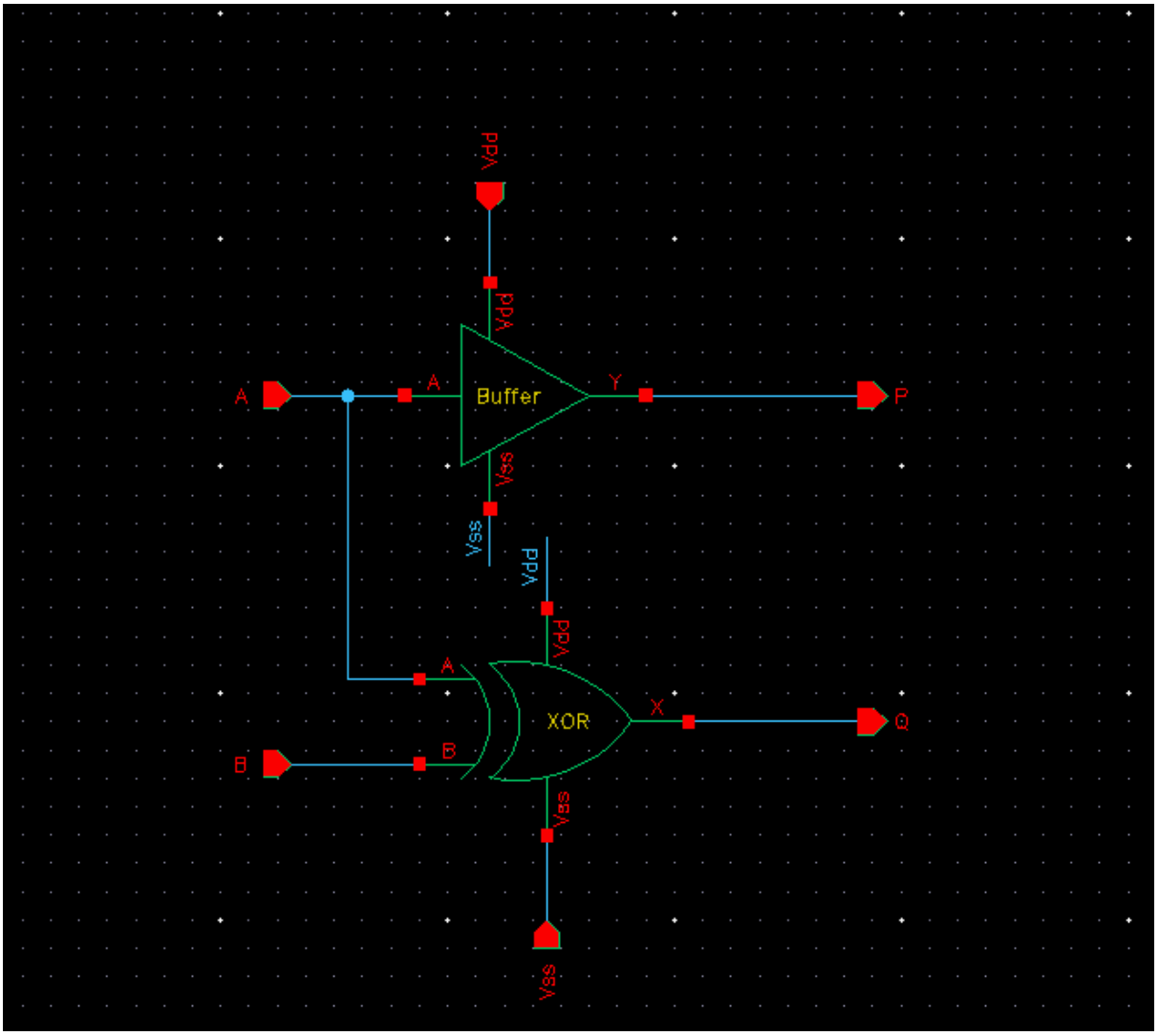
This work was carried out during the midterm.

Feynman gate:

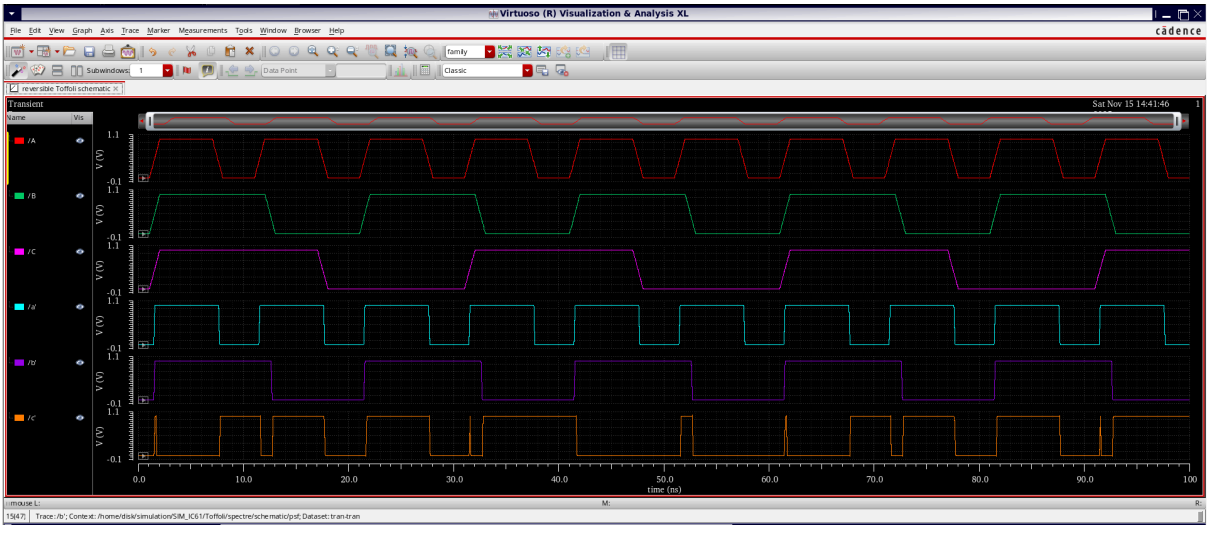


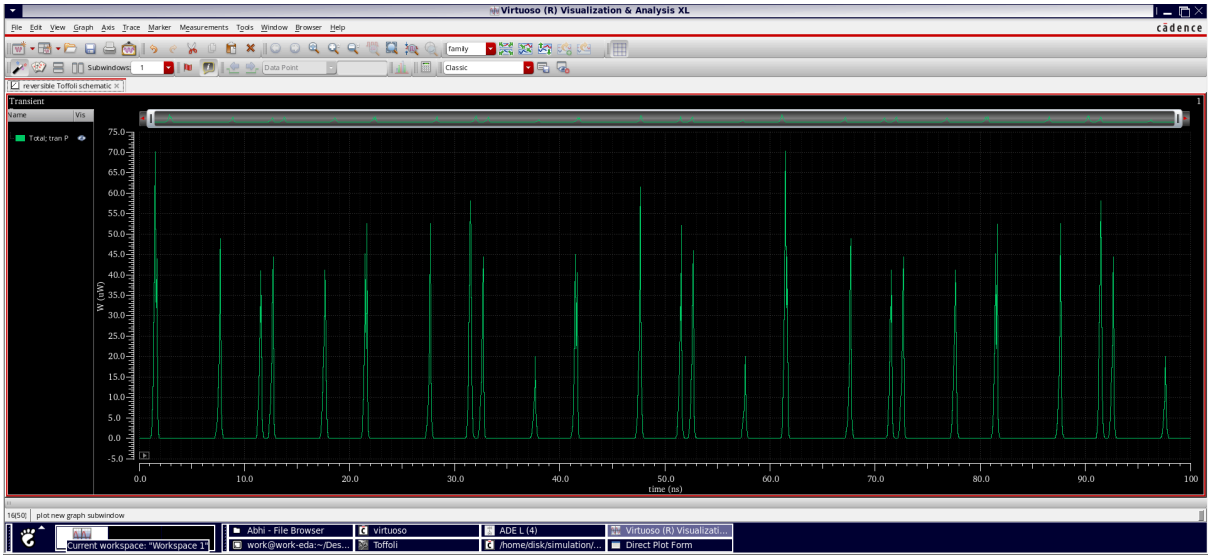

Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Total: tran P
W (uW)
time (ns)
Trace: Total; tran P; Context: /home/disk/simulation/SIM_IC61/Feynman/spectre/schematic/psf; Dataset: tran-tran
work@work-eda:~/Desktop/Abhi
virtuoso
ADE L (3)
Virtuoso (R) Visualizati...
Feynman
/home/disk/simulation/...
Direct Plot Form

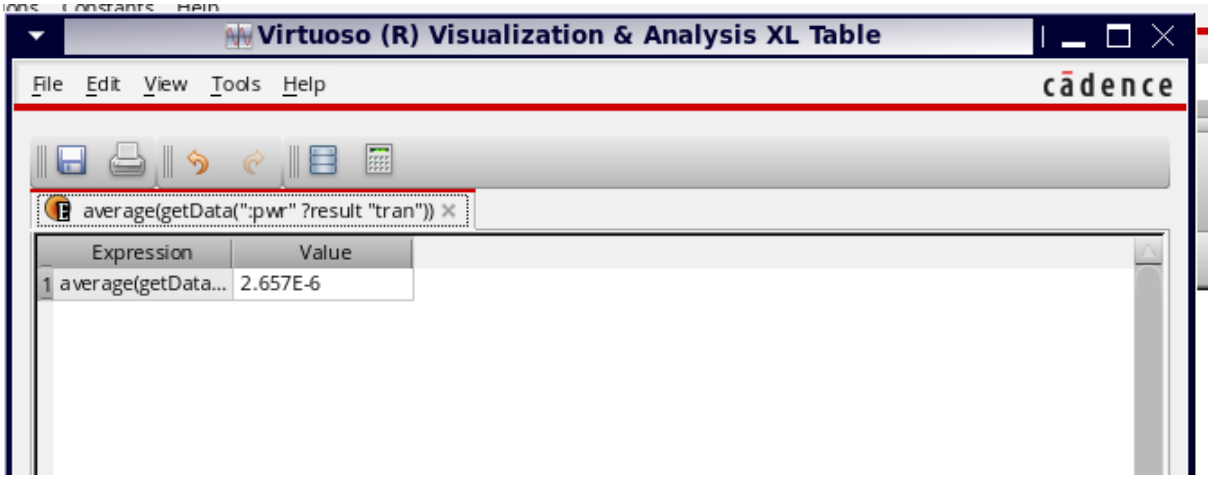

Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Sat Nov 15 14:32:39
/A
/B
/P
/Q
V (V)
time (ns)
Trace: /Q; Context: /home/disk/simulation/SIM_IC61/Feynman/spectre/schematic/psf; Dataset: tran-tran
Click to switch to "Workspace 3"
virtuoso
ADE L (3)
Feynman
/home/disk/simulation/...



Toffoli Gate:




Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient
Total: tran P
W (uW)
time (ns)
current workspace: "Workspace 1"
Abhi - File Browser
virtuoso
ADE L (4)
Virtuoso (R) Visualizati...
work@work-eda:~/Des...
Toffoli
/home/disk/simulation/...
Direct Plot Form


Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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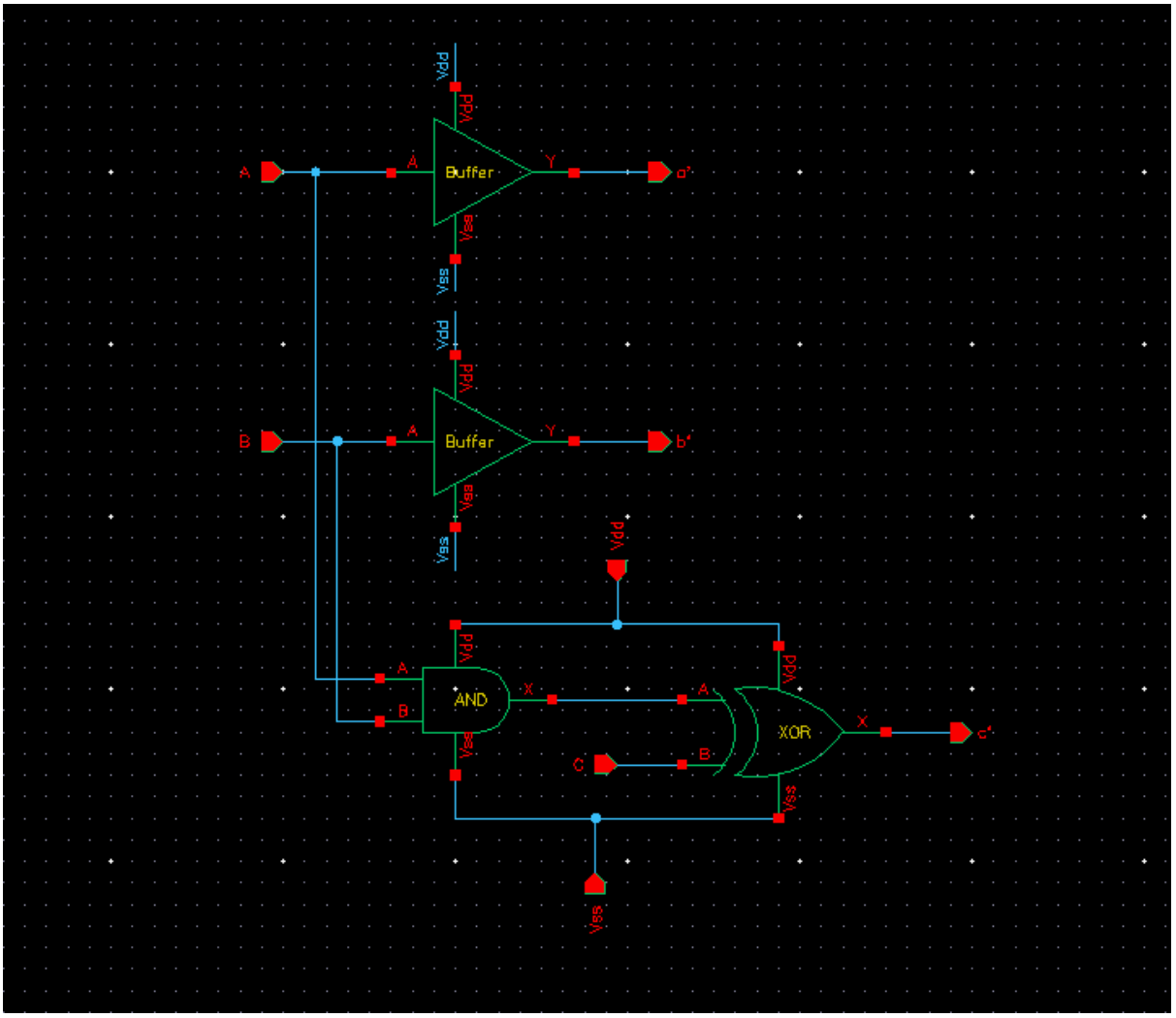
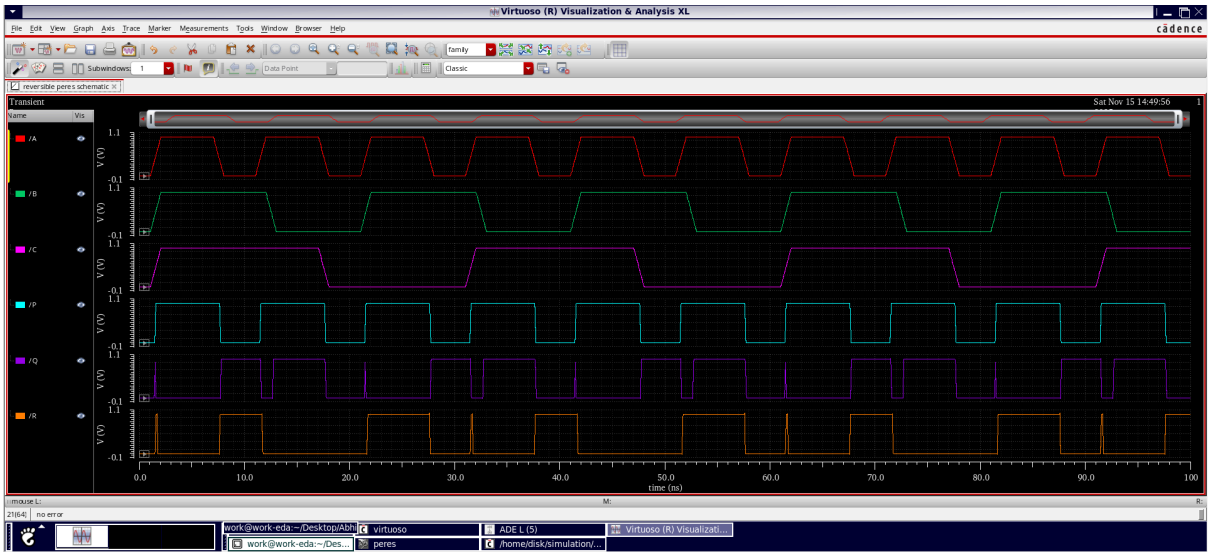
Expression
Value
1
average(getData...
2.657E-6


Vdd
Vdd
A
A
Buffer
Y
a'
Vss
Vss
Vdd
Vdd
B
A
Buffer
Y
b'
Vss
Vss
Vdd
Vdd
A
AND
X
A
Vdd
B
Vss
XOR
X
c'
C
B
Vss
Vss

Peres gate:


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
reversible peres schematic
Transient
Sat Nov 15 14:49:56
/A
/B
/C
/P
/Q
/R
V (V)
time (ns)
0.0
10.0
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40.0
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60.0
70.0
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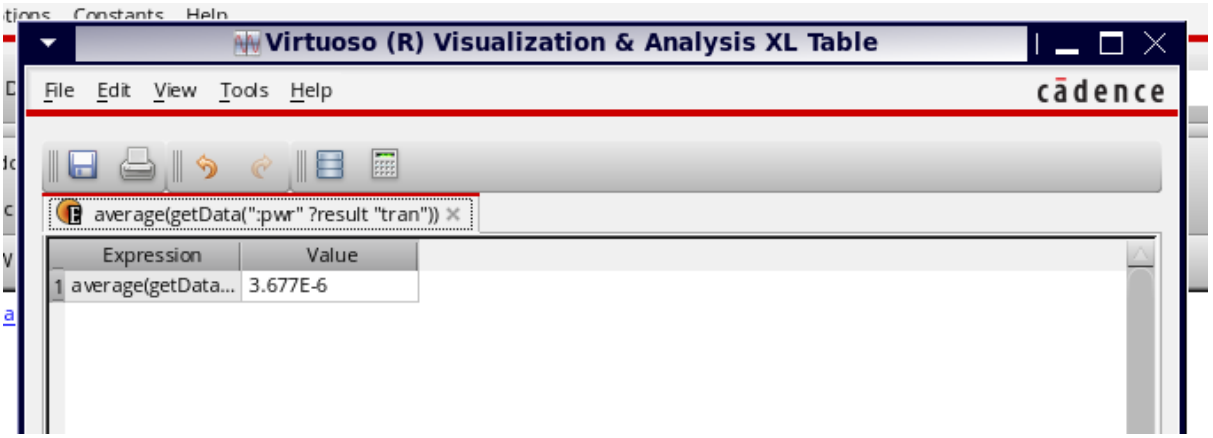
100
work@work-eda:~/Desktop/Abh
virtuoso
ADE L (5)
Virtuoso (R) Visualizati...
work@work-eda:~/Des...
peres
/home/disk/simulation/...


Virtuoso (R) Visualization & Analysis XL Table
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Expression
Value
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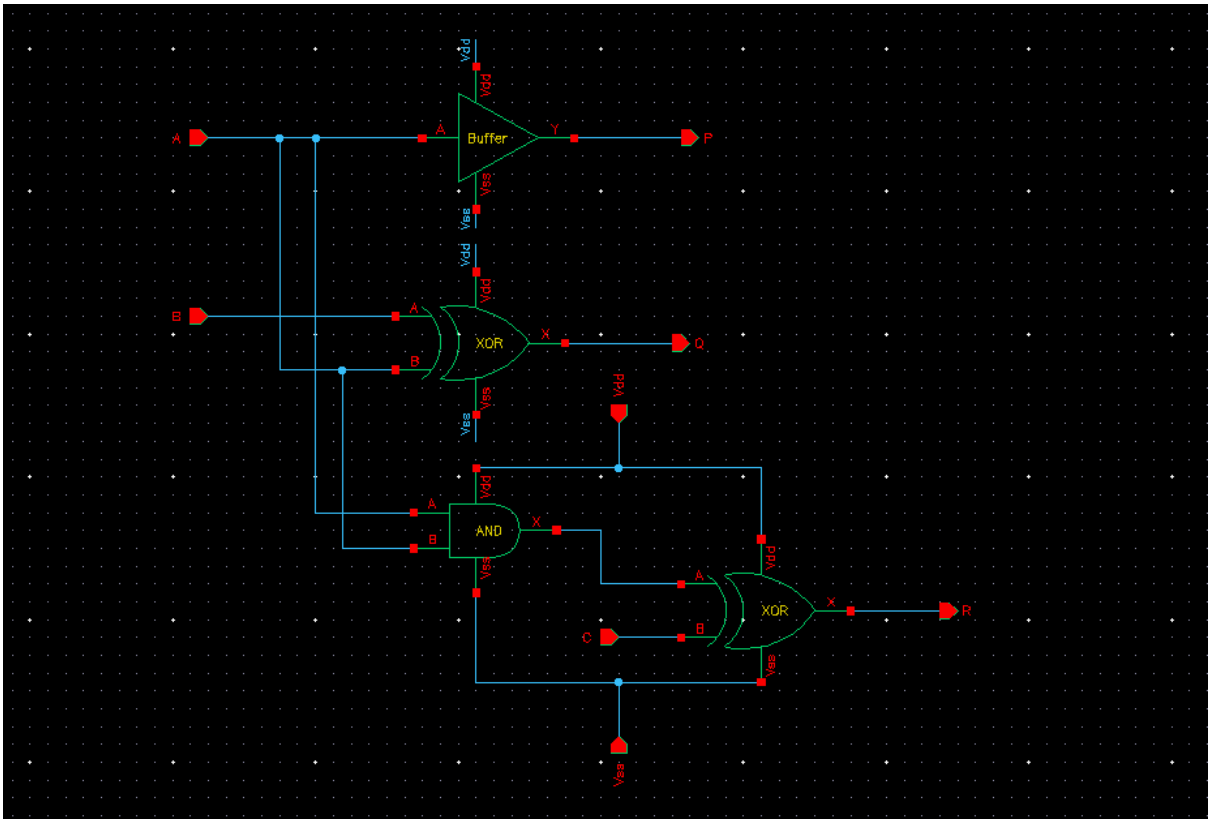
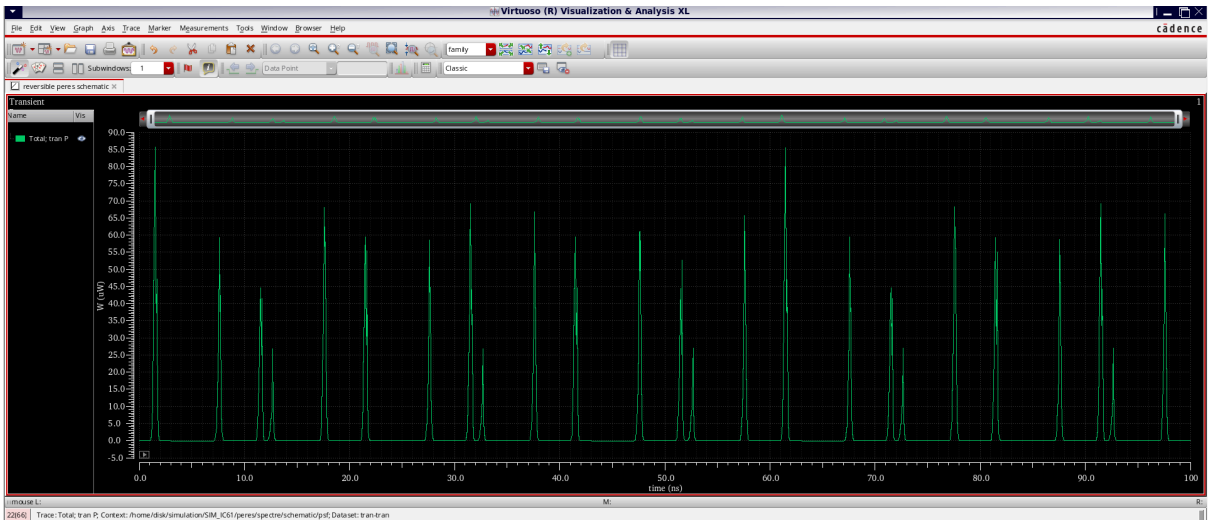
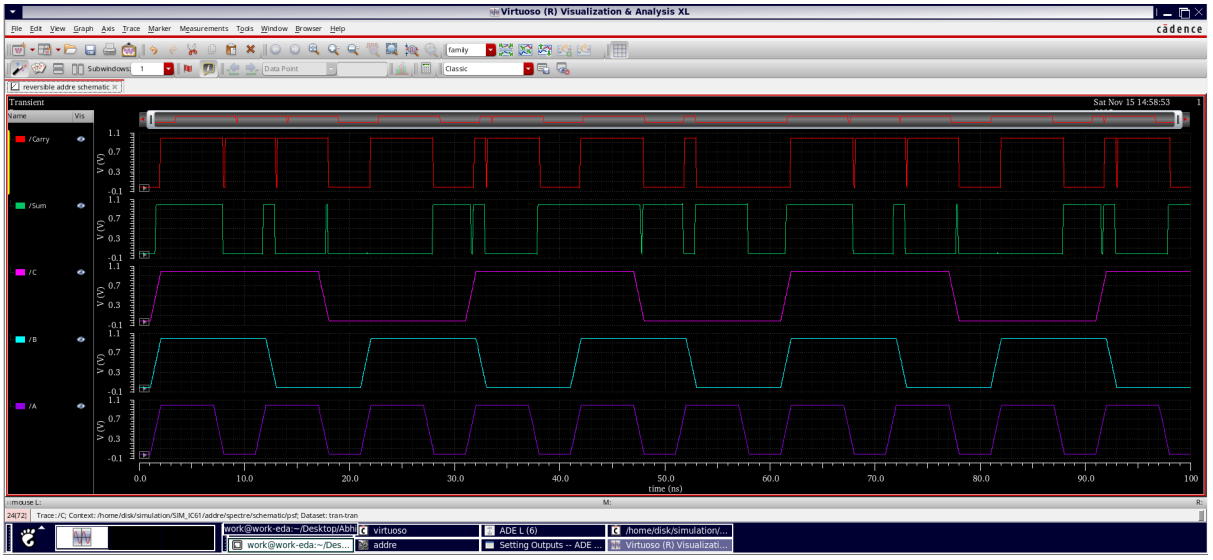
3.677E-6


Vdd
Vss
A
B
C
Buffer
XOR
AND
XOR
Y
X
X
P
Q
R


Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Total: tran P
W (uW)
time (ns)

Adder90nm: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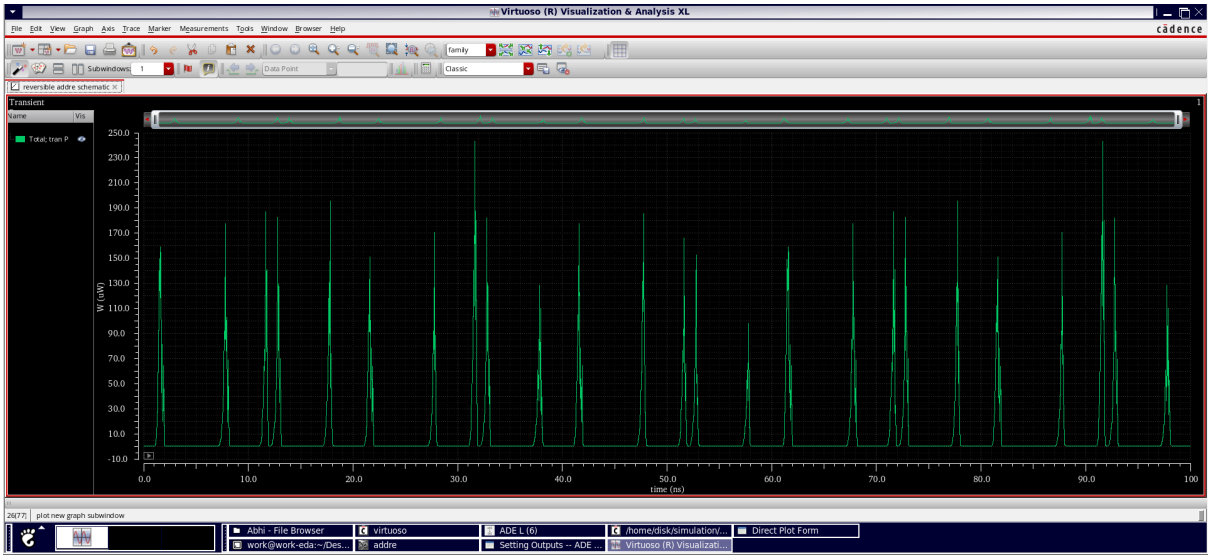
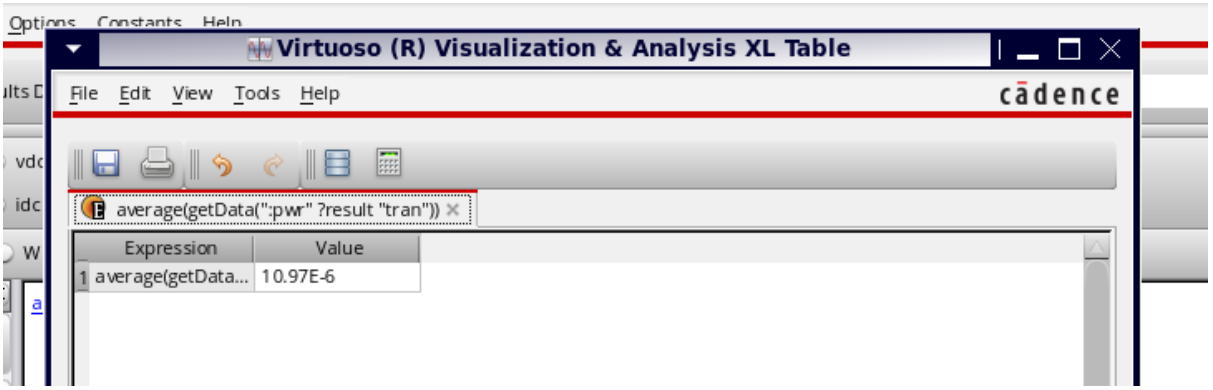
cadence
Transient
/Carry
/Sum
/C
/B
/A
V (V)
time (ns)


Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Total; tran P
W (nW)
time (ns)


Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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Expression
Value
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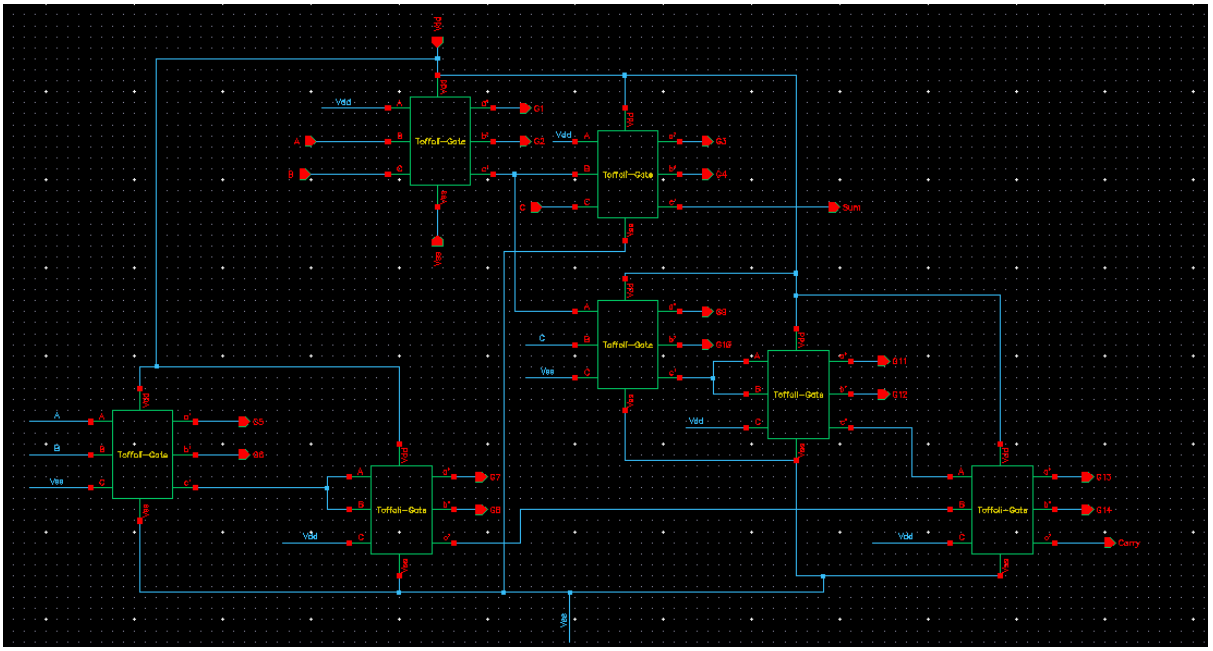
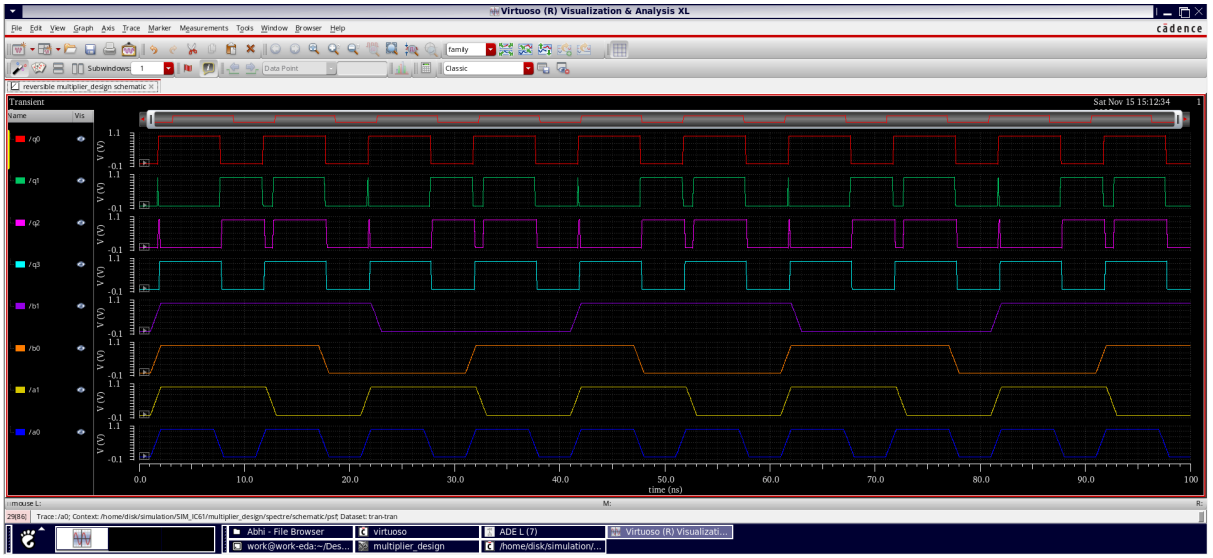
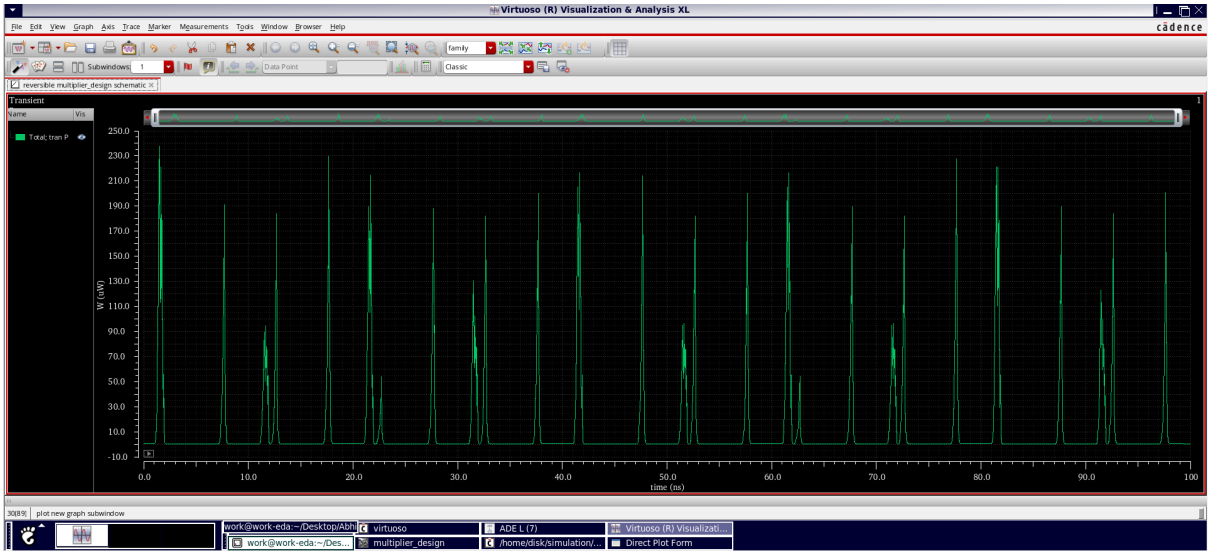
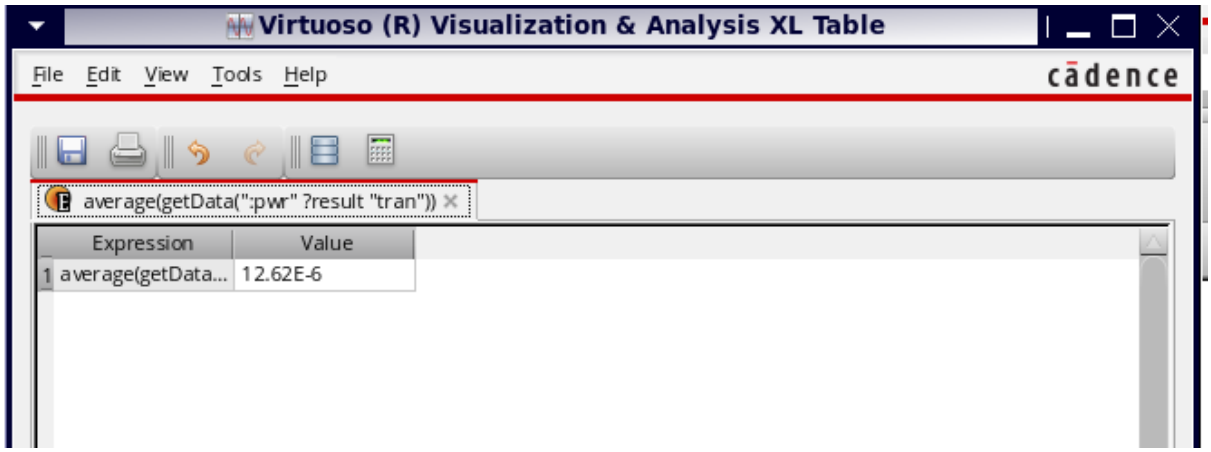
10.97E-6



Multiplier_90nm:




Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Total: tran P
W (uW)
time (ns)


Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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Value
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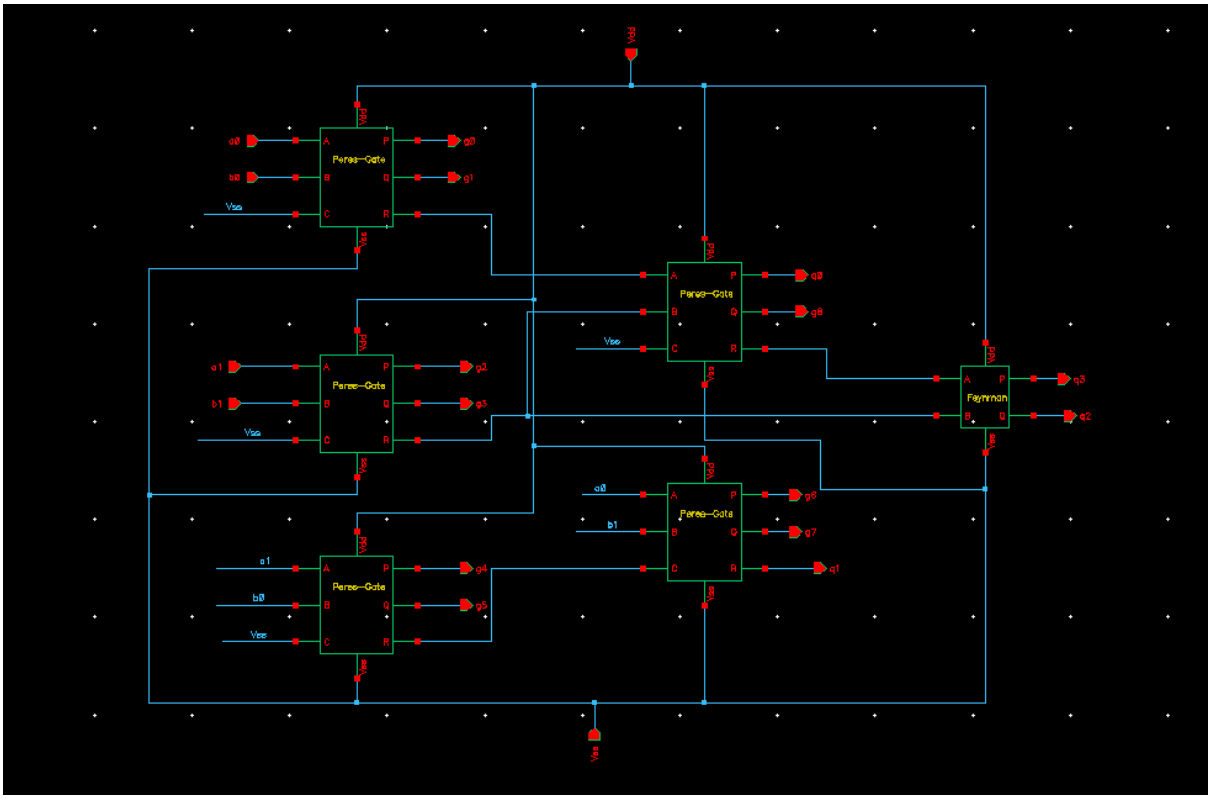
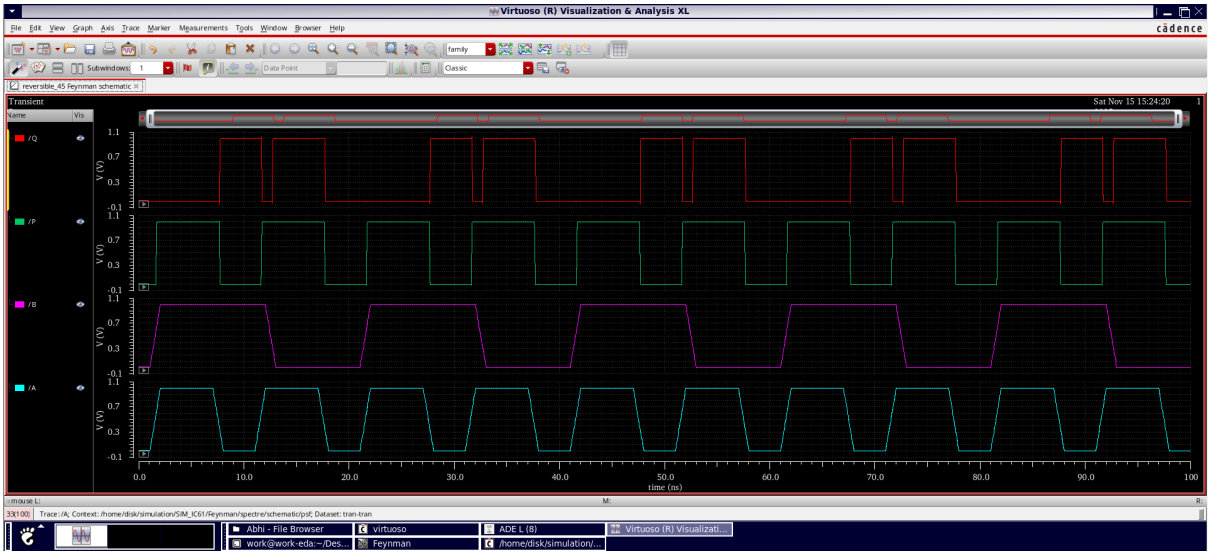
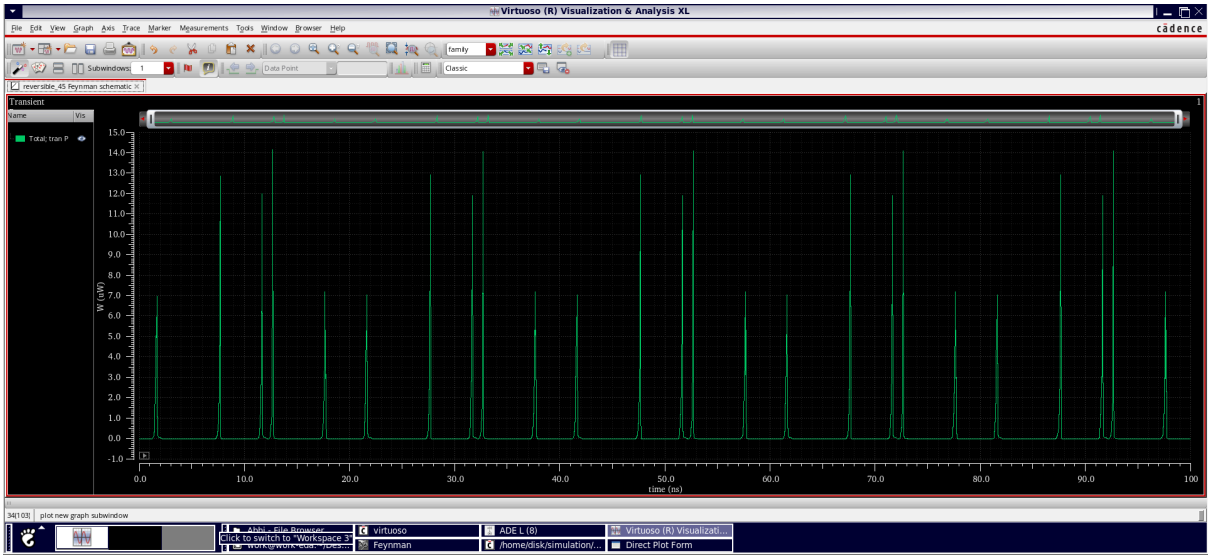
12.62E-6

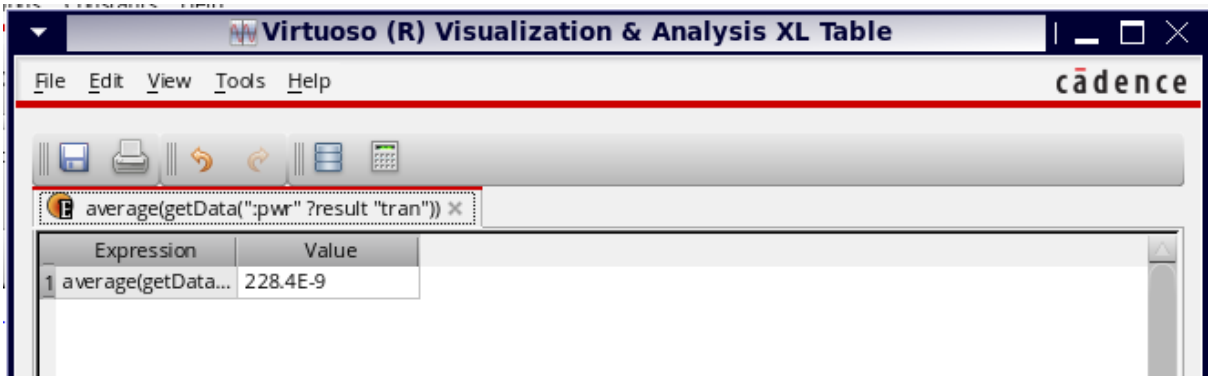

Vdd
Vss
Peres_Gate
Feynman

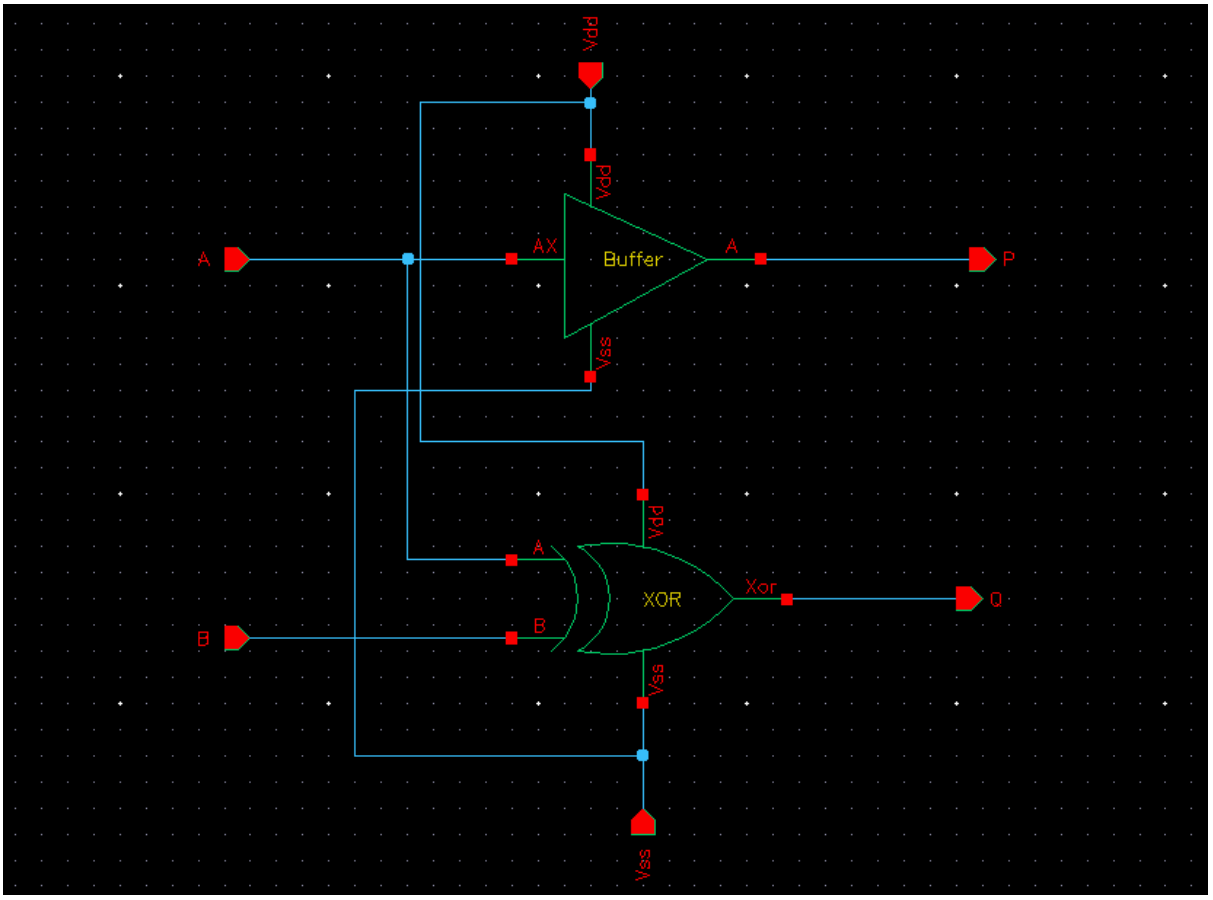
45nmtech:

Feynman gate:









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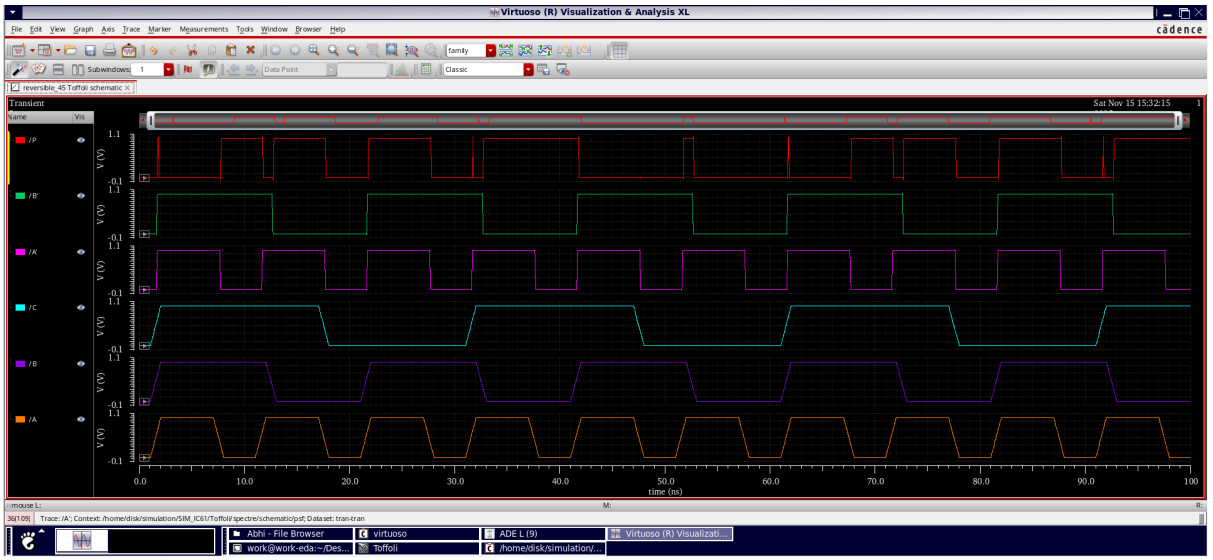

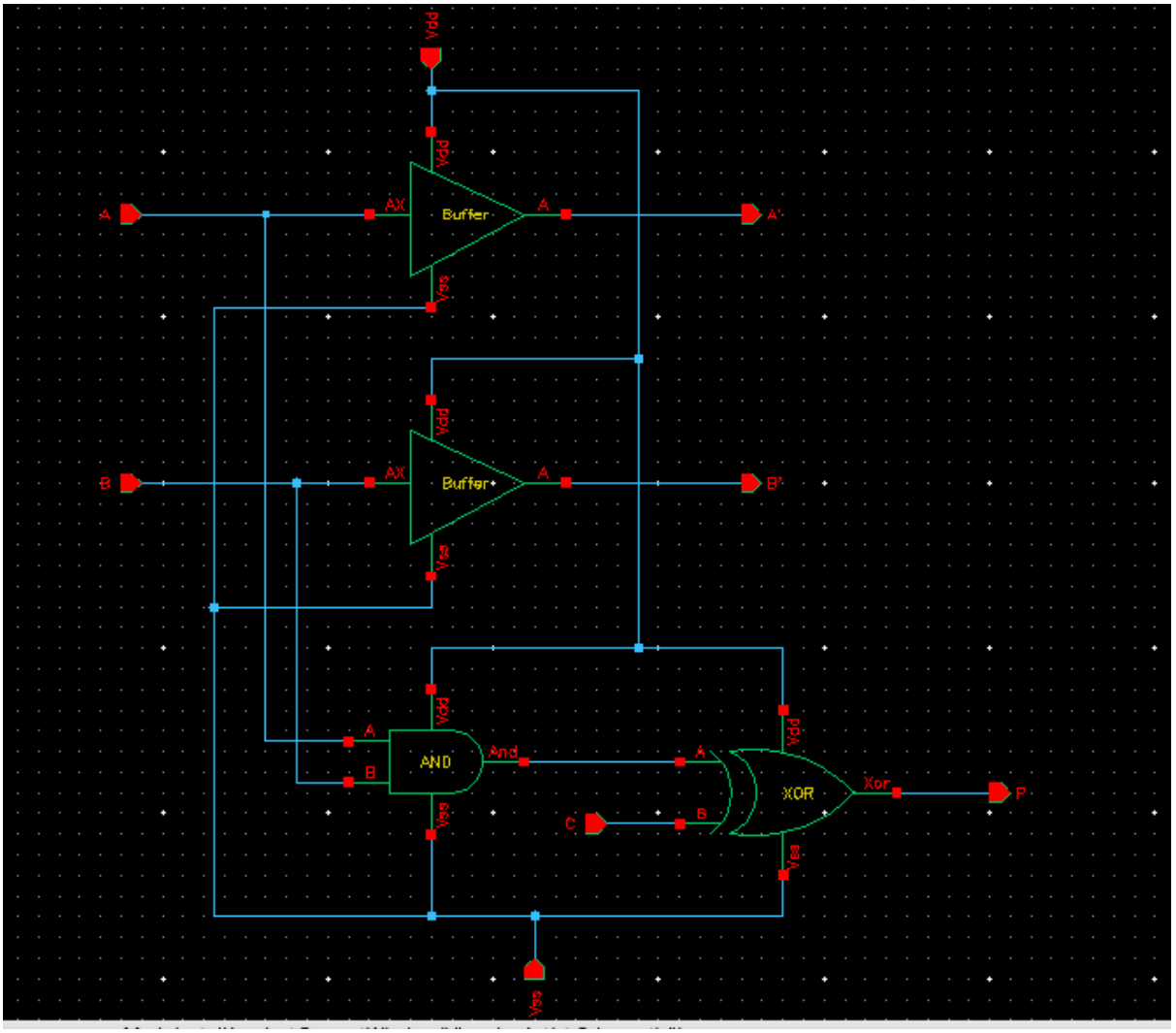
Vdd
Vdd
A
AX
Buffer
A
A'
Vss
Vdd
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AX
Buffer
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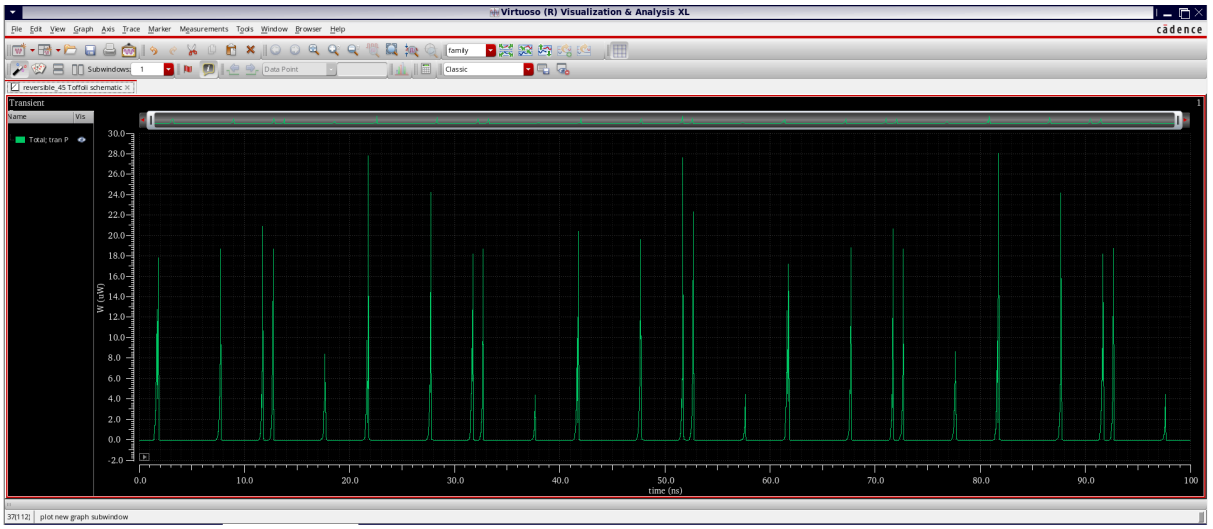
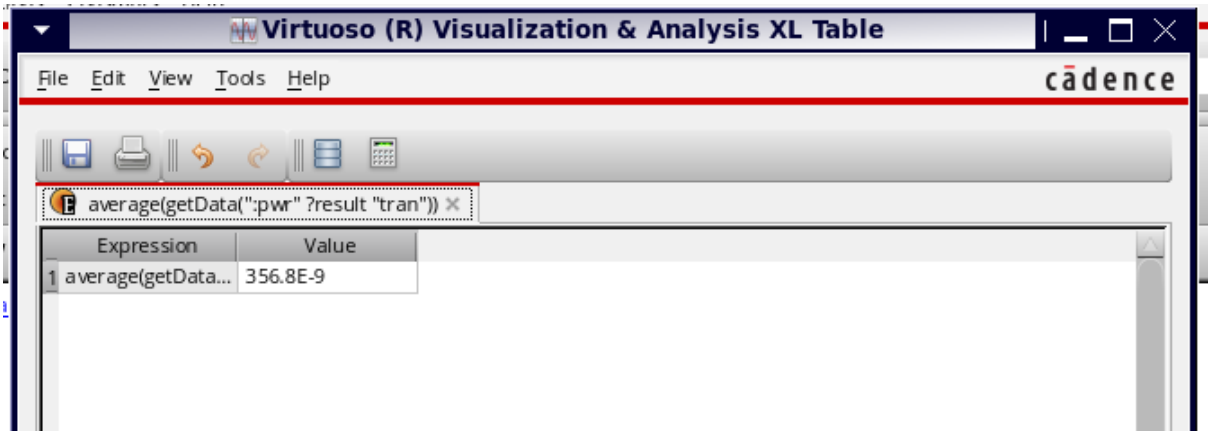
Vss


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
reversible_45 Toffoli schematic
Transient
Name
Vis
Total; tran P
W (nW)
time (ns)
plot new graph subwindow


Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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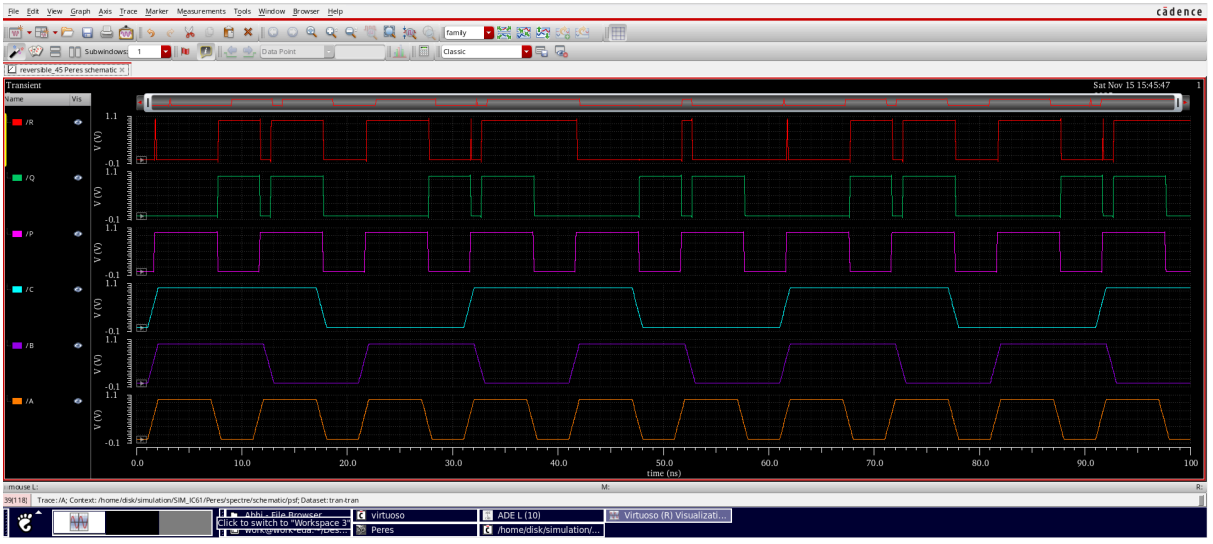
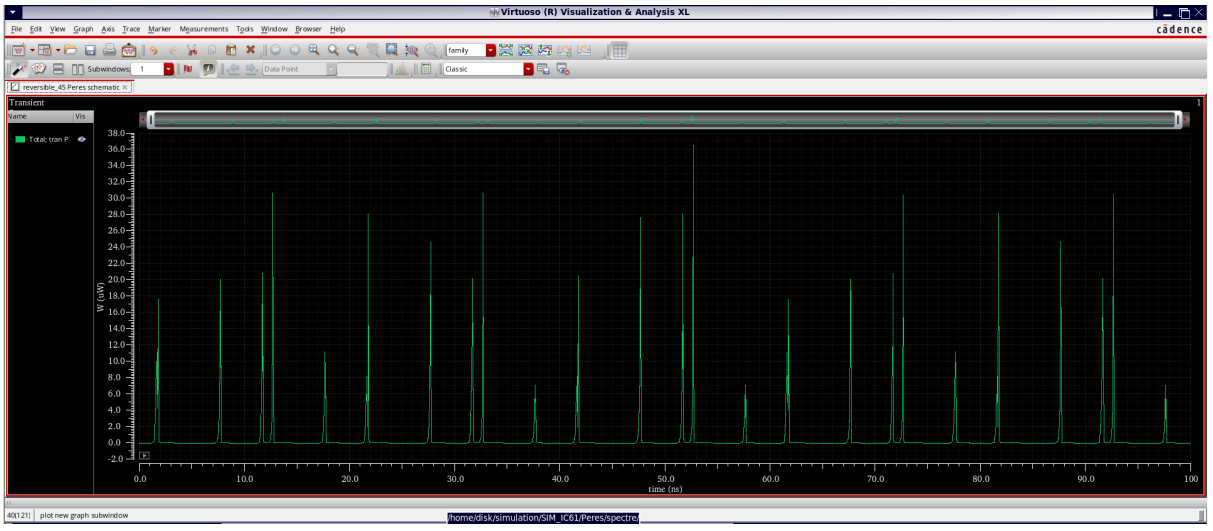
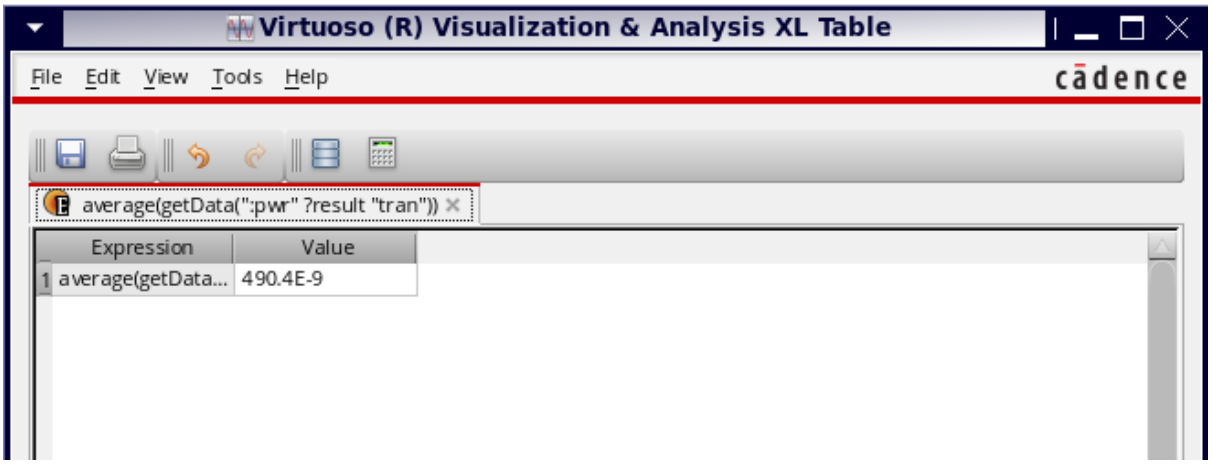
Expression
Value
1 average(getData...
356.8E-9

Peres Gate:


cadence
Transient
/R
/Q
/P
/C
/B
/A
V (V)
time (ns)


Virtuoso (R) Visualization & Analysis XL
cadence
Transient
Total; tran P
W (uW)
time (ns)


Virtuoso (R) Visualization & Analysis XL Table
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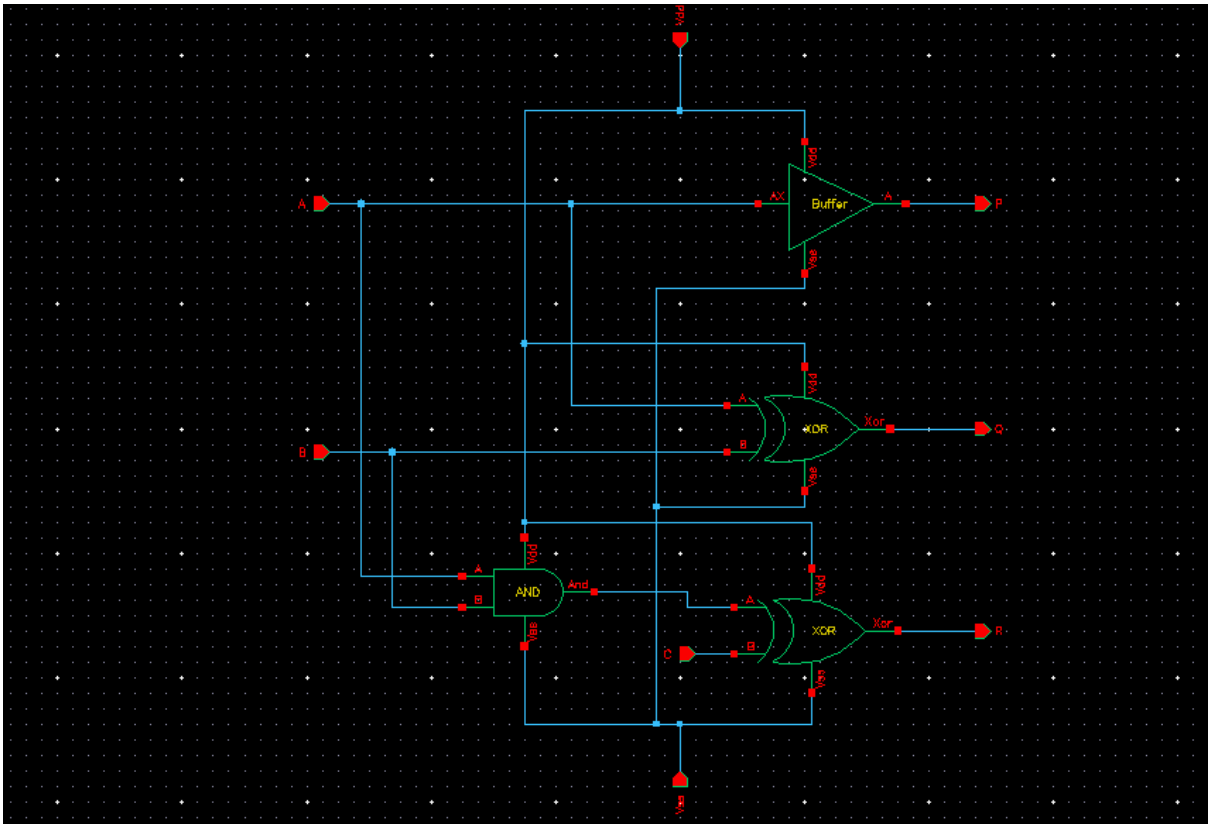
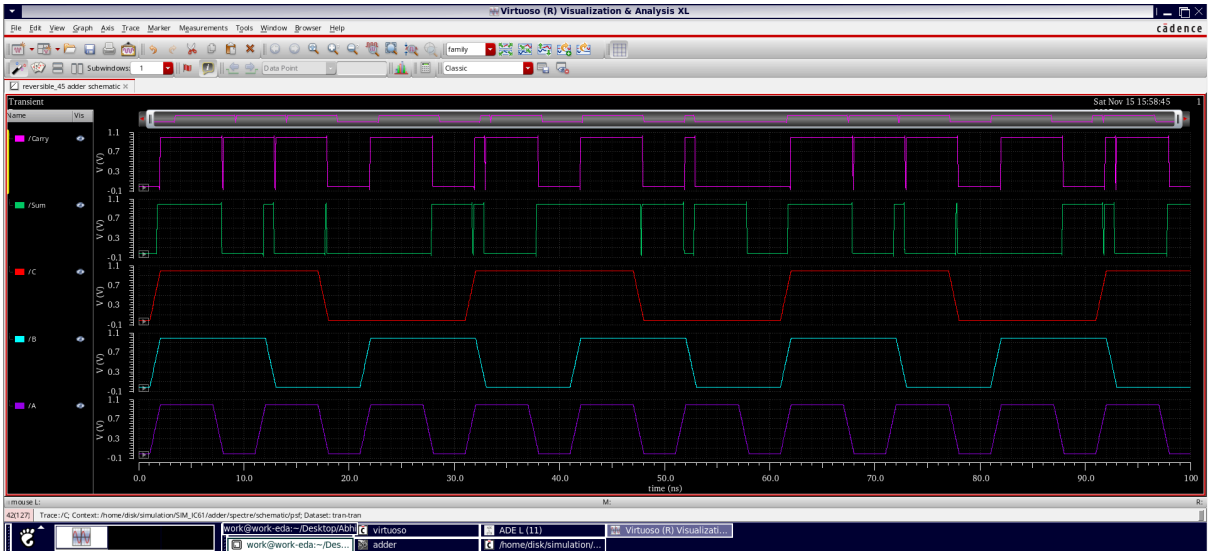
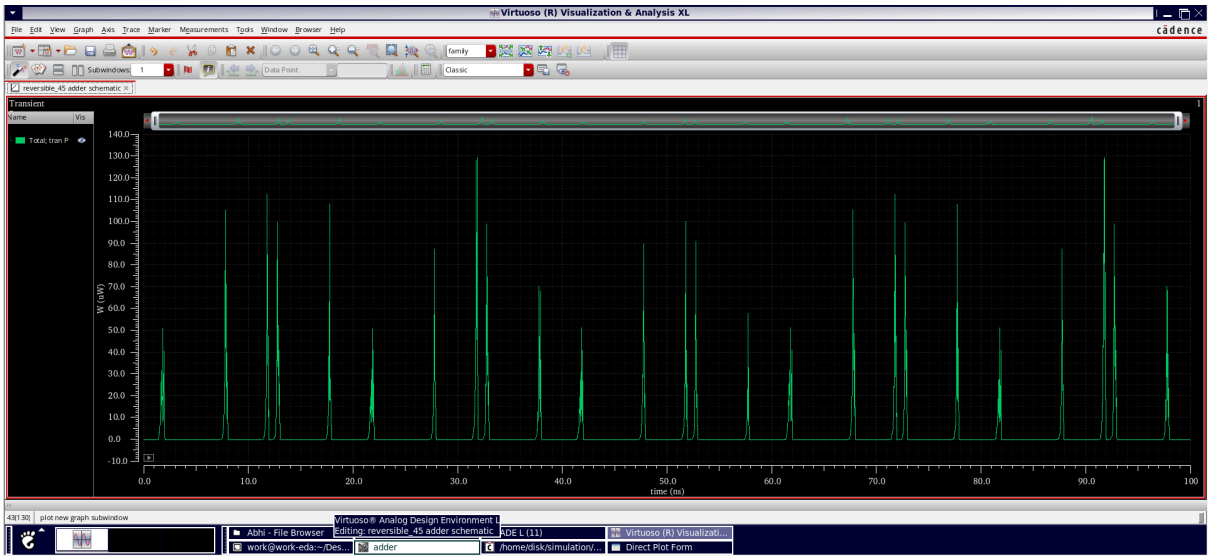
490.4E-9


Vdd
A
B
Buffer
AX
P
XOR
Xor
Q
AND
And
R
Vss

Adder_45nm:


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
reversible_45 adder schematic
Transient
Sat Nov 15 15:58:45
/Carry
/Sum
/C
/B
/A
V (V)
time (ns)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100
work@work-eda:~/Desktop/Abhi
virtuoso
ADE L (11)
Virtuoso (R) Visualizati...
work@work-eda:~/Des...
adder
/home/disk/simulation/...


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
reversible_45 adder schematic
Transient
Total: tran P
W (uW)
time (ns)
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10.0
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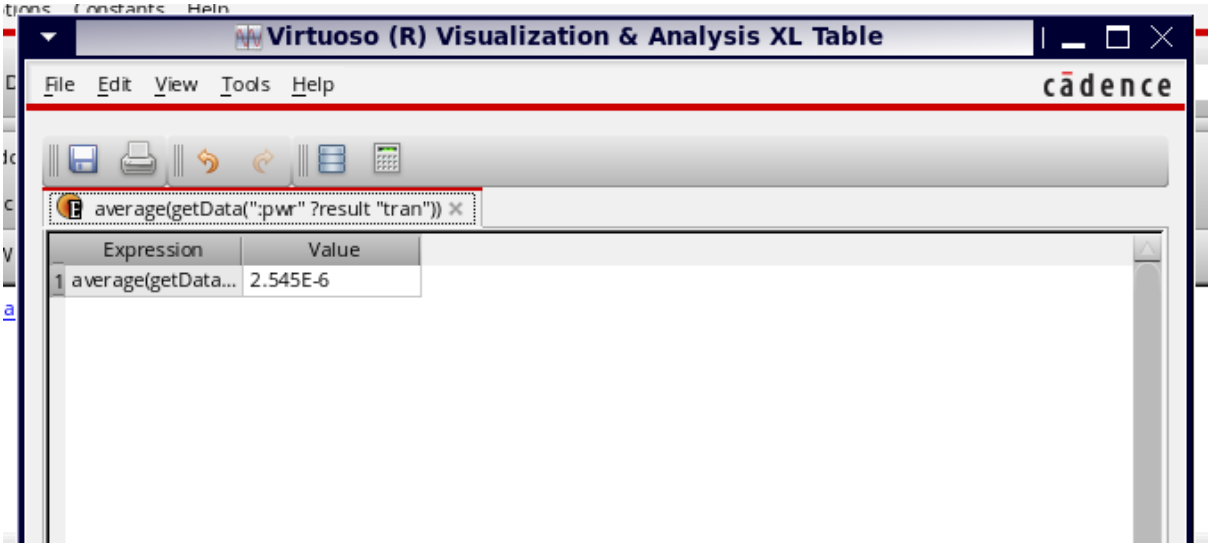
70.0
80.0
90.0
100
Abhi - File Browser
Virtuoso® Analog Design Environment L
Editing: reversible_45 adder schematic
ADE L (11)
Virtuoso (R) Visualizati...
work@work-eda:~/Des...
adder
/home/disk/simulation/...
Direct Plot Form


Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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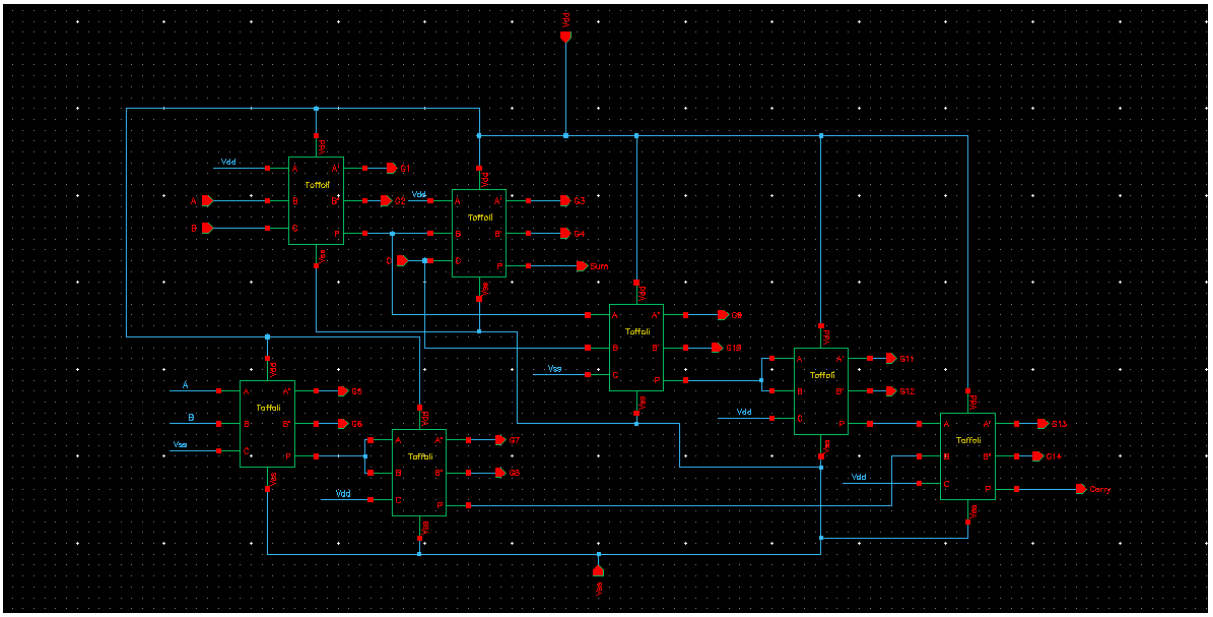
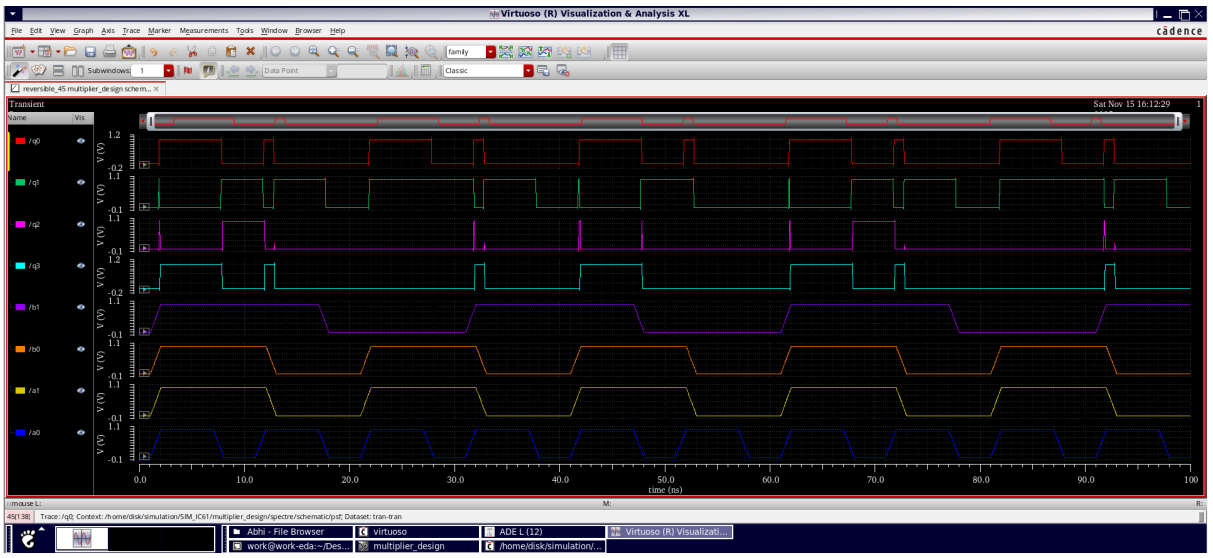
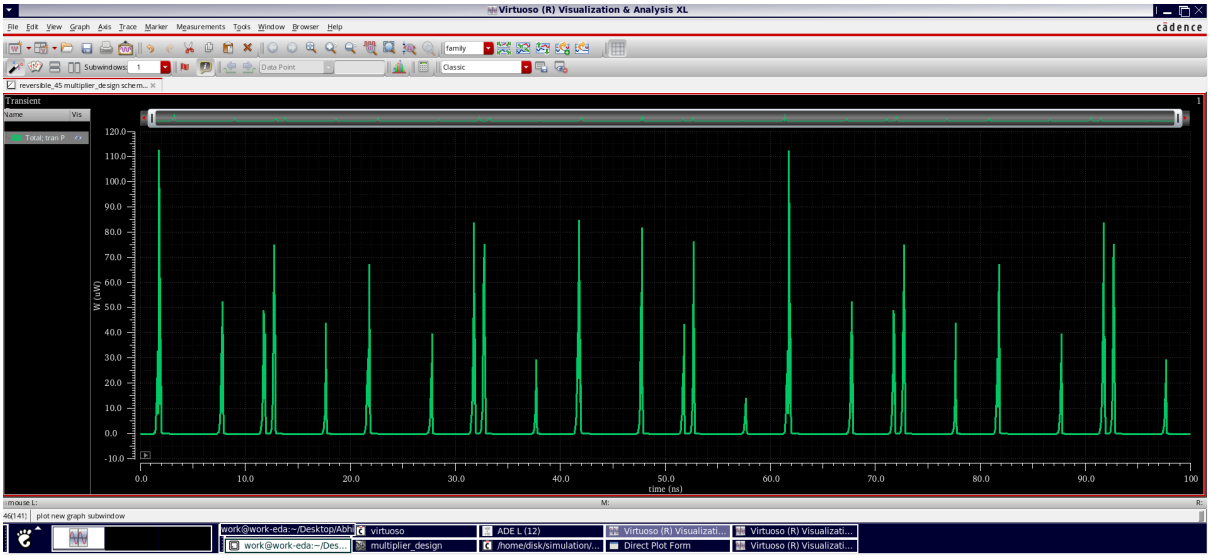
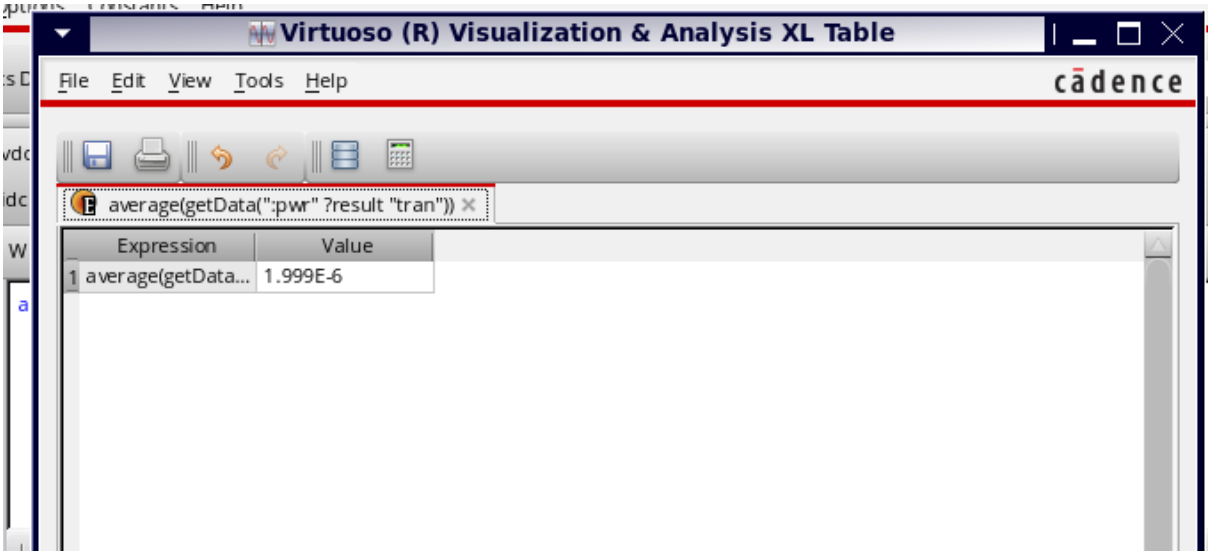
Expression
Value
1
average(getData...
2.545E-6



Multiplier_45nm:




Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient
W (uW)
time (ns)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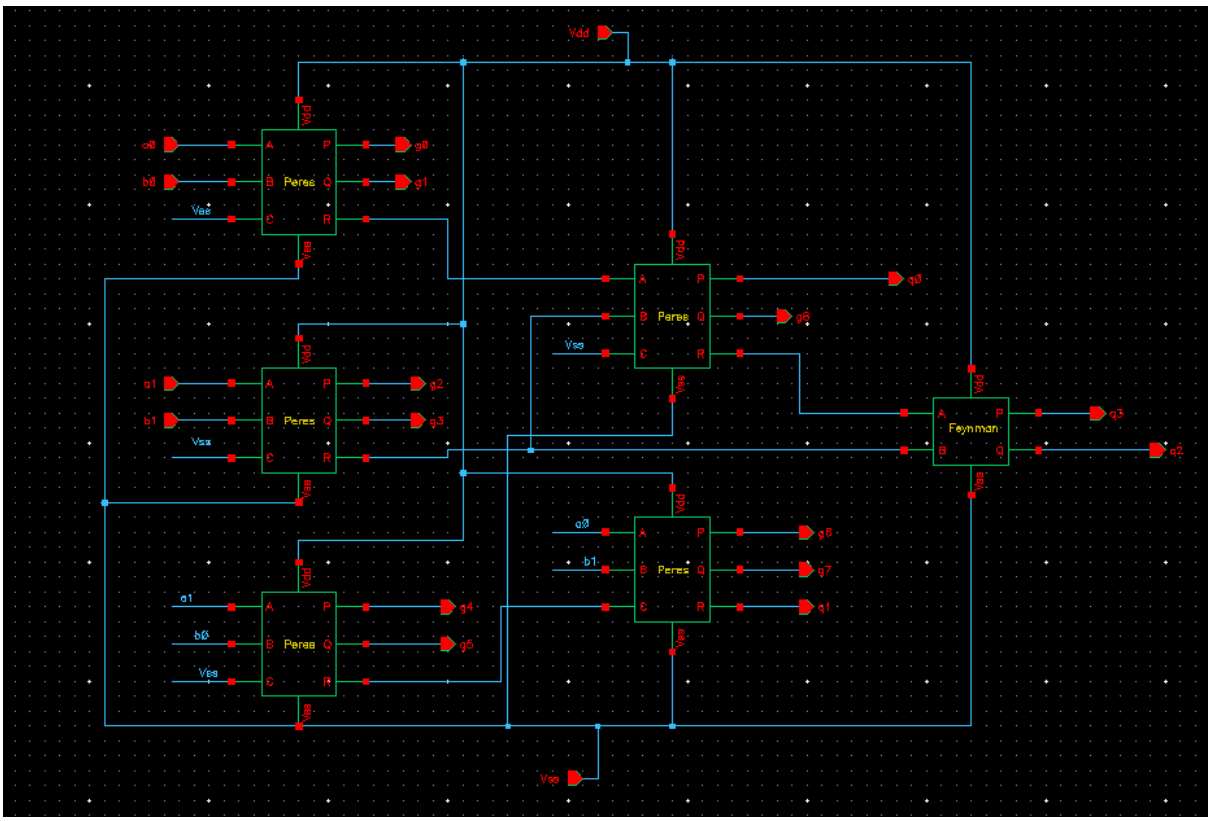
Vdd
a0
b0
Vss
Peres
g0
g1
a1
b1
g2
g3
g4
g5
g6
g7
Feynman
q0
q1
q2
q3