

सूक्ष्म कणिका एवं संचार अभियंत्रण विभाग

Department Of Electronics & Communication Engineering मोतीलाल नेहरू राष्ट्रीय प्रौद्योगिकी संस्थान इलाहाबाद

MOTILAL NEHRU NATIONAL INSTITUTE OF TECHNOLOGY Allahabad

प्रयागराज — 211004 PRAYAGRAJ - 211004

Computer Architecture (EC16106)

Tutorial No. 7

- 1. Explain the Memory Hierarchy system. What are three properties that must be satisfied by the memory system?
- 2. What is the difference between isolated I/O and memory-mapped I/O? What are the advantage and disadvantage of each?
- 3. How the data transfer between I/O and memory can be performed by the DMA? Explain with help of block diagram.
- 4. A CPU has 32- bit memory address and a 256 KB cache memory. The cache is organized as a 4-way set associative cache block size of 16 bytes.
 - a) What is the number of sets in cache?
 - b) What is size (in bits) of the tag field per cache block?
 - c) What is the number and size of comparators required for tag matching?
 - d) How many address bits are required to find the byte offset within a cache block?
 - e) What is the total amount of extra memory (in bytes) required for the tag bits?
- 5. How mapping is done from cache memory to main memory? Explain one mapping method with help of example.
- **6.** Write short notes:
 - a) Cache memory
 - b) RAM and ROM
 - c) Main memory and Secondary memory
 - d) Flash memory
- 7. Design a memory interfacing circuit for 8085 kit using memory chips/decoder IC given in figure below. Address range of 2732 EPROM should begin at 0000H and additional 4K memory space should be available for future expansion. Give the memory range of each memory chip. Address range should be continues and use only given IC (without using any other hardware).

