MINI PROJECT SYNOPSIS

Mini-Project Batch No.	:	BE/ECE/Sem-6/Section-	Batch Group No –
Semester & Section	:	VI	A,A,B,D
Academic Year	:	2021- 2022, Even Semester	
Course Name & Code	:	Mini Project & 19EC6DCMPR	
Title of the 6th Sem BE miniproject work	:	Low Power Scan-based Built-in Self-test Based on True Random Number Generator Using Multistage Feedback Ring Oscillator	
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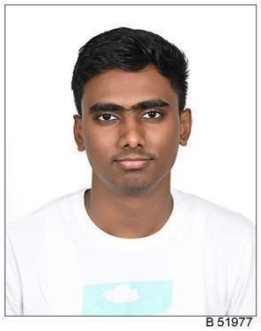
Mini-Project Sec. in-charge	:	Prof. Yashaswini Gowda N	Sign :
Mini-Project Coordinator	:	Prof. Trupti Tagare	Sign :
Head of the Department	:	Dr. T.C. Manjunath	Sign :
Field / Area of mini-project	:	VLSI	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Abstract :

A new low power scan-based built-in self-test (BIST) technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design for testability architecture is modified slightly while the linear feedback shift register is kept short. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach. This Proposed design will be implemented by Verilog HDL and simulated by Modelsim Tool.

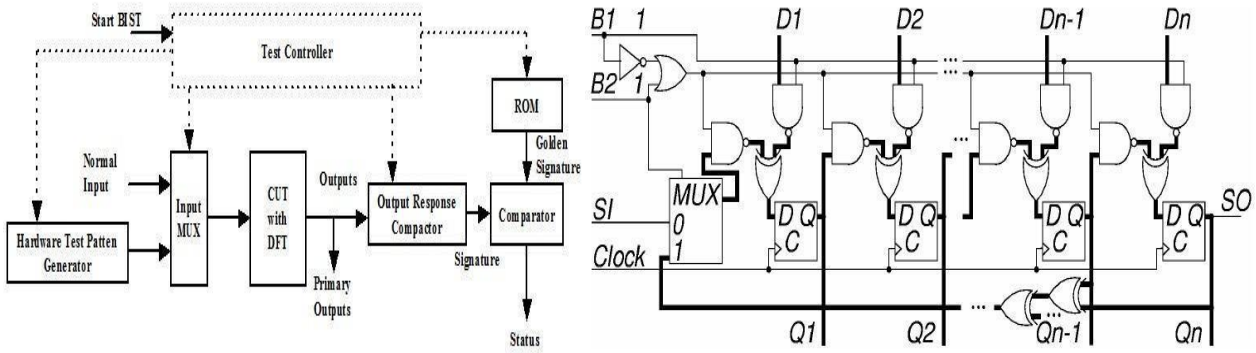
Introduction –

The gap between functional and test power consumption is growing bigger and bigger, with the latter reaching 2X to 5X of the former due to the ever-shrinking functional power and ever-increasing test power. Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe. A fast simulation approach was proposed for low-power (LP) off-chip interconnect design Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching activities caused by random patterns. Therefore, it is essential to propose an effective LP BIST approach. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods can effectively improve fault coverage.

Objective -

A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. To improve the low power scan based by using Xilinx and modelsim. Section 2 provides a Low power scan-based built-in self-test. Section 3 is about the Result and Discussion and Sections 4 and 5 is about Conclusion and Future works.

Block Diagram & Flow Chart –



Tools used (hardware / software) : Verilog language for Hardware designing, Intel Quartus Prime software for designing and verification.

Applications & Advantages :-Reduces switching activity: The BIST technique can reduce switching activity during test operation. Low power: The technique is low power. Support for both pseudorandom testing and deterministic BIST: The technique supports both pseudorandom testing and deterministic

BIS Application:-LBIST with TRNG based on MSFRO offers low-power, secure testing for integrated circuits.

It's applicable in IC testing, hardware security, key generation, tamper detection, authentication, secure communication, cryptographic protocols, and IoT security.\

Expected Outcome : The integration of Low Power Scan-based Built-in Self-test (LBIST) with a True Random Number Generator (TRNG) using Multistage Feedback Ring Oscillator (MSFRO) yields efficient integrated circuit testing, enhanced hardware security, reliable cryptographic key generation, and fortified IoT security measure.

Flow-line: Apr - Case Study, topic search, finalization, approval from guide

Apr – Starting of the mini-project work, stud

May-first phase presentation

June - Final implementation & mini-project demo with mini-project