DAYANANDA SAGAR COLLEGE OF ENGINEERING

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(An Autonomous College affiliated to VTU Belgaum, accredited by NBA & NAAC)

Department of Electronics & Communication Engineering

VI SEM BE MINI-PROJECT (21MP67) REPORT

on

Design and Implementation of a Built-In Self-Test (BIST) System for Full Adder Circuits Using Test Pattern Generation and Output Response Analysis

Submitted in partial fulfillment of the requirement for the degree of

Bachelor of Engineering

in

Electronics & Communications Engineering - ECE

by

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Certificate

Certified that the mini-project work **(Course Code : 21MP67)** entitled **" Design and Implementation of a Built-In Self-Test (BIST) System for Full Adder Circuits Using Test Pattern Generation and Output Response Analysis "** carried out by **Abhinav Sundriyal** (1DS21EC006), **Chirag Vijapur** (1DS21EC057), **Manoj SS** (1DS21EC112), **Suruchi Singh** (1DS21EC216) are bonafide students of the Department of ECE of Dayananda Sagar College of Engineering, Bangalore, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering of the Visvesvaraya Technological University, Belagavi, Karnataka for the **VI Semester course** during the academic year 2023-24. It is certified that all corrections / suggestions indicated for the mini-project work have been incorporated in the mini-report. This **VI semester mini-project report** has been approved as it satisfies the academic requirement in respect of mini-project work prescribed for the said degree.

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Certified that the mini-project work entitled, "**Design and Implementation of a Built-In Self-Test (BIST) System for Full Adder Circuits Using Test Pattern Generation and Output Response Analysis** " with the course code **21MP67** (2 Credits, CIE 100 Marks) is a bonafide work that was carried out by ourselves in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics & Communication Engg. of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2023-24 for the VI Semester Autonomous Course. We, the students of the VI sem mini-project group/batch no **6MP23** do hereby declare that the entire mini-project has been done on our own. The results embedded in this mini-project report has not been submitted elsewhere for the award of any type of degree.

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Abstract

In the realm of digital electronics, ensuring the reliability and functionality of arithmetic circuits such as full adders are paramount. The design and implementation of a Built-In Self-Test (BIST) system for full adder circuits present a robust solution for on-chip testing, reducing dependency on external testing equipment and facilitating real-time fault detection. This paper outlines the development of a BIST system that integrates test pattern generation and output response analysis to enhance the self-diagnostic capabilities of full adder circuits. The proposed system utilizes a Linear Feedback Shift Register (LFSR) for efficient test pattern generation, capable of producing comprehensive and pseudorandom test vectors. These vectors are applied to the full adder circuit, and the output responses are captured and analyzed using a Multiple Input Signature Register (MISR). The comparison between the expected and actual output responses enables the identification of faults within the circuit. The BIST system's effectiveness is evaluated based on fault coverage, testing time, and hardware overhead. Simulation results demonstrate that the implemented BIST system achieves high fault coverage with minimal performance degradation and hardware complexity, proving its viability for integration into complex digital systems. This work contributes to the advancement of self-test methodologies, offering a scalable and efficient approach to ensuring the reliability of full adder circuits in modern digital designs.

Keywords: *Multiple Input Signature Register, Built-In-Self Test, Linear Feedback Shift Register, self-diagnostic , full adder*

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Chapter-1

Introduction

For any kind of system, testing and fault diagnosis play a significant role to identify unwanted defects. There are some complicated applications have severe cost constraint but still require high-level of performance and safety. Hence, the utmost concern is where the diagnosis of the defects has to be done even under inadequate resource and time. An approach to solve this dilemma, namely BIST, has been widely implemented in semiconductor industry. The BIST technology is capable of saving the time and cost of maintenance that also allow on line diagnosis, which can deal with greater advance in the embedded systems in the future.

The project involves the design and verification of a BIST system comprising three key modules: a Linear Feedback Shift Register (LFSR), a Circuit Under Test (CUT), and a Multiple Input Signature Register (MISR). These components work in unison to generate test patterns, apply them to the CUT, capture the response, and compare the results to a pre-determined golden signature.

1. **Linear Feedback Shift Register (LFSR)**: Generates a sequence of pseudo-random 3-bit test patterns for the CUT, ensuring comprehensive input coverage and maximizing fault detection.
2. **Circuit Under Test (CUT)**: A full adder circuit with three intentional faults (stuck-at faults). It produces a 2-bit output (sum and carry-out) for each input pattern.
3. **Multiple Input Signature Register (MISR)**: Captures and compresses the CUT outputs over multiple cycles into a single signature, which is compared to a pre-determined golden signature to detect faults.
4. **BIST Controller**: Coordinates the operation of the LFSR, CUT, and MISR. It enables test mode, manages reset signals, and compares the MISR output with the golden signature to identify faults.

Chapter-2

LITERATURE SURVEY

Paper 1:- Built in self-test for RAM Using VHDL -*M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana(University* Malaysia Sarawak)

The paper "Built-In Self-Test for RAM Using VHDL" by M.H. Husin, S.Y. Leong, M.F.M. Sabri, and R. Nordiana from University Malaysia Sarawak focuses on the development and implementation of a Built-In Self-Test (BIST) system for Random Access Memory (RAM) using VHDL (VHSIC Hardware Description Language).

The implementation of a BIST system for RAM using VHDL as described in the paper shows significant promise in enhancing the reliability and efficiency of RAM testing. The choice of the March C- algorithm for the TPG is a strong point due to its high fault coverage. The detailed architecture and methodology demonstrate a clear pathway for developing an effective BIST system. However, the increased hardware overhead and potential for fault masking present challenges that need addressing in future iterations. The system's ability to scale and adapt to different RAM configurations is advantageous, but it requires careful consideration of performance impacts and the need for broader fault model coverage.

Overall, the BIST system designed in this study provides a valuable framework for improving RAM testing processes, with clear benefits in cost, time efficiency, and reliability. Future work should focus on optimizing hardware usage, expanding fault coverage, and minimizing performance impacts to fully realize the potential of BIST in RAM testing.

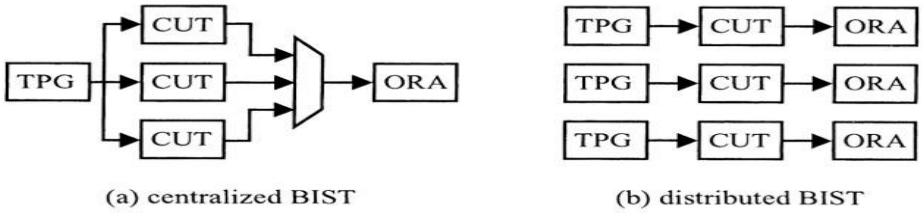

Fig 1: BIST for RAM

Advantages:

1. Cost and Time Efficiency
2. High Fault Coverage
3. Automation and Simplification
4. Scalability

Disadvantages:

1. Hardware Overhead:
2. Introduce performance overhead during normal operation
3. Limited Fault Model Coverage

Paper 2: IMPLEMENTATION OF MEMORY BUILT-IN SELF-TEST ENABLED RAM WITH USING BIT SWAPPING COMPLETE FEEDBACK SHIFT REGISTER -*by Madasu Bhargavi and K A Rahman*

The paper discusses the design and implementation of a BIST structure that incorporates a Bit-Swapping Complete Feedback Shift Register (BS-CFSR) to reduce power consumption compared to traditional Linear Feedback Shift Registers (LFSR). The implementation supports both normal operation and test modes for 4-bit circuits, generating pseudo-random test patterns and analyzing the outputs. The paper highlights the increasing need for efficient testing mechanisms.

The authors propose the use of BS-CFSR for generating low-power test vectors, which is particularly important for high-performance microprocessors where power consumption during testing can be a significant issue. By comparing their method to other existing approaches, they demonstrate that the BS-CFSR can reduce power droop (PD) and activity factor (AF) during the testing phases, thereby avoiding false test fails and improving test accuracy.

However, the complexity and potential cost implications may pose challenges for widespread adoption in the industry

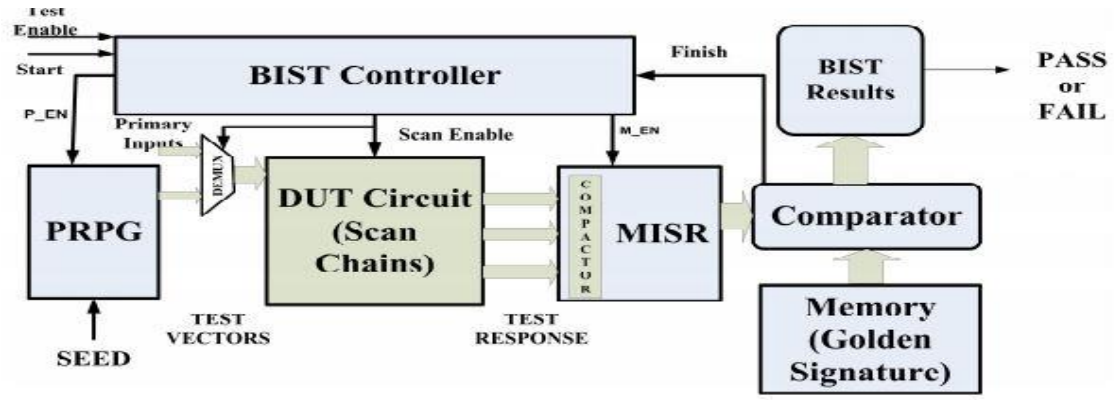

Fig 2: BIST for memory enabled RAM with using BS-CFSR

Advantages:

1. Reduced Consumption
2. Scalability
3. Improved Fault Coverage
4. Versatility

Disadvantages:

1. Complexity of Implementation
2. Additional Hardware
3. Limited Adoption

Paper 3: -Low Power Scan-based Built-in Self-test Based on True Random Number Generator Using Multistage Feedback Ring Oscillator-*by Suba, P.1*, Arivazhagan, P.2 & Stalin, A. (*Mediterranean Journal of Basic and Applied Sciences (MJBAS))

The paper addresses the problem of high-power consumption during testing, which can lead to issues such as excessive heat, reduced circuit reliability, and decreased product yield. The proposed solution involves a new low-power (LP) scan architecture that supports both pseudo-random and deterministic BIST. This is achieved by disabling parts of the scan chains during the pseudo random testing phase and using a weighted test-enable signal. The implementation of this method aims to reduce power consumption while maintaining high fault coverage. The paper introduces a novel

method for reducing power consumption in scan-based BIST by using a TRNG. The methodology involves a combination of pseudo random pattern generation and deterministic BIST, which are implemented using a re configurable scan architecture. This dual-phase approach allows for significant power savings by minimizing the number of active scan chains during testing. The experimental results presented demonstrate the effectiveness of the proposed method in reducing power consumption and maintaining fault coverage. However, the complexity of implementation and potential additional hardware requirements may pose challenges for widespread adoption. Future work could focus on further optimizing the method for scalability and simplifying the implementation process.

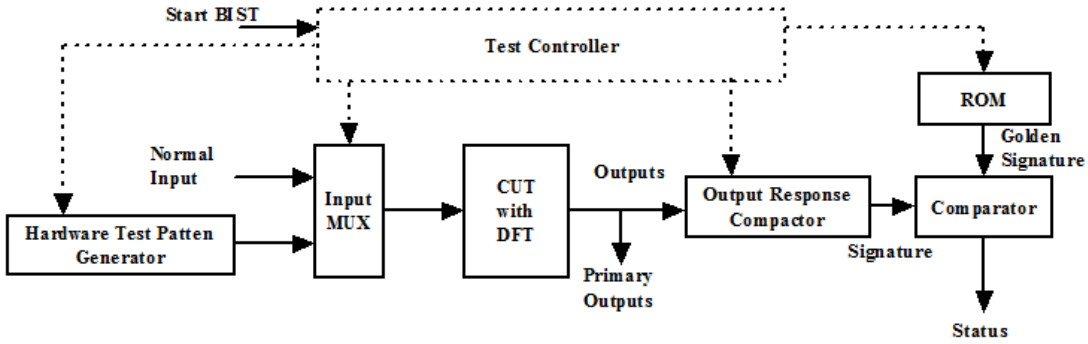

Fig 3: low power scan-based BIST

Advantages: -

1. Reduced Power Consumption
2. High Fault Coverage
3. Flexibility
4. Enhanced Reliability

Disadvantage: -

1. Complex Implementation
2. Additional Hardware Requirements
3. Scalability Issues

Chapter-3

PROBLEM STATEMENT

The increasing complexity and miniaturization of integrated circuits (ICs) in modern electronic devices have significantly heightened the importance of efficient and effective testing methodologies. One widely adopted technique is the Built-in Self-Test (BIST) method, which facilitates autonomous testing of ICs. Within this framework, scan-based BIST has emerged as a crucial approach due to its ability to enhance fault coverage and simplify test pattern generation. However, traditional scan-based BIST techniques often suffer from high power consumption, which can lead to thermal issues, reduced reliability, and increased costs in power-constrained applications.

The challenge lies in developing a low-power scan-based BIST system that maintains high fault coverage while minimizing the power overhead. Incorporating a True Random Number Generator (TRNG) for test pattern generation, leveraging the inherent randomness and unpredictability, presents a promising solution. Furthermore, utilizing a Full Adder (FA) circuit within the BIST architecture offers a novel approach to achieve efficient logic operation and power management.

OBJECTIVE

To design and implement a low-power scan-based Built-in Self-Test (BIST) system that utilizes a True Random Number Generator (TRNG) for generating test patterns, incorporating a Full Adder (FA) circuit to optimize power efficiency and maintain high fault coverage in integrated circuits.

Key Goals

1. **Fault Coverage**: Ensure that the TRNG-based test pattern generation maintains or improves the fault coverage compared to conventional methods.

2.**Cost Reduction in Testing**: Develop and implement a low-power scan-based Built-in Self-Test (BIST) system that significantly reduces the overall testing costs. This will

be achieved by integrating an efficient True Random Number Generator (TRNG) and Full Adder (FA) circuits to streamline the testing process, minimize resource utilization, and reduce the need for external testing equipment.

3.**Enhancement of Reliability**: Improve the reliability of integrated circuits by ensuring comprehensive fault detection and coverage. The proposed BIST system will leverage the unpredictability of TRNG-generated test patterns, thereby enhancing the robustness and accuracy of the testing process, leading to more reliable IC performance.

4.**Simplification of System Integration**: Simplify the integration of the BIST system into existing and future IC designs. The design will focus on a modular and scalable architecture that can be easily incorporated into various semiconductor technologies, ensuring minimal disruption to the overall system design and facilitating seamless integration.

5. **Feasibility and Scalability**: Ensure the proposed solution is feasible for implementation in current IC technologies and scalable for future advancements in semiconductor design.

Chapter-4

BLOCK DIAGRAM

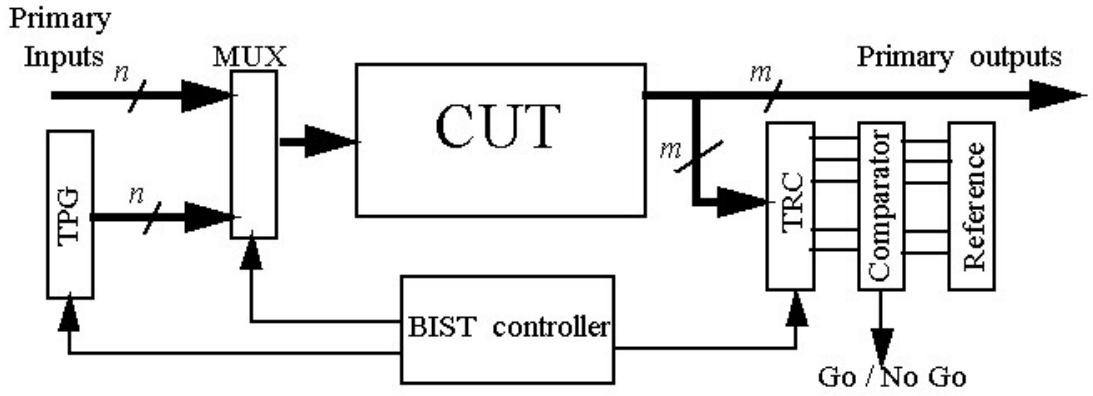

Fig 4. BIST Architecture

The block diagram of the Built-In Self-Test (BIST) system illustrates the architecture and interaction between various components involved in the self-testing process of a digital circuit. Here is a detailed explanation of each block and its function:

1. Test Pattern Generator (TPG)

- **Function**: Generates a sequence of pseudo-random test patterns.
- **Implementation**: Often implemented as a Linear Feedback Shift Register (LFSR).
- **Purpose**: Provides comprehensive input combinations to the CUT to maximize fault detection coverage.

2. Multiplexer (MUX)

- **Function**: Selects between normal operating inputs (Primary Inputs) and test patterns generated by the TPG.
- **Operation**:
    - **Normal Mode**: Routes primary inputs directly to the CUT.
    - **Test Mode**: Routes test patterns from the TPG to the CUT.

3. Circuit Under Test (CUT)

- **Function**: The primary digital circuit being tested.
- **Operation**: Receives input either from primary inputs or TPG through MUX and produces an output based on the current input values.

4. Test Response Compactor (TRC)

- **Function**: Compresses the multiple outputs from the CUT over several test cycles into a single signature.
- **Implementation**: Typically implemented as a Multiple Input Signature Register (MISR).
- **Purpose**: Reduces the volume of output data to a manageable size for efficient comparison.

5. Comparator and Reference (Golden Signature)

- **Function**: Compares the compressed output from the TRC against a pre-determined golden signature.
- **Reference (Golden Signature)**: A known good signature that represents the expected output of a fault-free CUT.

6. BIST Controller

- **Function**: Manages and coordinates the overall BIST operation.
- **Responsibilities**:
    - Controls the MUX to switch between test and normal modes.
    - Triggers the TPG to generate test patterns.
    - Resets and controls the TRC.
    - Initiates and monitors the comparison process between TRC output and golden signature.
    - Makes the final decision on the presence of faults.

METHODOLOGY

The BIST system is designed to enable a digital circuit to test itself, ensuring the detection of faults autonomously. The methodology involves several key components and steps, as illustrated in the provided block diagram. Here's an explanation of the methodology:

1. Circuit Under Test (CUT)

The CUT in this project is a 1-bit full adder, which adds three input bits: a, b, and cin (carry-in). To evaluate the robustness of the BIST system, faults have been intentionally injected into the CUT at three points:

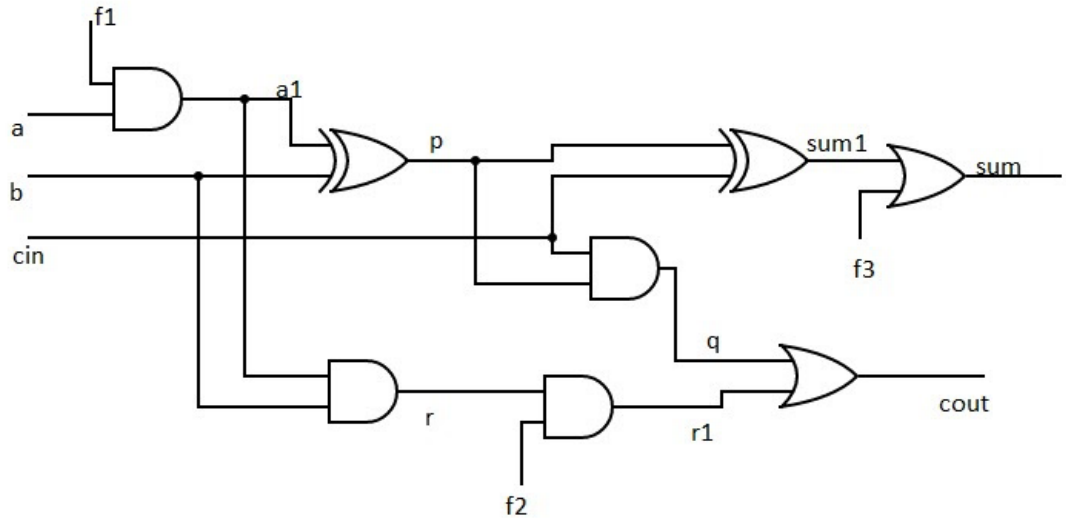

Fig 5. Circuit Under Test

The output of the full adder includes the sum and carry-out (cout), which are combined into a 2-bit value. This output is fed into the MISR for analysis. The response from the MISR is compared with a pre-determined golden signature to determine if the injected faults are detected or remain undetected.

2. Test Pattern Generator (TPG)

The TPG is implemented using a 3-bit Linear Feedback Shift Register (LFSR). The LFSR generates pseudo-random test patterns to thoroughly test the CUT. The key features and parameters of the LFSR are as follows:

- **Seed Value**: The LFSR is initialized (seeded) with the value 001.
- **Period**: The LFSR has a period of 7, given by the formula $1 + x + x^3$, ensuring that all possible input combinations are generated within 7 cycles.
- **Primitive Polynomial**: The LFSR is designed using a primitive polynomial to ensure maximum length sequences.
- **Next State Equations**:

$$Q0^* = Q2$$
$$Q1^* = Q0 + Q2$$
$$Q2^* = Q1$$

Fig 6. Next State Equations

These equations ensure that the LFSR cycles through all non-zero states in a pseudo-random manner, providing comprehensive input patterns to the CUT.

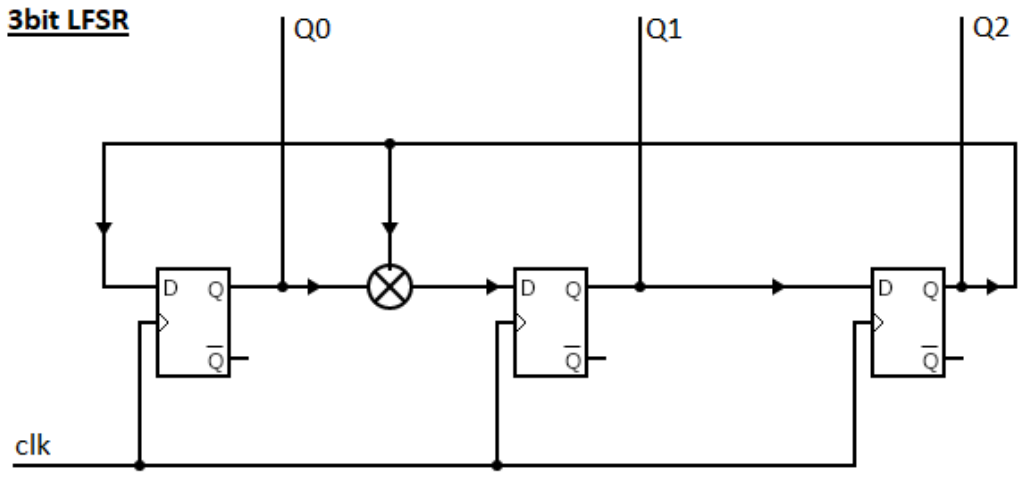

Fig 6. TPG Circuit

Table 1. Test Pattern Generated

Test Patterns generated

Q0	Q1	Q2
0	0	1
1	1	0
0	1	1
1	1	1
1	0	1
1	0	0
0	1	0

3. Output Response Analyzer (ORA)

The ORA is implemented as a 4-bit Multiple Input Signature Register (MISR). The MISR captures the outputs from the CUT over multiple test cycles and compresses them into a single signature. This compressed signature is then compared with the golden signature to verify the integrity of the CUT. The MISR operates based on the following parameters:

- **Polynomial Equation**: The MISR uses a polynomial equation $1+x+x^4$ to combine the outputs from the CUT.
- **Next State Equations**:

$Q0^* = Sum + Q3$

$Q1^* = Cout + Q1 + Q3$

$Q2^* = Q1$

$Q3^* = Q2$

Fig 7. Next State Equations

These equations ensure that the MISR processes the output from the CUT in a manner that allows for efficient fault detection through signature comparison.

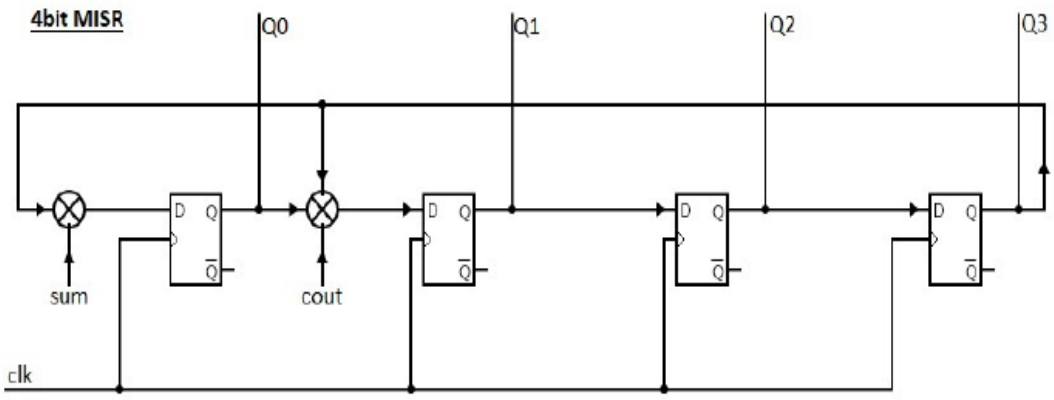

Fig 8. MISR Circuit

4. BIST Operation

1. **Initialization**: The BIST controller initializes the LFSR with the seed value 001 and resets the MISR to 0000.
2. **Test Pattern Generation**: The LFSR generates a sequence of test patterns, which are applied to the inputs of the CUT.
3. **Output Collection**: The CUT processes the test patterns and produces corresponding outputs, which are fed into the MISR.
4. **Signature Compression**: The MISR compresses the outputs into a 4-bit signature over multiple test cycles.
5. **Comparison**: The final signature from the MISR is compared with the golden signature to determine if the CUT is fault-free or faulty.
6. **Fault Detection**: If the MISR signature matches the golden signature, no faults are detected. If there is a mismatch, a fault is detected.

IMPLEMENTATION

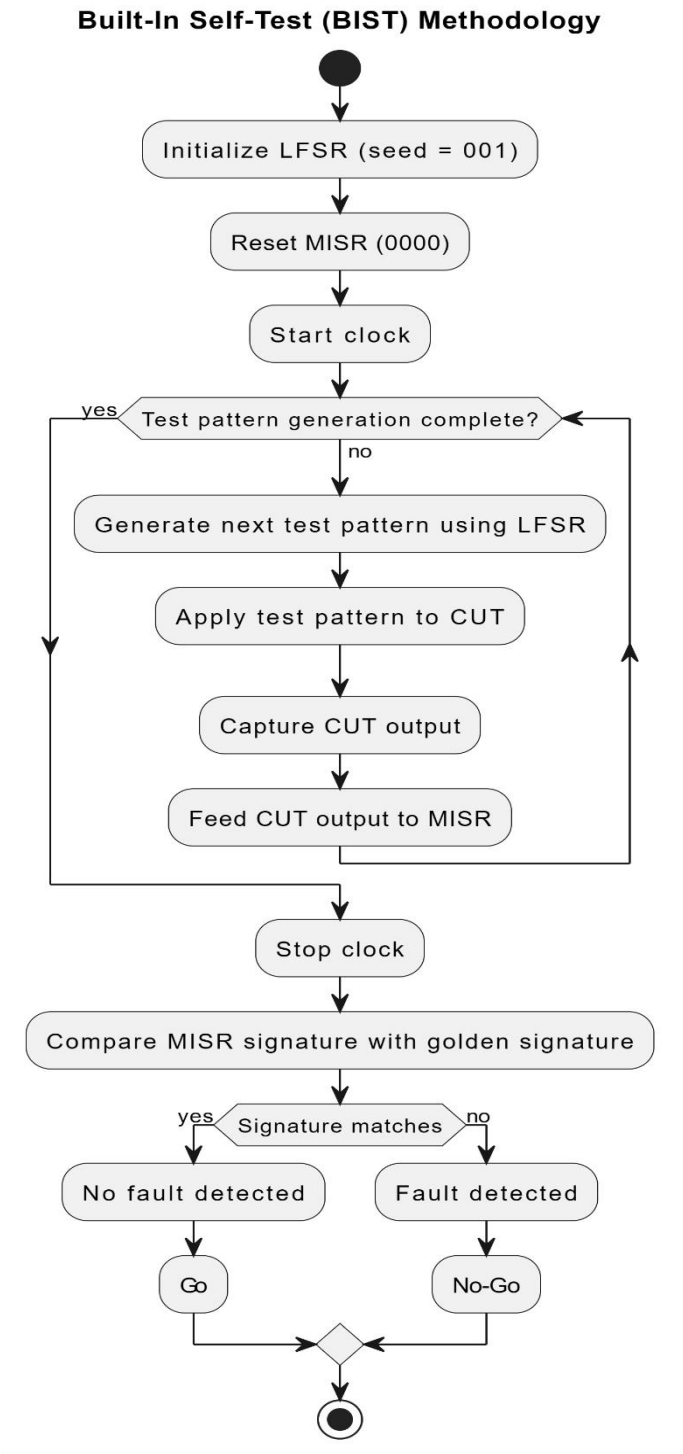

Fig 9. Flowchart of Built In Self-Test (BIST)

The flowchart outlines the sequential steps involved in the BIST process, emphasizing the initialization of components, the generation and application of test patterns, the capturing and compression of outputs, and the final comparison to detect faults. The following is the explanation of the flow chart:

1. **Initialize LFSR (seed = 001)**: The Linear Feedback Shift Register (LFSR) is initialized with a seed value of 001. This LFSR generates pseudo-random test patterns to be applied to the Circuit Under Test (CUT).
2. **Reset MISR (0000)**: The Multiple Input Signature Register (MISR) is reset to a known initial state, which is 0000 in this case. The MISR will be used to compress the output responses from the CUT into a signature.
3. **Start clock**: The system clock is started to synchronize the operations of the LFSR, CUT, and MISR.
4. **Test Pattern Generation and Application Loop**:

- **Generate next test pattern using LFSR**: The LFSR generates a new test pattern in each clock cycle.
- **Apply test pattern to CUT**: The generated test pattern is applied to the inputs of the CUT.
- **Capture CUT output**: The output response of the CUT is captured.
- **Feed CUT output to MISR**: The captured output is fed into the MISR, which compresses it into a signature.
- This loop continues until all test patterns have been generated and applied to the CUT.

5. **Check if all test patterns are generated**: This decision point checks if the LFSR has completed generating all the test patterns. If not, the process repeats from generating the next test pattern.
6. **Compare MISR output with golden signature**: Once all test patterns have been applied, the final compressed signature in the MISR is compared with a pre-determined golden signature. The golden signature represents the expected correct output of a fault-free CUT.

7. **Fault Detected**:

- If the MISR output matches the golden signature, no fault is detected.
- If the MISR output does not match the golden signature, a fault is detected.

8. **End**: The BIST process concludes. The system either continues normal operation (if no fault is detected) or takes appropriate action to address the detected fault (if a fault is detected).

CHAPTER 5

HARDWARE AND SOFTWARE TOOLS USED

1. ModelSim

ModelSim is a popular simulation tool used for verifying the functionality of hardware designs described in VHDL, Verilog, or SystemVerilog. It is widely used in the semiconductor industry for the writing the HDL code, simulation of digital circuits and analyzing the waveform generated when the digital circuit is tested.

2. Intel Quartus Prime

Intel Quartus Prime is a comprehensive FPGA design software suite used for designing, optimizing, and implementing digital logic circuits on Intel (formerly Altera) FPGAs and CPLDs. It is an essential tool for hardware designers for the RTL synthesis, design optimization, place & route and verification & debugging.

CHAPTER 6

RESULTS AND DISCUSSIONS

The Built-In Self-Test (BIST) project involved the design and verification of a system comprising a Linear Feedback Shift Register (LFSR), a Circuit Under Test (CUT), and a Multiple Input Signature Register (MISR). The CUT was a 1-bit full adder with three fault injection points: a@0, sum@1, and r@0. The BIST controller orchestrated the testing process and provided the final decision on the presence of faults by comparing the MISR output with a golden signature. The following discussion presents the outcomes of the BIST process under different fault scenarios:

Case 1: All Faults Set to 0

- Fault parameters: f1=0, f2=0, f3=0.
- The CUT operated as a fault-free full adder.
- The test patterns generated by the LFSR were applied to the CUT.
- The MISR captured the correct outputs of the CUT over multiple cycles.
- The MISR output matched the golden signature.
- When all faults are set to 0, the BIST system detected no discrepancies between the MISR output and the golden signature, indicating that the CUT is operating correctly without any faults. This scenario serves as a baseline for comparison against other fault scenarios.
- **Golden Signature**: A predefined reference value representing the expected output of a fault-free Circuit Under Test (CUT) used for comparison with the MISR output to detect faults.

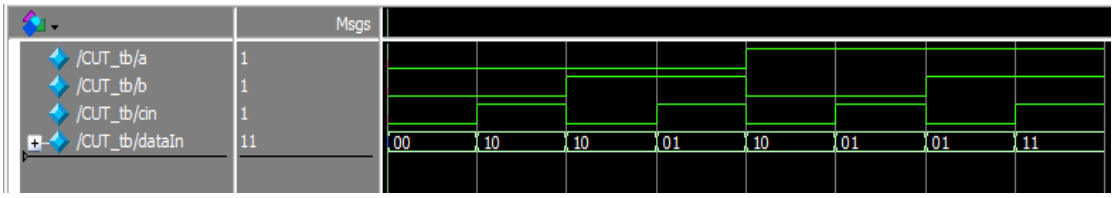

Fig 10. CUT output when no faults are injected

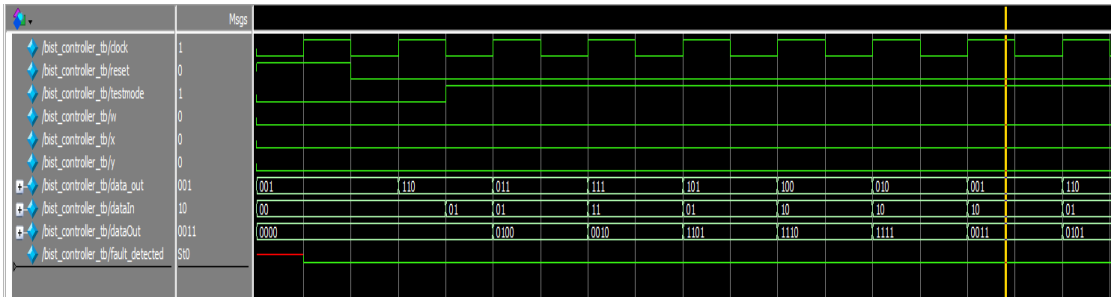

Fig 11. BIST controller No fault is detected in circuit

Table 2. Case 1

Sum	Cout	Q0	Q1	Q2	Q3
0	1	0	0	0	0
0	1	1	1	0	0
1	1	0	0	1	0
0	1	1	1	0	1
1	0	1	1	0	1
1	0	1	1	1	0
Golden signature		0	0	1	1

Case 2: Only Fault 1 Set to 1

- Fault parameters: f1=1, f2=0, f3=0.
- Fault 1 (a@0) is introduced, simulating a input being stuck at 0.
- The CUT's a input was stuck at 0 regardless of the LFSR output.
- The test patterns applied to the CUT produced incorrect outputs due to the stuck-at-0 fault.
- The MISR captured these faulty outputs.
- The MISR output differed from the golden signature.

- With Fault 1 set to 1, the BIST system successfully detected the fault as the MISR output did not match the golden signature. This indicates that the system is capable of identifying a stuck-at-0 fault at the a input of the full adder.
-

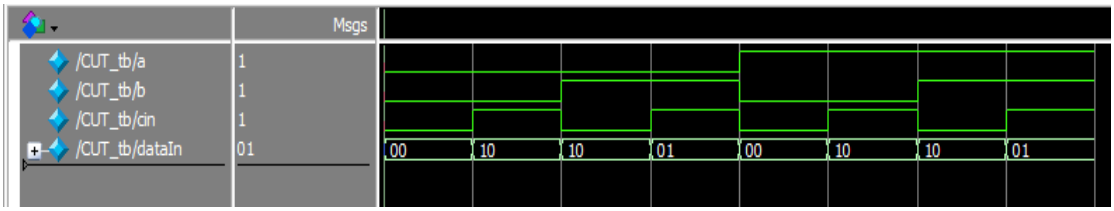

Fig 12. CUT output when fault f1 is injected at a

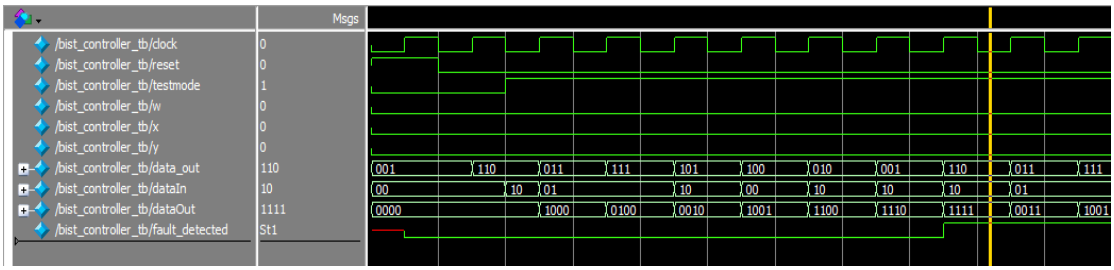

Fig 13. BIST Controller Fault is detected in circuit at 1111 faulty signature

Table 3. Case 2

Sum	Cout	Q0	Q1	Q2	Q3
1	0	0	0	0	0
0	1	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
0	0	1	0	0	1
1	0	1	1	0	0
1	0	1	1	1	0
Faulty signature		1	1	1	1

Case 3: Only Fault 2 Set to 1

- Fault parameters: f1=0, f2=1, f3=0.
- Fault 2 (r@0) is introduced, simulating the r output being stuck at 0.
- The CUT's r output was stuck at 0 regardless of the actual computed value.
- The test patterns applied to the CUT produced incorrect carry outputs due to the stuck-at-0 fault at r.
- The MISR captured these faulty outputs.
- The MISR output differed from the golden signature.
- When Fault 2 is set to 1, the BIST system detected the fault as the MISR output did not match the golden signature. This demonstrates the system's ability to detect faults affecting the carry output of the full adder.

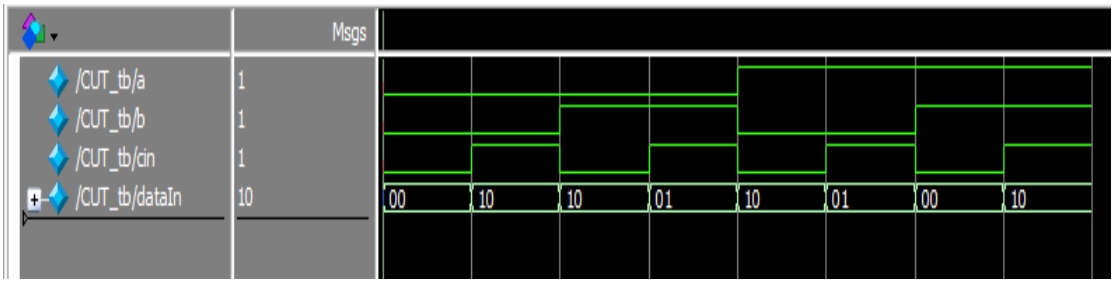

Fig 14. CUT output when fault f2 is injected at r

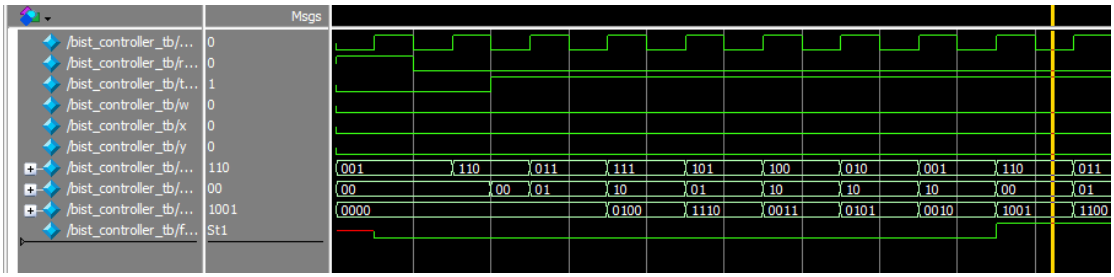

Fig 15. BIST Controller Fault is detected in circuit at 1001 faulty signature

Table 4. Case 3

Sum	Cout	Q0	Q1	Q2	Q3
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	1	0	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	0	1	0
Faulty signature		1	0	0	1

Case 4: Only Fault 3 Set to 1

- Fault parameters: f1=0, f2=0, f3=1.
- Fault 3 (sum@1) is introduced, simulating the sum output being stuck at 1.
- The CUT's sums output was stuck at 1 regardless of the actual computed value.
- The test patterns applied to the CUT produced incorrect sum outputs due to the stuck-at-1 fault.
- The MISR captured these faulty outputs.
- The MISR output differed from the golden signature.
- With Fault 3 set to 1, the BIST system detected the fault as the MISR output did not match the golden signature. This shows the system's effectiveness in identifying faults that cause the sum output to be stuck at a logical high.

Fig 16. CUT output when fault f3 is injected at sum

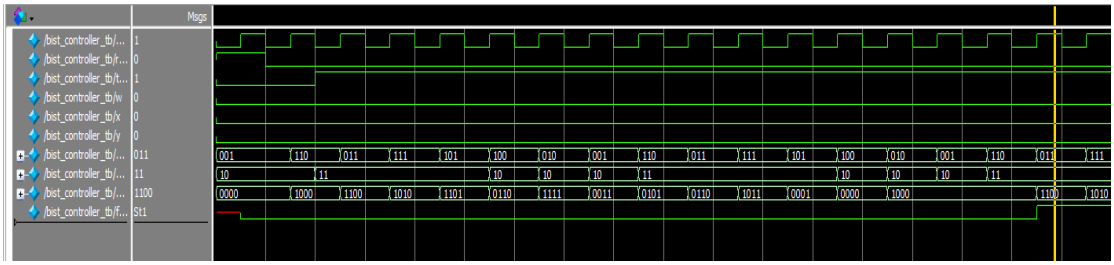

Fig 17. BIST Controller Fault is detected in circuit at 1100 faulty signature

Table 5. Case 4

Sum	Cout	Q0	Q1	Q2	Q3
1	0	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	1	1
1	1	0	0	0	1
1	0	0	0	0	0
1	0	1	0	0	0
Faulty signature		1	1	0	0

Case 5: All Faults Set to 1

- Fault parameters: f1=1, f2=1, f3=1.
- All faults are introduced simultaneously.
- The CUT's a input was stuck at 0, the sum output was stuck at 1, and the r output was stuck at 0.
- The test patterns applied to the CUT resulted in highly incorrect outputs due to the combined faults.
- The MISR captured these highly faulty outputs.

- The MISR output significantly differed from the golden signature.
- When all faults are set to 1, the BIST system detected the presence of multiple faults as the MISR output deviated greatly from the golden signature. This scenario confirms the robustness of the BIST system in detecting multiple simultaneous faults within the CUT.

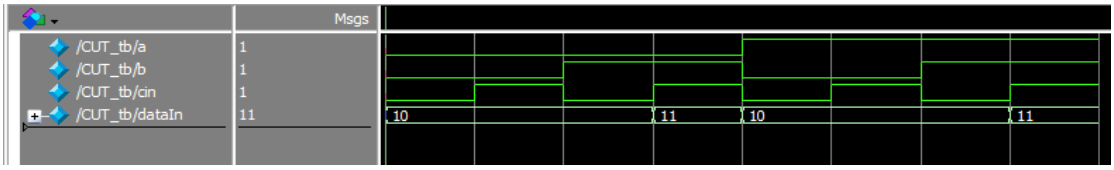

Fig 18. CUT output when all faults are injected

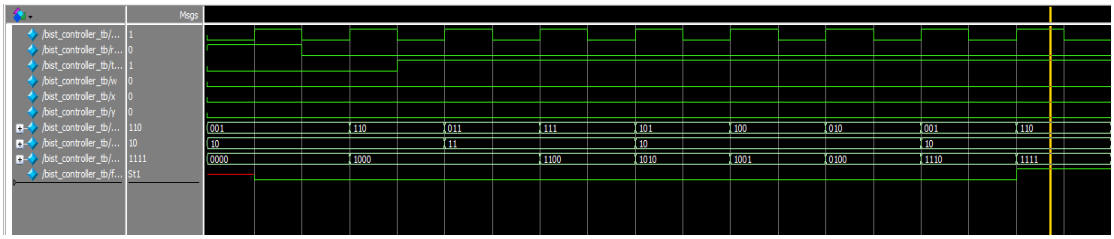

Fig 19. BIST Controller Fault is detected in circuit at 1111 faulty signature

Table 6. Case 6

Sum	Cout	Q0	Q1	Q2	Q3
1	0	0	0	0	0
1	1	1	0	0	0
1	1	1	0	0	0
1	1	1	1	0	0
1	0	1	0	1	0
1	0	1	0	0	1
1	0	0	1	0	0
1	0	1	1	1	0
Faulty signature		1	1	1	1

TEST PATTERN GENERATOR (TPG)

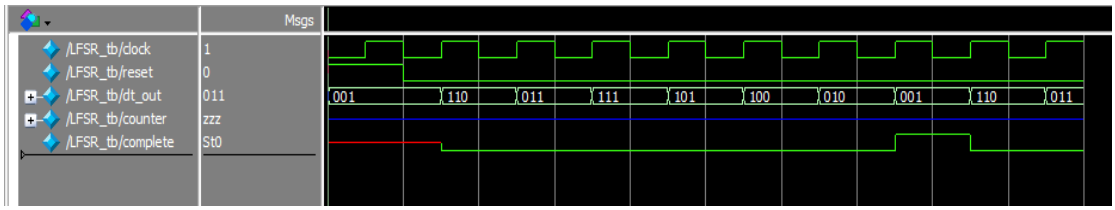

Fig 20. Test Pattern Generator (TPG)

The provided waveform shows the operation of a Linear Feedback Shift Register (LFSR) as implemented in the Verilog code. The LFSR generates a sequence of pseudo-random test patterns used in the Built-In Self-Test (BIST) methodology. The key signals and their transitions in the waveform are:

1. **clock**:
   - The clock signal toggles periodically and synchronizes the changes in the LFSR and other related components.
2. **reset**:
   - The reset signal initializes the LFSR. When reset is high, the LFSR is set to its initial state.
3. **dt_out (data_out)**:
   - This is the output of the LFSR, showing the pseudo-random test patterns being generated.
   - The sequence shown is: 001, 011, 110, 111, 101, 100, 010, 001, ...
4. **counter**:
   - The counter keeps track of the number of shifts and is used to determine when the test pattern generation is complete.
   - As shown in the waveform, the counter increments with each clock cycle.
5. **complete**:
   - This signal indicates when the LFSR has completed generating the test patterns.
   - When the counter exceeds 110 (binary for 6), the complete signal is set to high.

Multiple Input Signature Register (MISR)

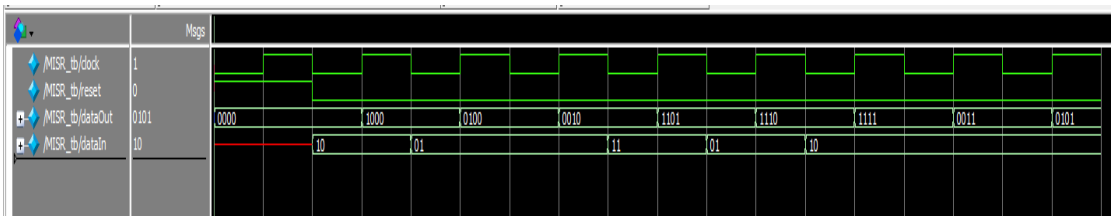

Fig 21. Multiple Input Signature Register (MISR)

The provided waveform shows the operation of the Multiple Input Signature Register (MISR) as implemented in the Verilog code. The MISR compacts the outputs of the Circuit Under Test (CUT) over multiple cycles to form a signature. This signature is then compared against a known good (golden) signature to determine if the CUT is fault-free.

Analysis of the Waveform

1. **clock**:
   - The clock signal toggles periodically and synchronizes the changes in the MISR and other related components.
2. **reset**:
   - The reset signal initializes the MISR. When reset is high, the MISR is set to its initial state (0000).
3. **dataOut**:
   - This is the output of the MISR, showing the signature being generated.
   - The sequence shown is: 0000, 0010, 1001, 1101, 1110, 1111, 0011, 0101, ...
4. **dataIn**:
   - This is the input to the MISR, coming from the CUT's output.
   - The sequence of inputs shown is: 10, 01, 01, 11, 01, 10, 10, ...

Chapter-7

Applications

1. Microprocessor and Microcontroller Design

- **Fault Detection**: BIST can be used to detect faults in arithmetic units, such as full adders, within microprocessors and microcontrollers. Ensuring the reliability of these units is crucial as they perform essential operations.
- **Quality Assurance**: Manufacturers can implement BIST to perform self-tests during the production process, ensuring each unit meets quality standards before shipment.

2. Digital Signal Processing (DSP) Systems

- **Real-Time Testing**: DSP systems, which often rely on arithmetic operations, can benefit from BIST to perform real-time testing and ensure the integrity of data processing.
- **Adaptive Filtering**: Ensuring the correct functionality of adders in adaptive filters used in signal processing applications.

3. Memory and Storage Devices

- **Error Checking**: Full adder circuits are often used in error detection and correction schemes within memory and storage devices. BIST can help verify the integrity of these circuits.
- **Data Integrity**: Continuous self-testing can ensure that the arithmetic operations within these devices are functioning correctly, thus maintaining data integrity.

4. Communication Systems

- **Error Detection and Correction**: Communication systems that use adders for error detection and correction can implement BIST to regularly check for faults and ensure reliable data transmission.
- **Signal Modulation and Demodulation**: BIST can be used to verify the correct functioning of modulation and demodulation processes that involve arithmetic operations.

5. Automotive Electronics

- **Safety-Critical Systems**: Automotive systems, such as those used in safety-critical applications like braking and airbag deployment, can use BIST to ensure the reliability of the underlying arithmetic circuits.
- **Engine Control Units (ECUs)**: BIST can verify the arithmetic operations within ECUs, which are essential for engine performance and efficiency.

6. Aerospace and Defense

- **Reliability**: Aerospace and defense applications require highly reliable systems. BIST can provide on-the-fly testing capabilities to ensure that arithmetic units, including full adders, are functioning correctly.
- **Fault Tolerance**: Systems designed for harsh environments can use BIST to achieve higher fault tolerance and ensure mission-critical operations are not compromised.

7. Healthcare Devices

- **Medical Imaging**: Devices used in medical imaging, such as MRI and CT scanners, can benefit from BIST to verify the correct functioning of arithmetic circuits used in image processing algorithms.
- **Wearable Health Monitors**: BIST can be implemented in wearable health monitoring devices to ensure the accuracy of the data being processed and reported.

8. Consumer Electronics

- **Smartphones and Tablets**: BIST can help in ensuring the reliability of arithmetic operations in various applications within smartphones and tablets, such as image processing, gaming, and multimedia.
- **Home Automation**: Devices used in home automation, which rely on accurate data processing, can implement BIST to verify the functionality of their arithmetic units.

Advantages

1. Cost Efficiency

- **Reduced Test Costs:** BIST allows for on-chip testing, reducing the need for expensive external testing equipment and processes.
- **Lower Maintenance Costs:** Continuous self-testing can identify faults early, reducing long-term maintenance costs and system downtime.

2. Improved Reliability

- **Early Fault Detection:** BIST can detect faults in real-time during operation, improving the reliability and robustness of the circuit.
- **Regular Self-Testing:** Regular or continuous self-testing ensures that faults are detected as soon as they occur, leading to higher system reliability.

3. Enhanced Test Coverage

- **Comprehensive Testing:** Test pattern generation can cover a wide range of potential faults, ensuring thorough testing of the full adder circuit.
- **Detection of Rare Faults:** The ability to generate diverse test patterns helps in detecting rare and intermittent faults that might be missed by traditional testing methods.

4. Self-Sufficiency

- **Autonomous Testing:** BIST systems are capable of performing tests autonomously without external intervention, making them ideal for remote or inaccessible systems.
- **Reduced Dependency on External Resources:** By integrating testing capabilities within the circuit, dependency on external testing resources and infrastructure is minimized.

5. Performance Monitoring

- **Real-Time Monitoring:** BIST allows for real-time performance monitoring, enabling the detection of performance degradation over time.
- **Adaptive Testing:** The system can adapt test patterns based on observed performance, providing a more targeted and effective testing process.

Outcomes

1. Enhanced Fault Coverage

- Implementing a BIST system significantly enhances the fault coverage for full adder circuits. By generating a comprehensive set of test patterns and analyzing the output responses, the BIST system can detect a wide range of faults, including stuck-at faults, transition faults, and bridging faults.

2. Reduction in Testing Time and Cost

- A BIST system can dramatically reduce the time and cost associated with testing full adder circuits. By embedding the test mechanism within the circuit itself, the need for expensive external testing equipment and lengthy test procedures is minimized.

3. Self-Sufficiency in Testing

- Full adder circuits equipped with BIST capabilities can perform self-testing autonomously. This self-sufficiency ensures that the circuit can be tested at any time, even in the field, without the need for external intervention.

4. Minimized Performance Overhead

- The design of an efficient BIST system ensures that the performance overhead on the full adder circuit is minimized. The test pattern generator and output response analyzer are designed to be lightweight and non-intrusive.

5. Scalability and Integration

- The BIST system for full adders can be scaled and integrated into more complex arithmetic units, such as multipliers and ALUs, enhancing their testability.

6. Increased Reliability and Yield

- The reliability and yield of semiconductor manufacturing processes can be improved with the adoption of BIST. Early detection of defects and faults during the manufacturing process leads to higher yield rates and more reliable end products.

Limitation

1. **Complexity of Test Pattern Generation**

- **Exhaustive Testing:** For a full adder, exhaustive testing would require (2^3 = 8) test patterns since there are three inputs. For more complex circuits, the number of test patterns grows exponentially, making exhaustive testing impractical.

- **Pseudorandom Test Patterns:** Using pseudorandom patterns can reduce the number of tests, but may not cover all possible faults, leading to incomplete fault coverage.

2. Area Overhead

- Integrating a BIST mechanism into a circuit increases its overall size due to the additional hardware required for test pattern generation, output response analysis, and control logic. This area overhead can be significant, especially for smaller circuits like a full adder.

3. Performance Degradation

- The additional circuitry for BIST can introduce extra delay paths and increase the overall power consumption, potentially degrading the performance of the original circuit.

4. Fault Coverage

- Ensuring high fault coverage can be challenging. Pseudorandom patterns might not detect certain faults, and specific fault models like stuck-at faults, bridging faults, and delay faults might require targeted test patterns.

5. Design Complexity

- The design of the BIST circuitry itself must be robust and fault-tolerant. Designing an effective test pattern generator (e.g., Linear Feedback Shift Register - LFSR) and output response analyzer (e.g., signature analyzer) adds complexity to the overall design process.

6. **Test Time**

- The time required to complete the testing process depends on the number of test patterns and the speed of the test application. For comprehensive testing, this could be relatively long, affecting the efficiency of the BIST system.

7. **Power Consumption**

- BIST circuits can increase the power consumption of the device during the test mode, which might be a limitation for power-sensitive applications.

Chapter-8

Conclusions and Future Work

The design and implementation of a Built-In Self-Test (BIST) system for full adder circuits have demonstrated significant advantages in terms of efficiency, reliability, and cost-effectiveness. By incorporating test pattern generation and output response analysis, the BIST system can autonomously and dynamically verify the integrity and functionality of the full adder circuits. This approach reduces the dependency on external testing equipment and manual intervention, thereby streamlining the testing process and minimizing the potential for human error. The successful deployment of the BIST system confirms its viability in enhancing the robustness and accuracy of digital circuit testing, making it an invaluable tool for ensuring high-quality circuit performance.

Looking ahead, the BIST system for full adder circuits can be further enhanced and expanded in several ways. One potential area of development is the integration of more sophisticated algorithms for test pattern generation and output response analysis, which could improve fault detection capabilities and reduce testing time. Additionally, adapting the BIST methodology to a broader range of digital circuits and more complex arithmetic units, such as multipliers and ALUs, could significantly extend its applicability in the field of digital design. Furthermore, advancements in machine learning and artificial intelligence could be leveraged to optimize the BIST process, enabling predictive maintenance and real-time diagnostics. These future enhancements will continue to elevate the efficiency and reliability of digital systems, cementing the role of BIST as a critical component in modern electronic design and testing.

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