Dayananda Sagar College of Engineering

Department of Electronics and Communication Engineering

ShavigeMalleshwara Hills, Kumaraswamy Layout, Bangalore – 560 078.

(An Autonomous Institute affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)

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AAT

Program: B.E.	Branch: ECE
Course: Fundamentals of CMOS VLSI Design	Semester/Section :5th Sem
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A Report on

TOPIC

CASCODED CURRENT MIRROR CIRCUIT

Submitted by

A.Himanshu	**1DS21EC001**
Abhijith Nayak	**1DS21EC004**
Abhinav. Sundriyal	**1DS21EC006**
Aditya. K. Pawaskar	**1DS21EC016**

Faculty In-charge

Dr.P.Vimala

CADENCE VIRTUOSO

- Cadence virtuoso is a very important EDA tool for electronics students learning about IC design/analysis and PCB design/analysis.
- At undergraduate level, virtuoso is majorly used for custom design and analysis of circuits based on MOS technologies, especially in the CMOS VLSI course.
- The Virtuoso System Design Platform allows IC designers to easily include system-level layout parasitic in the IC verification flow, enabling time saving by combining package/board layout connectivity data with the IC layout parasitic electrical model.
- It enables engineers to design concurrently across chip, package, and board, saving time and minimizing errors. It is ideal for designs that integrate multiple heterogeneous ICs, including RF, analog, and digital devices.

Some key benefits of Cadence Virtuoso are:

1. Easy to use, easy to understand software with an interactive interface.

2. Supports circuit design by using symbols and structures in the workspace and also allows text based design.

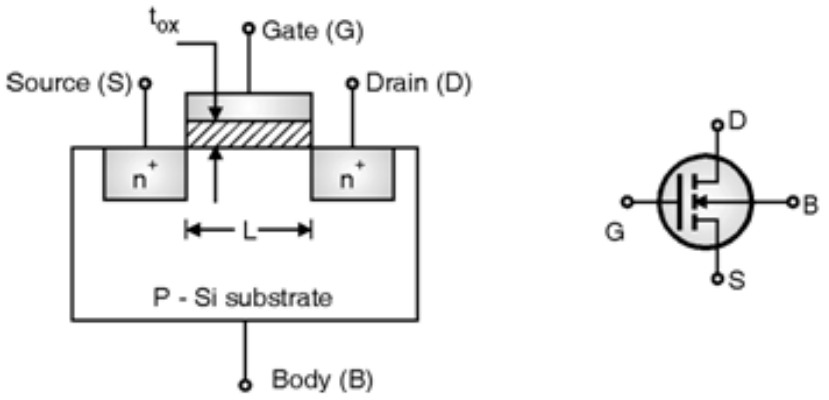
3. Great platform for beginners in the core industry to start learning about design and synthesis.

4. Allows the user to analyse the designs on various parameters like power consumption, area usage and delay.

INTRODUCTION

NMOS TRANSISTOR

NMOS transistor is a type of device which has a P-substrate and n+ type of regions in the drain and the source type. As a transistor says we can use it as a switch or an amplifier based on how we use it.
Below is the diagram for its cross-sectional view of the same



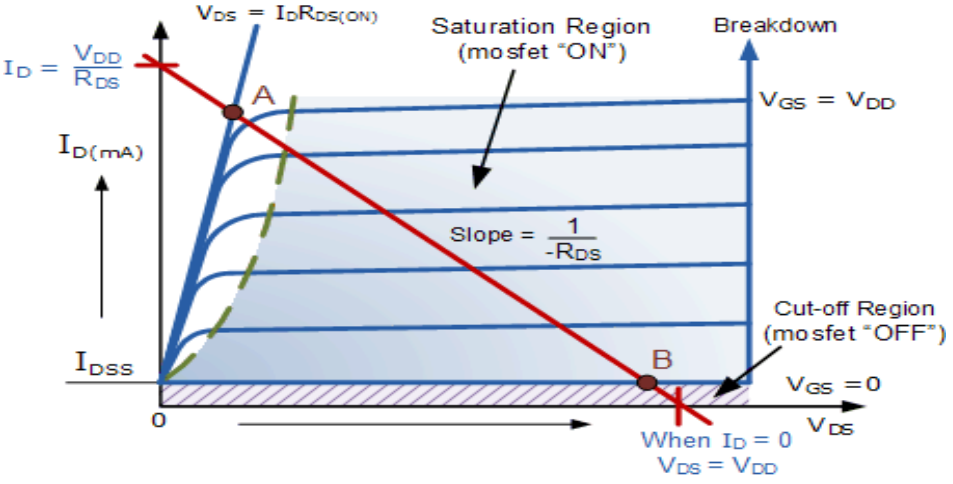
(a) Cross sectional view **(b) Symbol**

n-channel enhancement mode MOSFET

The types of operation of mosfets are as below:

1) Cut-off region
2) Linear or Ohmic region (Active)
3) Saturation region

The graph for the regions mentioned is shown below:



DIODE CONNECTED TRANSISTOR

The mosfets in general is a three terminal device used for switching and amplifying purposes. The three terminals mainly are Drain(D), Gate(G), Source(S). When we short the drain and the gate terminal of the mosfets then, the transistor becomes a two terminal device just like a diode which is represented in the fig. below

Diode connected NMOS

From the above figure we can now right the equations governing this transistor,

We know that for NMOS to be in saturation region;

Vds>=Vgs-Vt

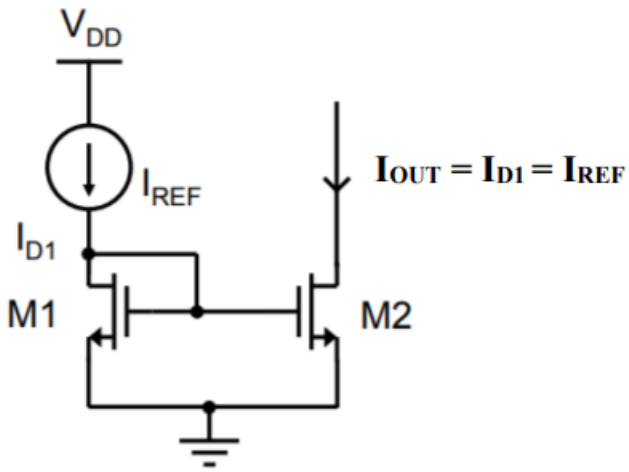
Now since drain and gate of NMOS are shorted

Vds>=Vds-Vt

Therefore, the mosfets is in saturation region.

CURRENT MIRROR

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being "copied" can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well, or it could consist of a constant current source. The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source. In analog IC design, current mirror structure is one of the most used concepts.



EQUATIONS:

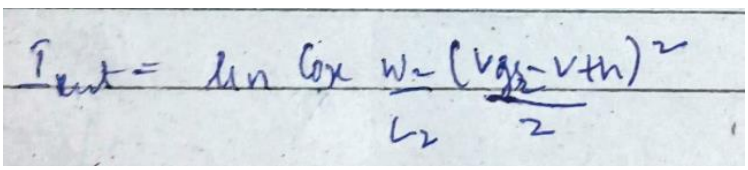
NMOS (N-Type metal oxide semiconductor)

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 \cdot (1 + \lambda \cdot V_{DS})$$

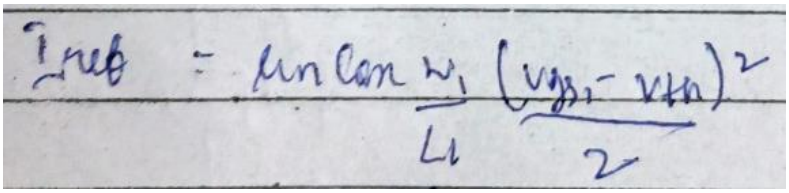
In above equation we neglect channel length modulation consider long channel mosfets have been used. There for lambda becomes zero. Therefore, we have the saturation equation as

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2$$

The equation for Iout is

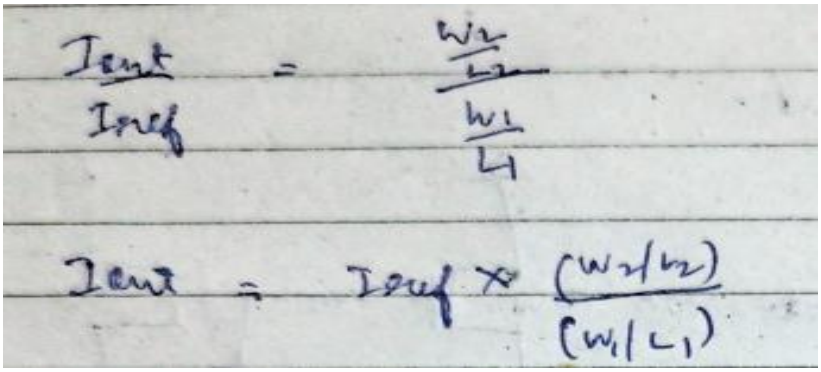


The equation for Iref is



Now since Vgs1 = Vgs2 = Vgs

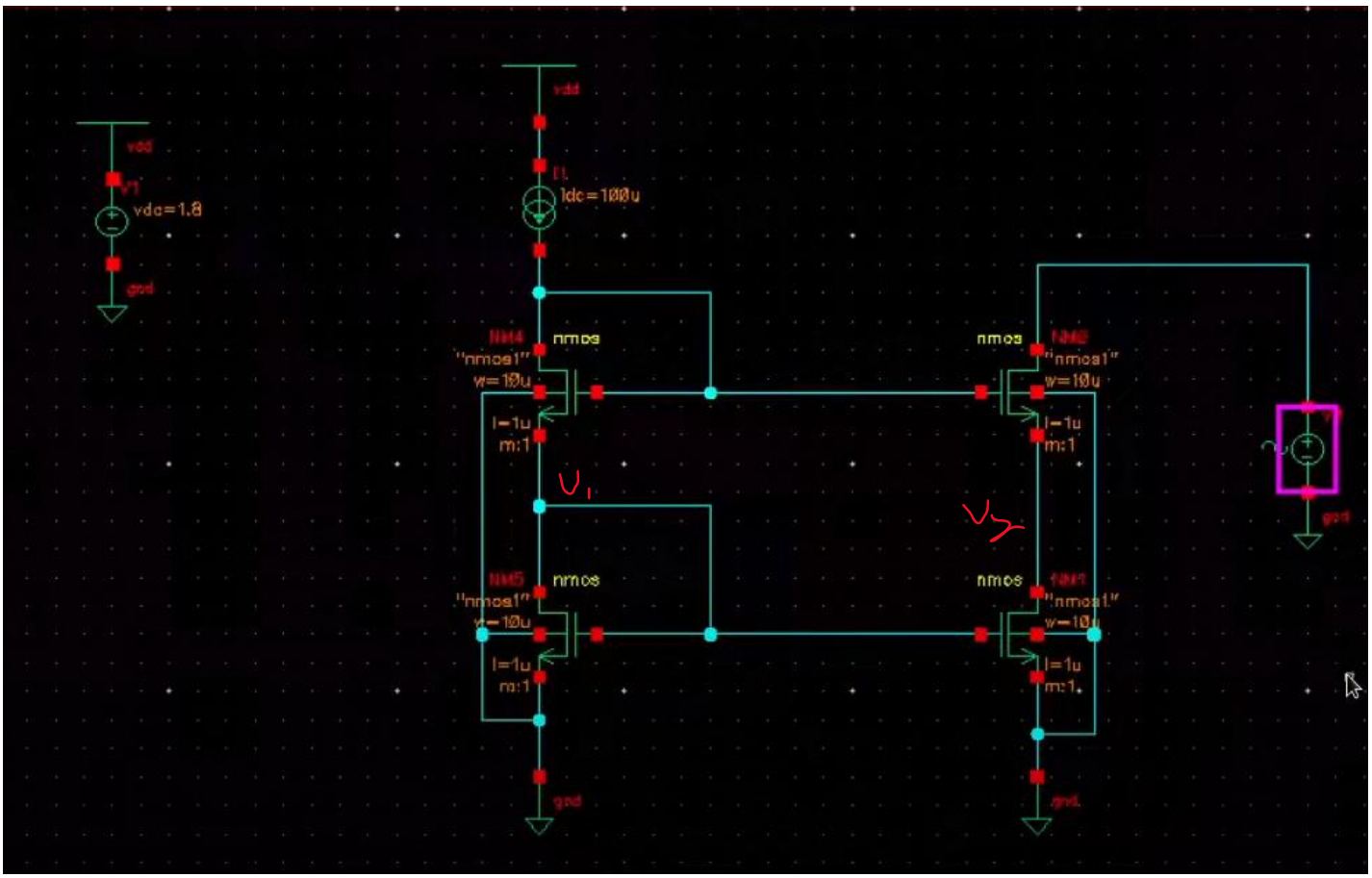
Therefore, Iout/Iref we have,



So, we can say that only by varying the W/L ratios of M2 transistor we can get the same amount of current or the multiplied version of It based on our requirements.
If we want the same current then (W/L) of M1 and (W/L) of M2 should be same.

CASCODED CURRENT MIRROR

The schematic view from cadence is shown below



Here the sizing of transistors of above 2 NMOS have to be same in order to get same values of current.

The main reason for implementing a cascoded version of current mirror is that the effect of channel length modulation is to be taken care because we cannot neglect this effect in real life implementation of analog circuits.

Now, if we divide Iout with Iref we get the ratios of (W/L)1/(W/L)2 multiplied with (1+λVds) of both M1 and M2 transistors.

Now we have to make V1 = V2 in order to match the values of Iout and Iref respectively.

By using cascoded version we Can get Vds1 = Vds2 which will cancel in the equations and thereby producing Iout = (W/L)1/(W/L)2 * Iref.

∴ Iref & Io will completely depend upon M1 & M2

additional setup will neglect channel length modulation.

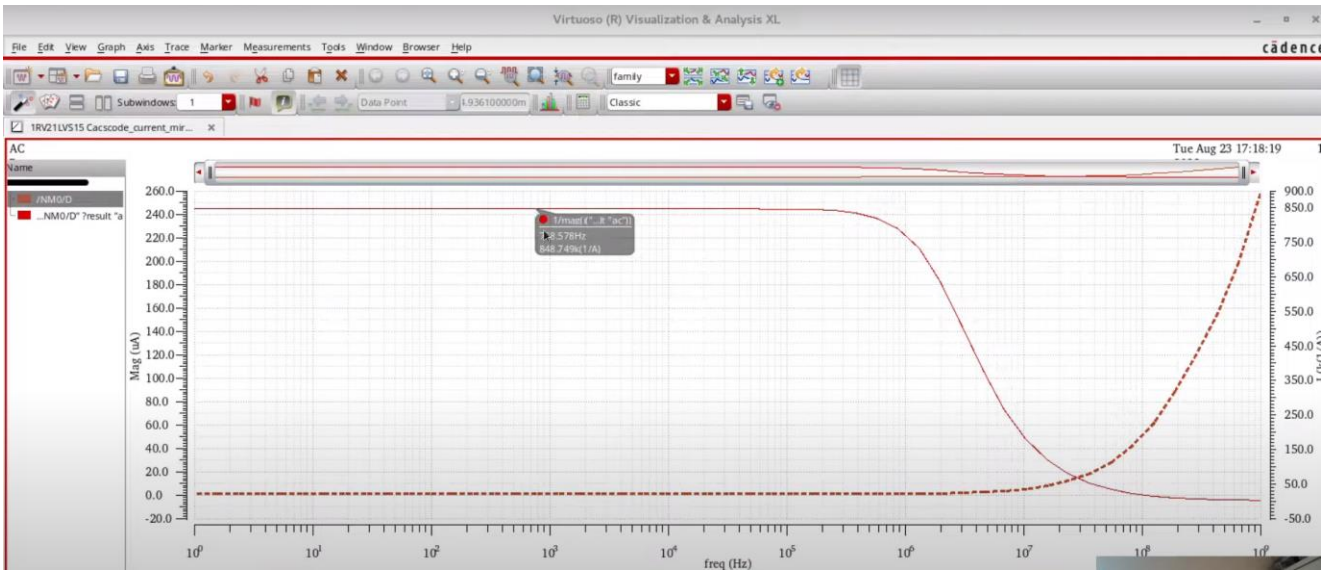
$$\frac{I_o}{I_{ref}} = \frac{(W_2/L_2)}{(W_1/L_1)} \frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \approx 1$$

now since $V_X = V_Y$

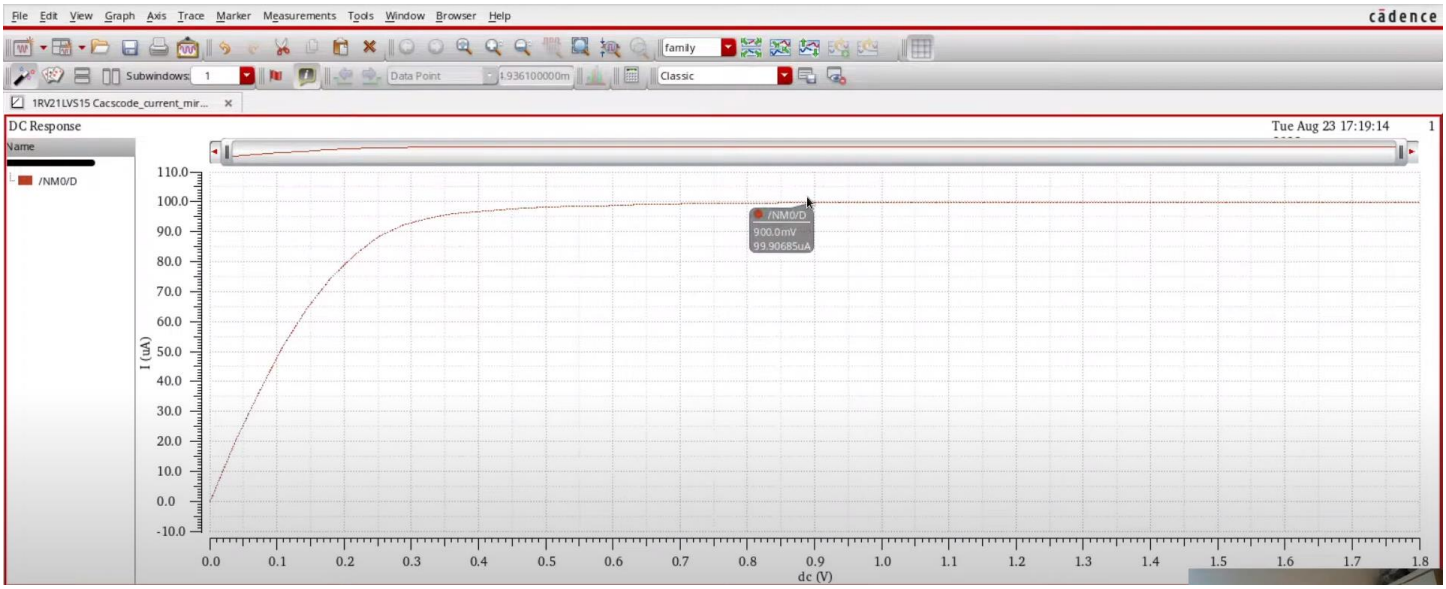
There should be some Vm in the circuit sufficient voltage else it would'nt work.

output swing V_{DD} to V_m.

Performing **AC analysis (frequency response)** for finding Rout for the above Schematic we get:



Performing **DC analysis** to find out the Iout current in microamps:



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The References used for this project include:

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