VISVESVARAYA TECHNOLOGICAL UNIVERSITY

Jnanasangama, Macche, Santibastwada Road
Belagavi-590018, Karnataka

OPEN ENDED EXPERIMENT

T Flipflops 'And' Gate

Submitted in partial fulfillment of the requirement for the degree of

Bachelor of Engineering – Third Year BE (5th Semester)
in
Electronics & Communication Engineering
by

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Under the guidance
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Faculty for **VLSI LAB**
(21ECL55)
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Department of Electronics & Communication Engineering
(An Autonomous College affiliated to VTU Belgaum, accredited by NBA & NAAC)
Shavige Malleshwara Hills, Kumaraswamy Layout,
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2023-24

Certificate

Certified that the open ended experiment titled " T Flipflop 'And' Gate " carried out by A.Himanshu(1DS21EC001), Abhijith J Nayak(1DS21EC004), Abhinav Sundriyal (1DS21EC006), Aditya K Pawaskar(1DS21EC016) are bonafide students of Dayananda Sagar College of Engineering, Bangalore, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2023-24. This report has been approved as it satisfies the academic requirement in respect of the subject **VLSI LAB** (21ECL55) prescribed for the said degree.

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Dr.P.Vimala

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M.Shruti

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Head of the Department

Dr. T.C.Manjunath

Declaration

Certified that the work entitled, "T Flipflop 'And' Gate" is a bonafide work that was carried out by ourselves in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics & Communication Engg. of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2023-24. We, hereby declare that the entire work has been done on our own & we have not copied or duplicated any other's work. The results embedded in this report have not been submitted elsewhere for the award of any type of degree.

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Date: 29/ 02 /2024

Place: Bengaluru -78

CADENCE VIRTUOSO

- Cadence virtuoso is a very important EDA tool for electronics students learning about IC design/analysis and PCB design/analysis.
- At undergraduate level, virtuoso is majorly used for custom design and analysis of circuits based on MOS technologies, especially in the CMOS VLSI course.
- The Virtuoso System Design Platform allows IC designers to easily include system-level layout parasitic in the IC verification flow, enabling time saving by combining package/board layout connectivity data with the IC layout parasitic electrical model.
- It enables engineers to design concurrently across chip, package, and board, saving time and minimizing errors. It is ideal for designs that integrate multiple heterogeneous ICs, including RF, analog, and digital devices.

Some key benefits of Cadence Virtuoso are:

1. Easy to use, easy to understand software with an interactive interface.

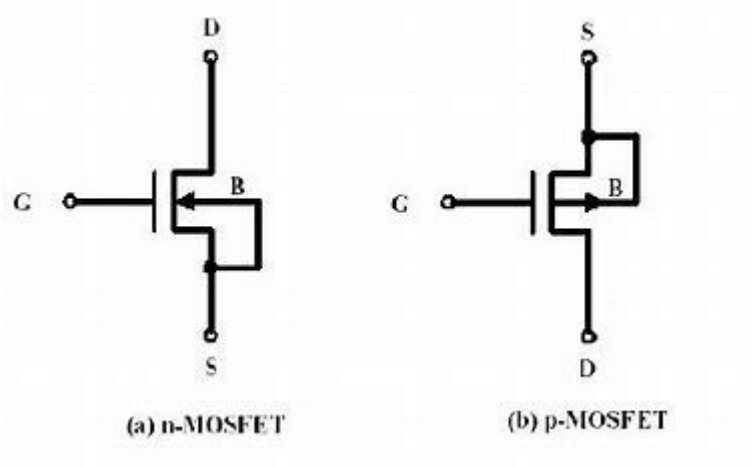
2. Supports circuit design by using symbols and structures in the workspace and also allows textbased design.

3. Great platform for beginners in the core industry to start learning about design and synthesis.

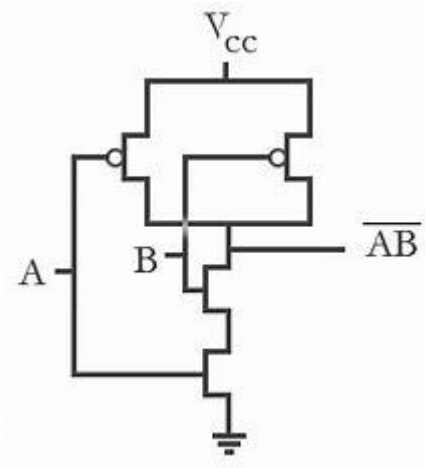
4. Allows the user to analyse the designs on various parameters like power consumption, area usage and delay.

INTRODUCTION

NMOS is a N channel metal oxide semiconductor system. It has P type Substrate and n+ type region in the drain and source. It is used to pass strong logic zero and weak logic1.
PMOS is a P channel metal oxide semiconductor system. It has N type Substrate and p+ type region in the drain and source. It is used to pass strong logic one and weak logic zero.



CMOS is Complementary metal oxide semiconductor system. It uses pair of NMOS and CMOS to design a different logic.
Below diagram shows CMOS circuit for 2 input NAND gate

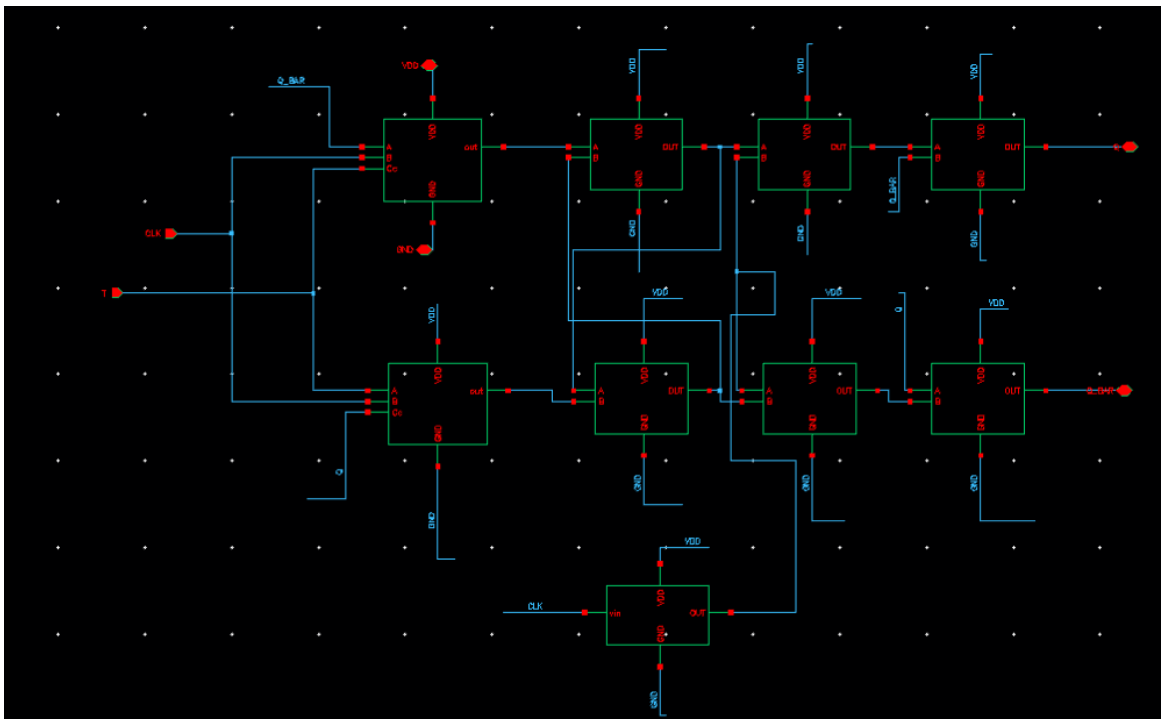


T FLIPFLOPS

A T flip-flop, also known as a “Toggle Flip-Flop,” is a fundamental component in the field of digital electronics. It plays a pivotal role in storing and processing binary data, acting as the building block for various digital systems such as counters, shift registers, and memory devices. Essentially, a T flip-flop is a bistable device, which means it has two stable states. It can store one bit of information, either a ‘0’ or a ‘1’. The ‘T’ in T flip-flop stands for “toggle,” which succinctly describes its behavior. When the input or ‘T’ is high (1), the flip-flop toggles its output state. Conversely, when the input is low (0), the output state remains unchanged.

- **Input T (Toggle):** This is the control input of the flip-flop. Depending on its state, the flip-flop either changes or maintains its output.
- **Output Q:** This is the main output which reflects the current state of the flip-flop.
- **Output Q^{bar}:** This is the inverse of the main output Q. If Q is high, Q^{bar} is low, and vice versa.
- **Clock Input:** This input is used to synchronize the flip-flop’s operation with the rest of the digital circuit.

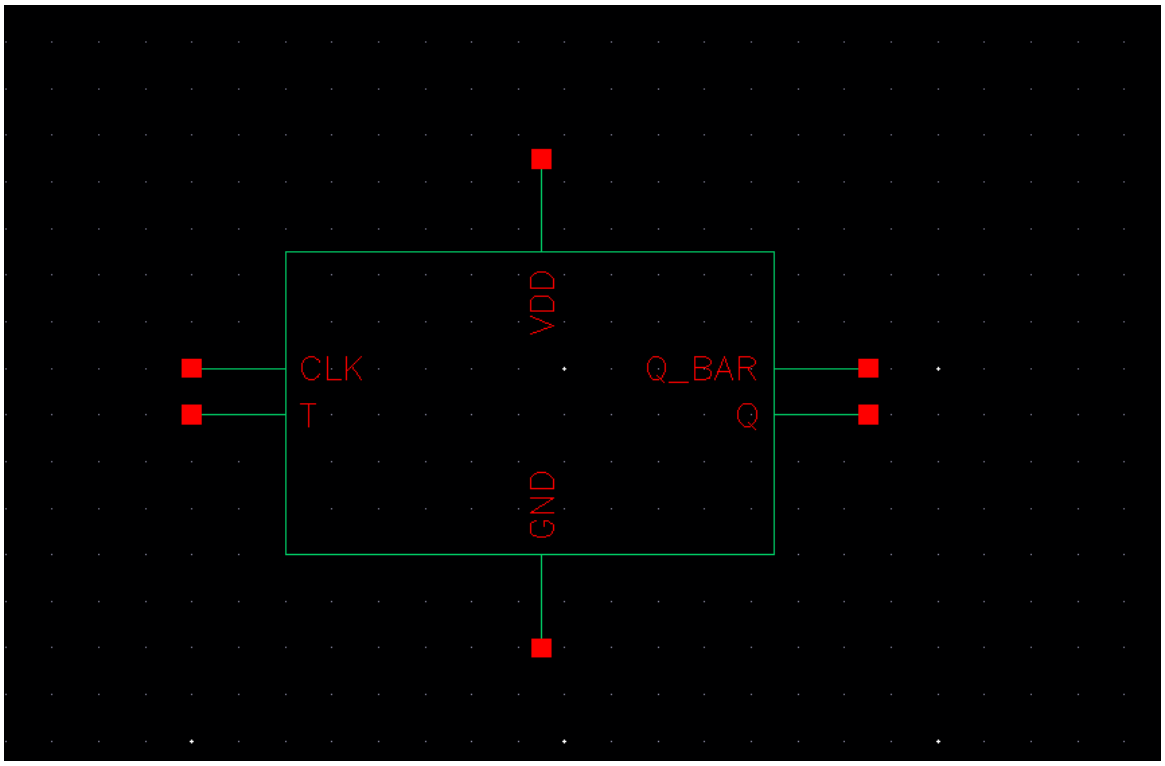
SCHEMATIC OF T FLIPFLOP



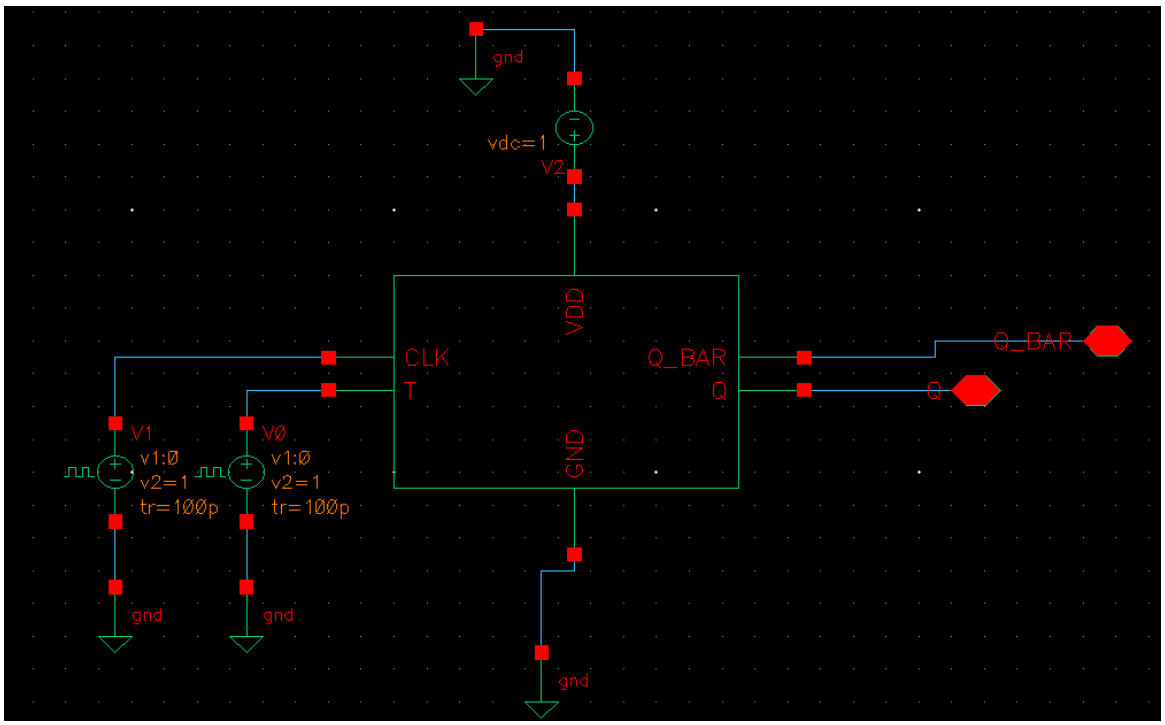
Schematic of T flipflop is done using master-slave JK Flipflops by shorting J and K input and connecting to new input T.

Q and Q_BAR acts as input and output. T and CLK are the input.

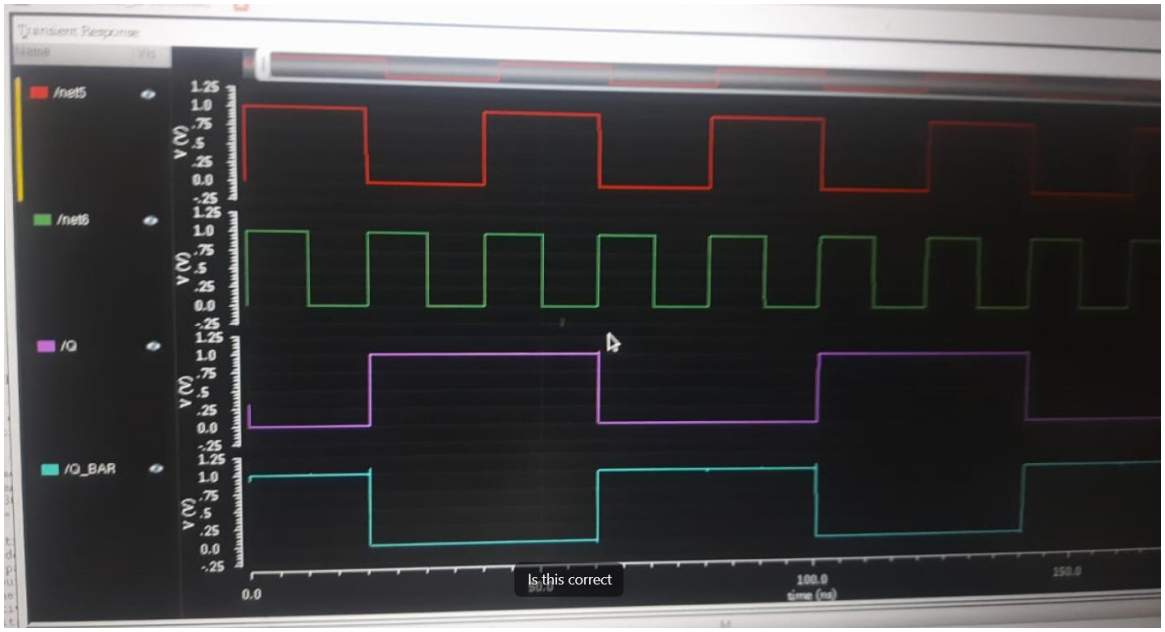
SYMBOL



TESTING THE CIRCUIT



OUTPUT WAVEFORM



Transient analysis of T Flipflops

In the above waveform red color waveforms is clock and green color waveform is T input. In the above waveform we can see that, at the start, the flip-flop has an initial state, typically either set or reset, depending on its design. The flip-flop waits for the clock signal to change from high to low that is, it reacts to the falling edge of the clock signal. The flip-flop has an input called T. If T is high (usually logic 1), the flip-flop toggles its output. If T is low (usually logic 0), the output remains unchanged. If T is high at the falling edge of the clock, the flip-flop toggles its output. If T is low, the output remains the same. The flip-flop maintains its output state until the next falling edge of the clock signal occurs.

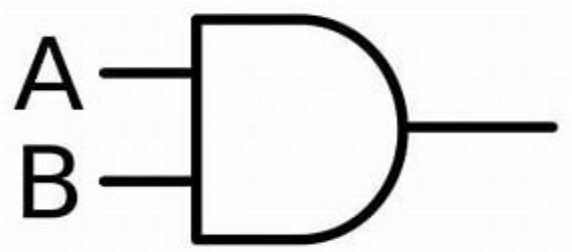
CONCLUSION

The Cadence simulation of the T Flip Flop has demonstrated its efficiency and reliability. Key parameters such as signal integrity, power consumption, and response time were evaluated. The T Flip Flop exhibited low power consumption, minimal signal distortion, and fast response times, aligning with the design requirements and specifications.

AND GATE

An AND gate is a logic gate having two or more inputs and a single output. An AND gate operates on logical multiplication rules. In this gate, if either of the inputs is low (0), then the output is also low. If all of the inputs are high (1), then the output will also be high. An AND gate can have any number of inputs, although 2 input and 3 input AND gates are the most common.

SYMBOL



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

VERILOG CODE

TESTBENCH

This are following commands and library used for digital design of And gate
vi cds.lib – It is used to create cds lib for mapping and make the following entries in new tab
DEFINE and1 lib ./and1.lib
mkdir and1.lib – this library creates a work directory for mapping.
vi hdl.var – it creates variable library and we include following command
DEFINE WORK and1_lib

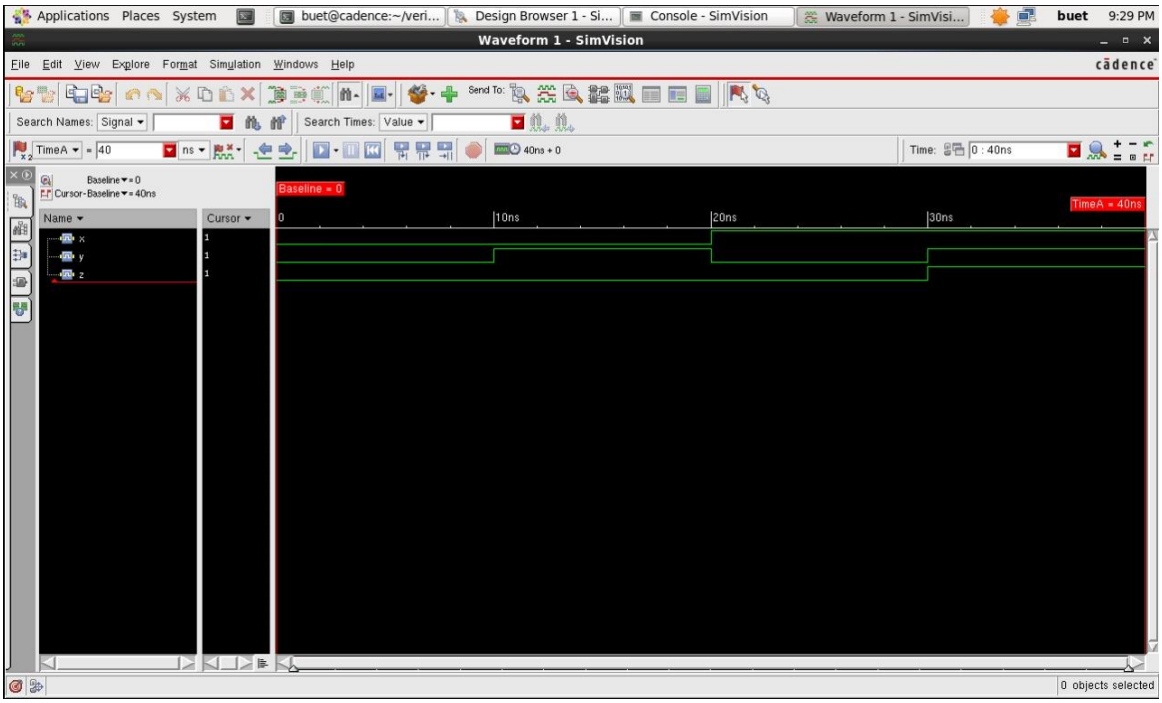
ncvlog and1.v –mess this command is used to compile Verilog code

ncvlog and1_tb.v –mess this command is used to compile Verilog testbench

ncelab and1_tb –access +rwc –mess this is used to read/write access and connectivity.

ncsim and1_tb –gui we use this command to display waveform

OUTPUT WAVEFORMS



Transient analysis of And gate

From the above waveform we can see that if any of the input A and B is low then output is low(logic 0). If both the inputs are high then output ids high(logic 1)

CONCLUSION

The implementation of an AND gate using Verilog in NCSim has been successful. The design process and simulation have deepened our understanding of digital circuits and Verilog. The behavior of the AND gate under various test cases has been insightful.

REFERENCES

[1].

[2]. https://www.cadence.com/

[3].

[4]. https://technobyte.org/verilog-and-gate/