ES204 Digital Systems

Implementation of Tiny Processor

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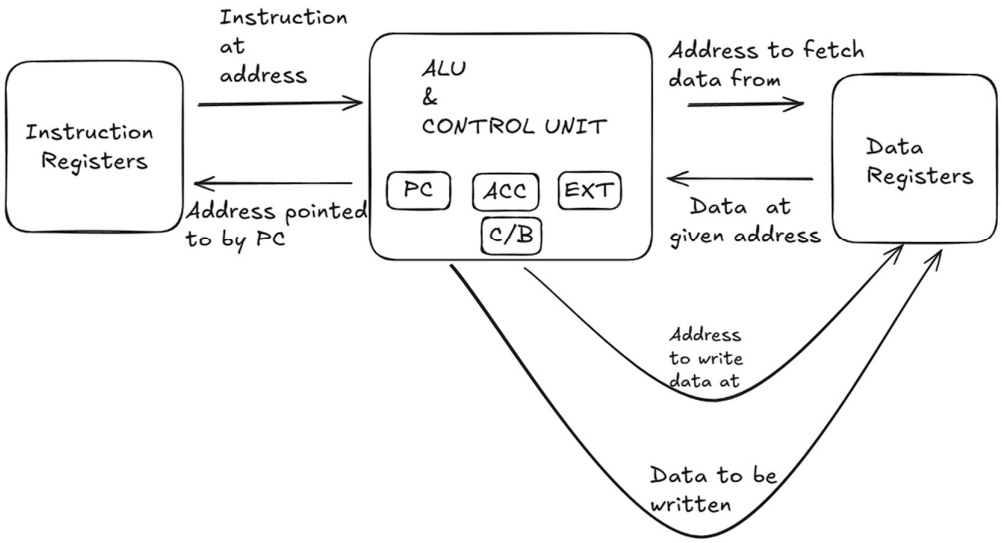
Block diagram of workflow:



As soon as the program counter is updated, the new instruction is fetched from the instruction register and according to the instruction any required data is fetched from the data register. The required computation is done and the **next** value of PC, EXT, ACC, C/B and the data that needs to written onto the data register is stored. In the next clock edge, the registers are updated with the new values and the PC is updated.

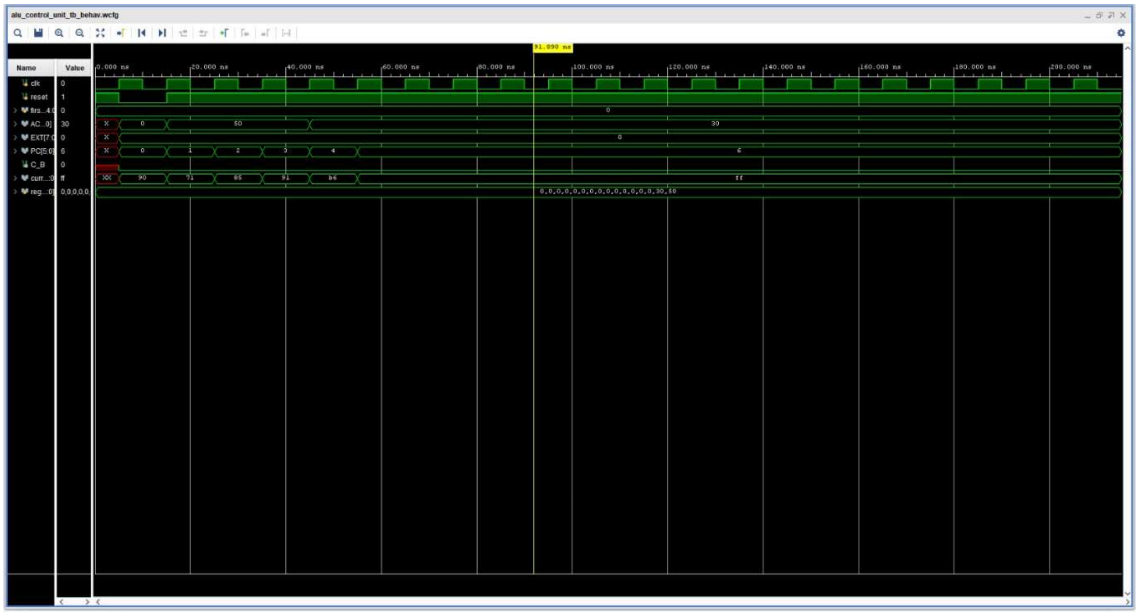
Simulation Results:

Execute ALL Instructions:

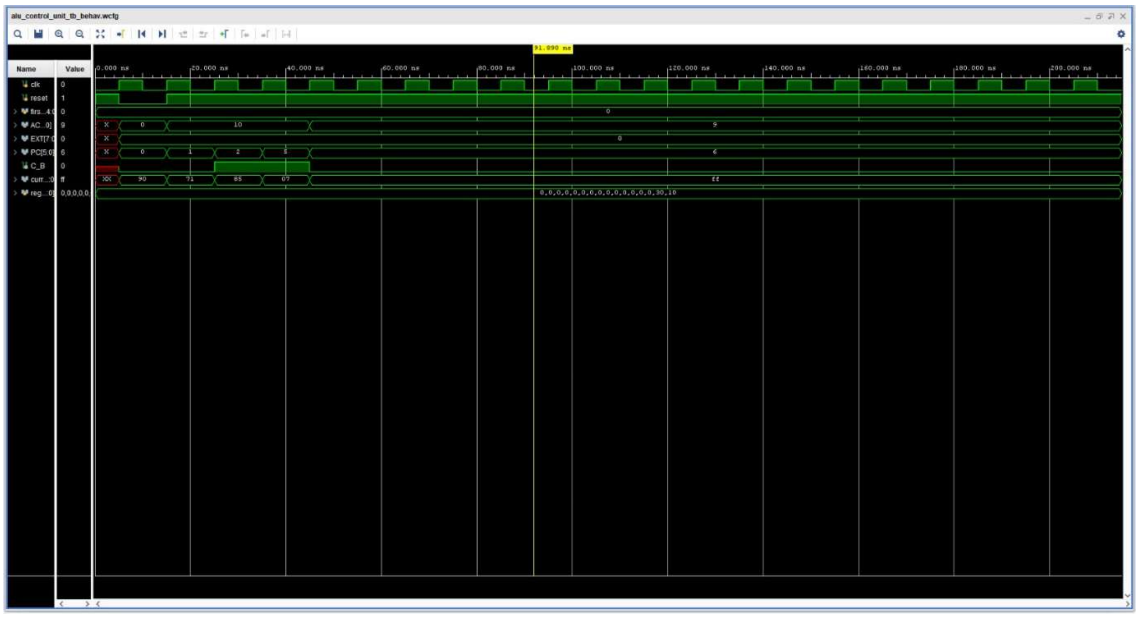
Sample Program:

We write a program for an if-else statement. The program essentially loads a value from a register_0 into the ACC and checks if the new ACC value is greater than or equal to value in register_1. If it is the case then we set ACC to the value of register_1 else we decrement ACC.

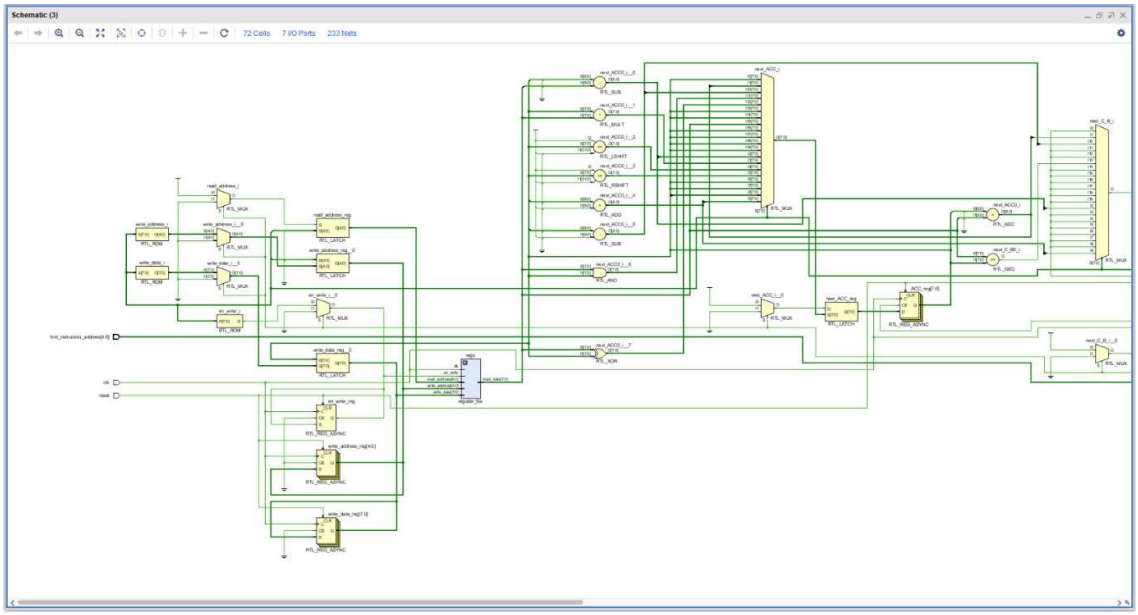
Data registers are set such that IF block is executed:

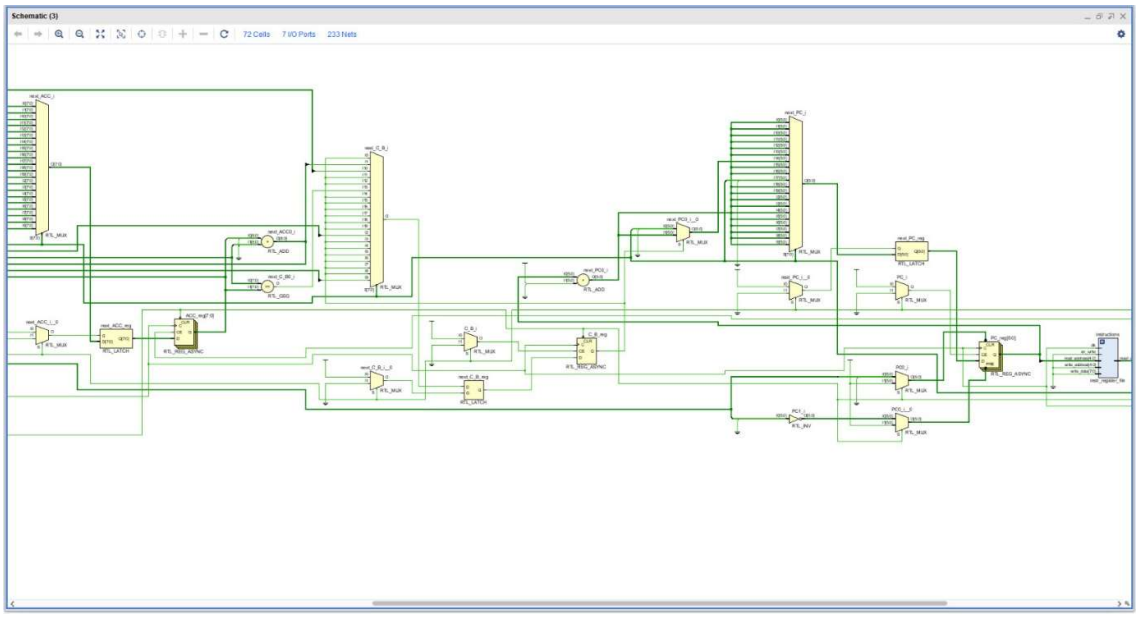


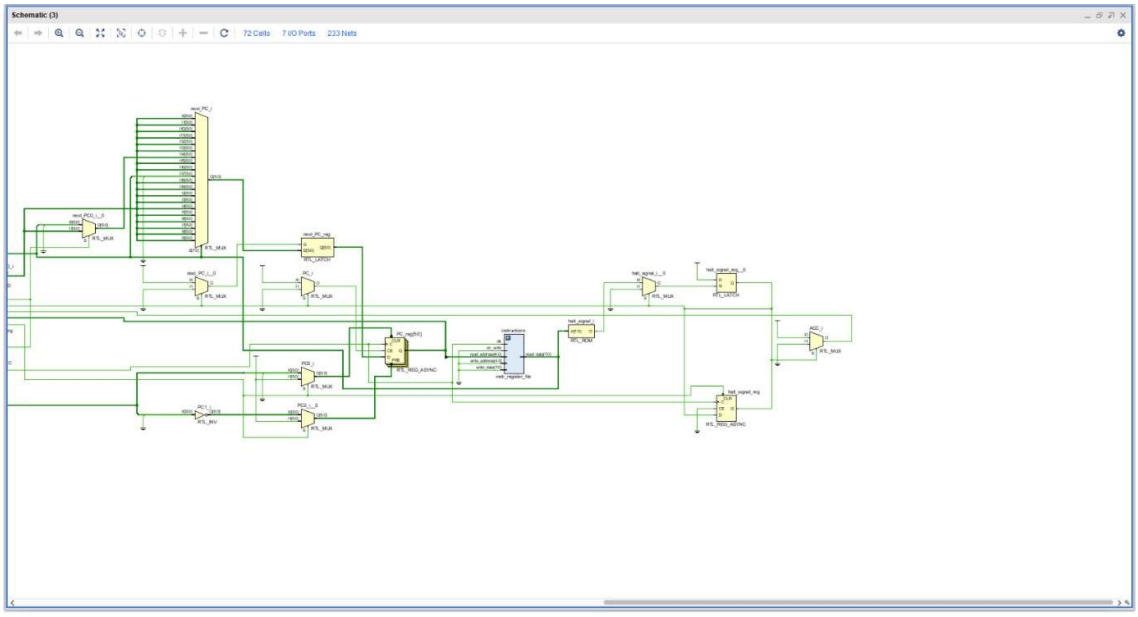
Data registers are set such that ELSE block is executed:



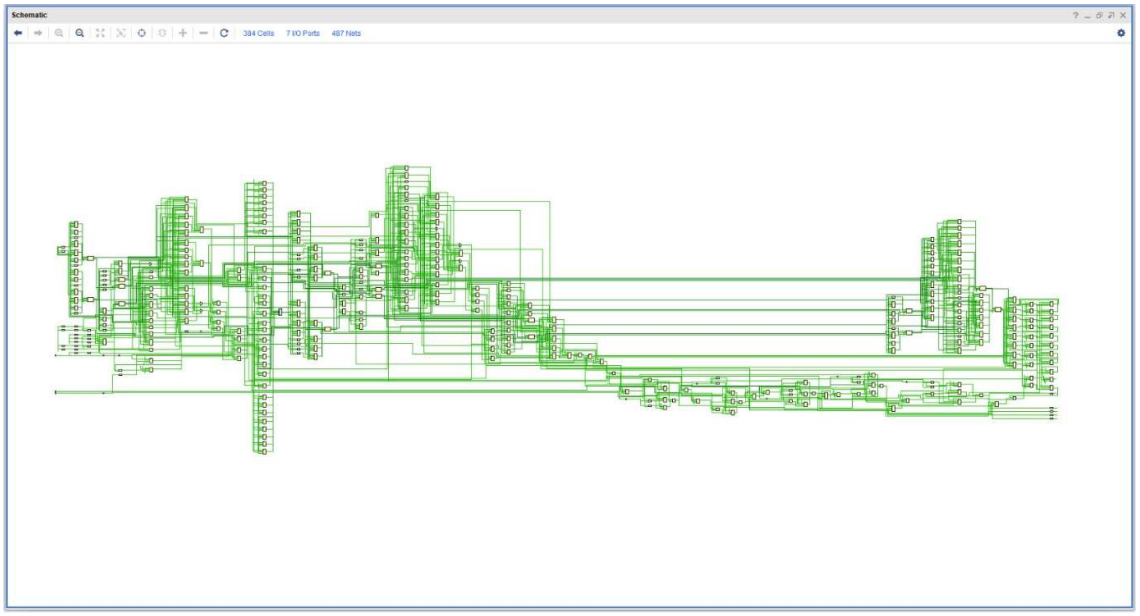
RTL Analysis Schematic:

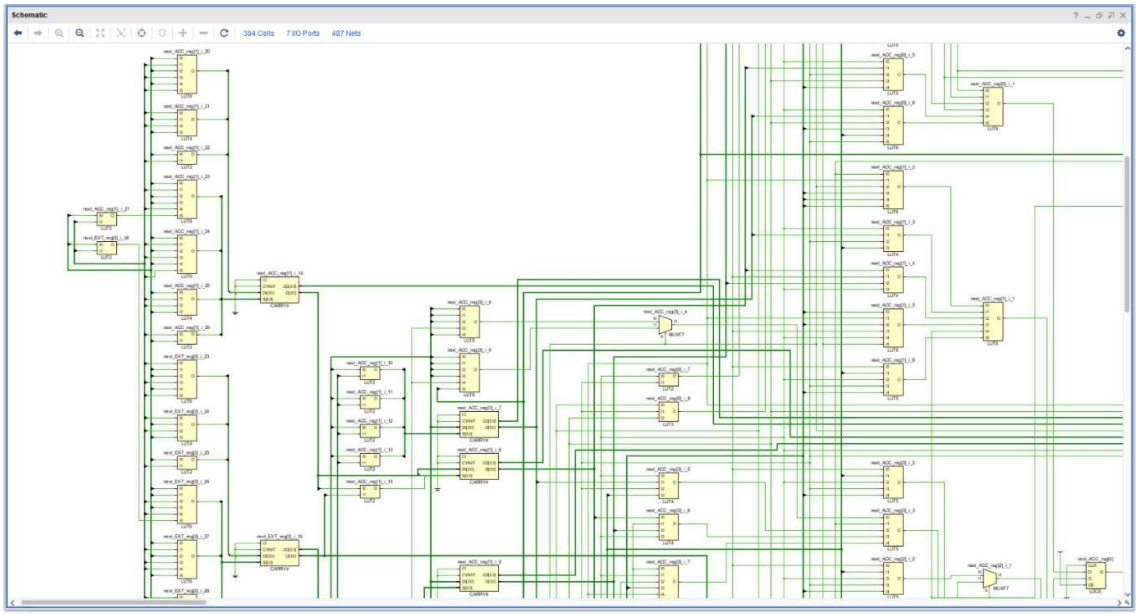


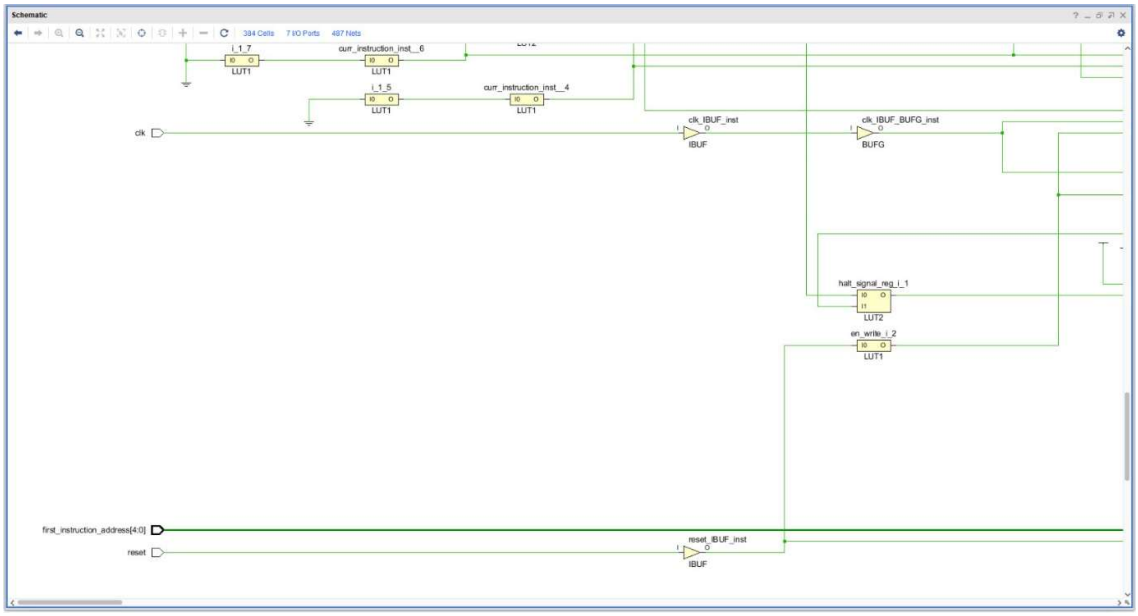


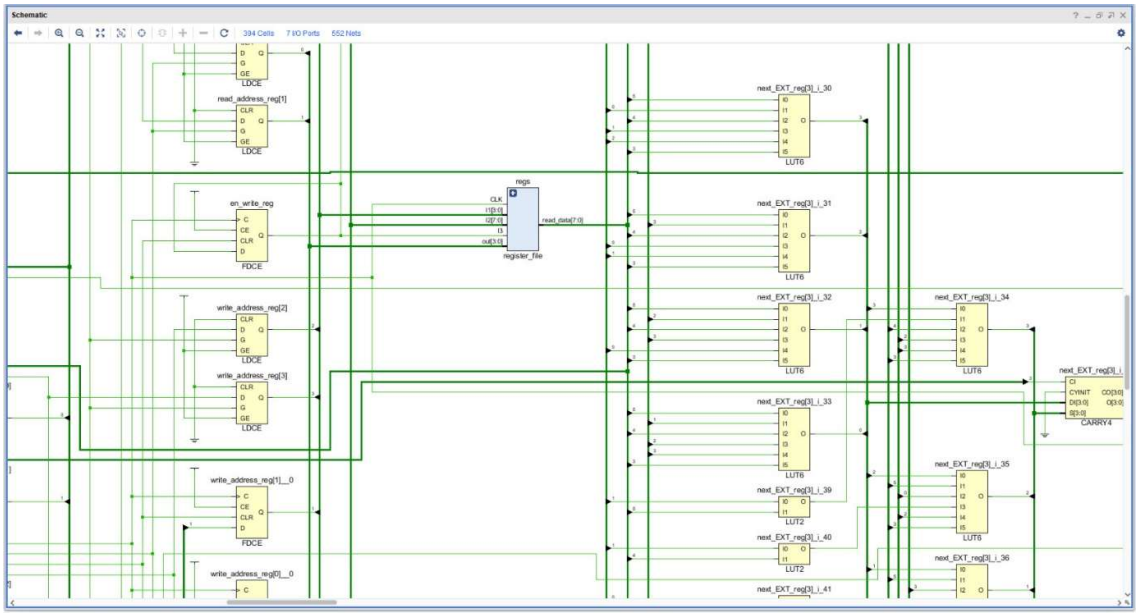


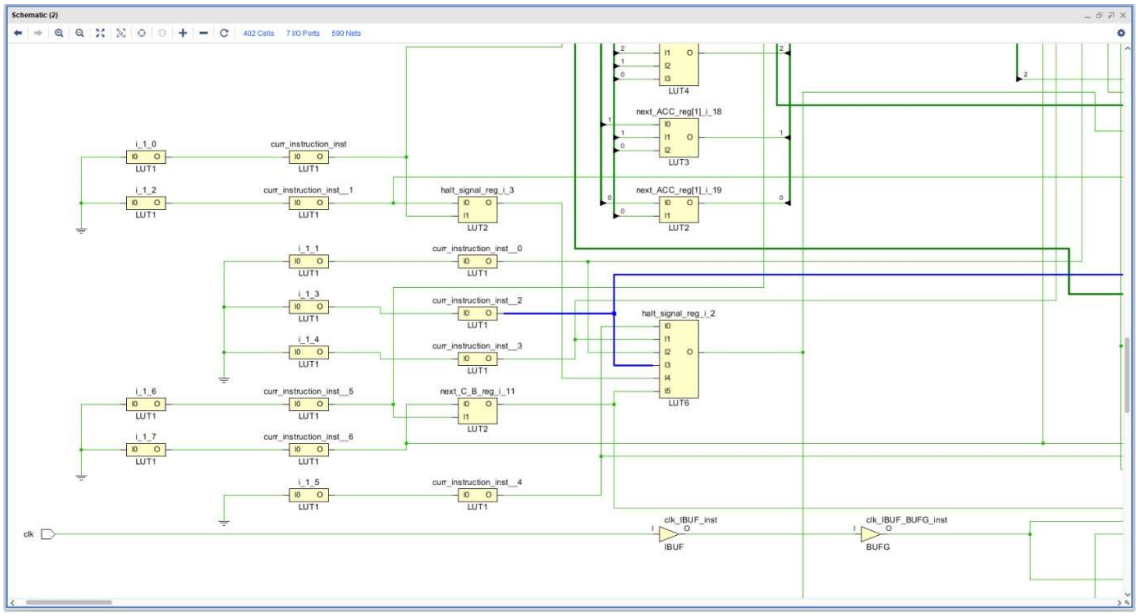
Synthesis Schematic:


Schematic
384 Cells
7 I/O Ports
487 Nets


Schematic
384 Cells
7 I/O Ports
487 Nets


Schematic
384 Cells
7 I/O Ports
487 Nets
i_1_7
LUT1
curr_instruction_inst__6
LUT1
i_1_5
LUT1
curr_instruction_inst__4
LUT1
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
halt_signal_reg_i_1
LUT2
en_write_i_2
LUT1
first_instruction_address[4:0]
reset
reset_IBUF_inst
IBUF


Schematic
394 Cells
7 I/O Ports
552 Nets
LDCE
read_address_reg[1]
LDCE
en_write_reg
FDCE
regs
register_file
read_data[7:0]
write_address_reg[2]
LDCE
write_address_reg[3]
LDCE
write_address_reg[1]__0
FDCE
write_address_reg[0]__0
next_EXT_reg[3]_i_30
LUT6
next_EXT_reg[3]_i_31
LUT6
next_EXT_reg[3]_i_32
LUT6
next_EXT_reg[3]_i_34
LUT6
next_EXT_reg[3]_i
CARRY4
next_EXT_reg[3]_i_33
LUT6
next_EXT_reg[3]_i_35
LUT6
next_EXT_reg[3]_i_39
LUT2
next_EXT_reg[3]_i_40
LUT2
next_EXT_reg[3]_i_36
next_EXT_reg[3]_i_41


Schematic (2)
402 Cells
7 I/O Ports
590 Nets
LUT4
next_ACC_reg[1]_i_18
LUT3
next_ACC_reg[1]_i_19
LUT2
i_1_0
curr_instruction_inst
LUT1
i_1_2
curr_instruction_inst__1
halt_signal_reg_i_3
LUT2
i_1_1
curr_instruction_inst__0
LUT1
i_1_3
curr_instruction_inst__2
LUT1
halt_signal_reg_i_2
LUT6
i_1_4
curr_instruction_inst__3
LUT1
i_1_6
curr_instruction_inst__5
next_C_B_reg_i_11
LUT2
i_1_7
curr_instruction_inst__6
LUT1
i_1_5
curr_instruction_inst__4
LUT1
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG